passivation material. Then the wafer bumping process, illustrated in Fig. 4.6, involves the placement of small solder bumps directly to the aluminum pads of the dies. These solder bumps (small balls) are utilized to make solder connections to the pads on the PCB.

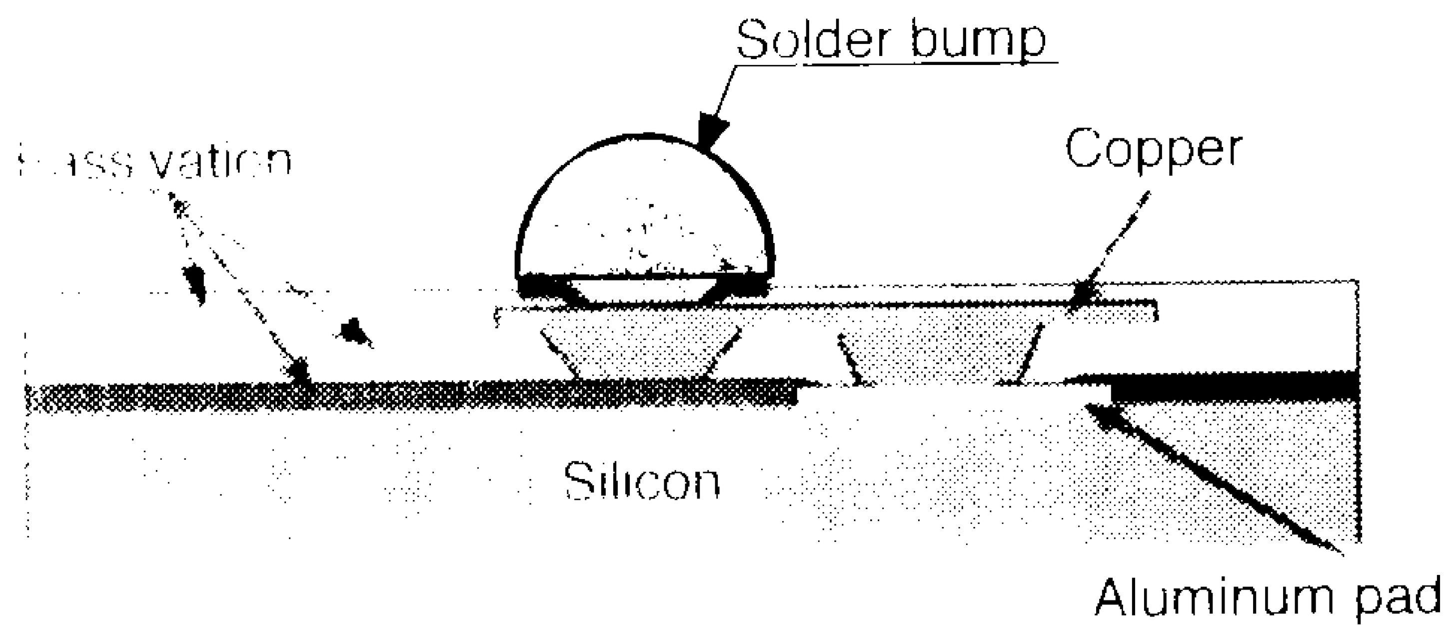

Fig. 4.6 Placement of a solder bump directly on a chip to facilitate direct attachment to a PCB

Several different substrates are employed with direct die attachment. Ceramic and glass-ceramic substrates exhibit excellent dielectric and thermal properties. Organic substrates that weigh and cost less than the ceramic and glass ceramic substrates are also used. These organic substrates have the advantage of lower dielectric constant. Flexible substrates that are pliable, have the ability to bend and support relatively dense circuits are used in some products.

The DDA process consists of only a few steps. For DDA with wire bonding, the chip is adhesively bonded to the PCB with its face up. The connections from the chip to the PCB are made with wire bonding. Then the die and wires are encapsulated with a plastic to protect it from the environment. For flip-chip bonding, solder bumps on the chip are aligned with the pads on the PCB and the mechanical and electrical connections are made by melting (reflowing) the solder bumps. If the PCB is made from an organic laminate it is necessary to fill the small gap between the chip and the PCB. This process, known as underfilling, reduces the thermally induced shear strain on the solder bumps and extends the cyclic life of the product. The installation may be encapsulated to further protect the chip from mechanical and chemical damage.

4.2.2 Through-Hole Chip Carriers

The concept of through-hole chip carriers is illustrated in Fig. 4.7 where a cut away view of the chip carrier and circuit board is shown. With this approach the bonding pads on the chip are connected to leads that extend from the chip carrier. These leads are then inserted into plated-through-holes found on the circuit board. After insertion the leads are clinched and cut. The clenched leads hold the chip carriers in place on the PCB prior to soldering. The solder joints are made in a wave soldering process that is described in Chapter 6. The solder joints serve to mechanical fasten the chip carrier to the circuit board and to make the required electrical connections.

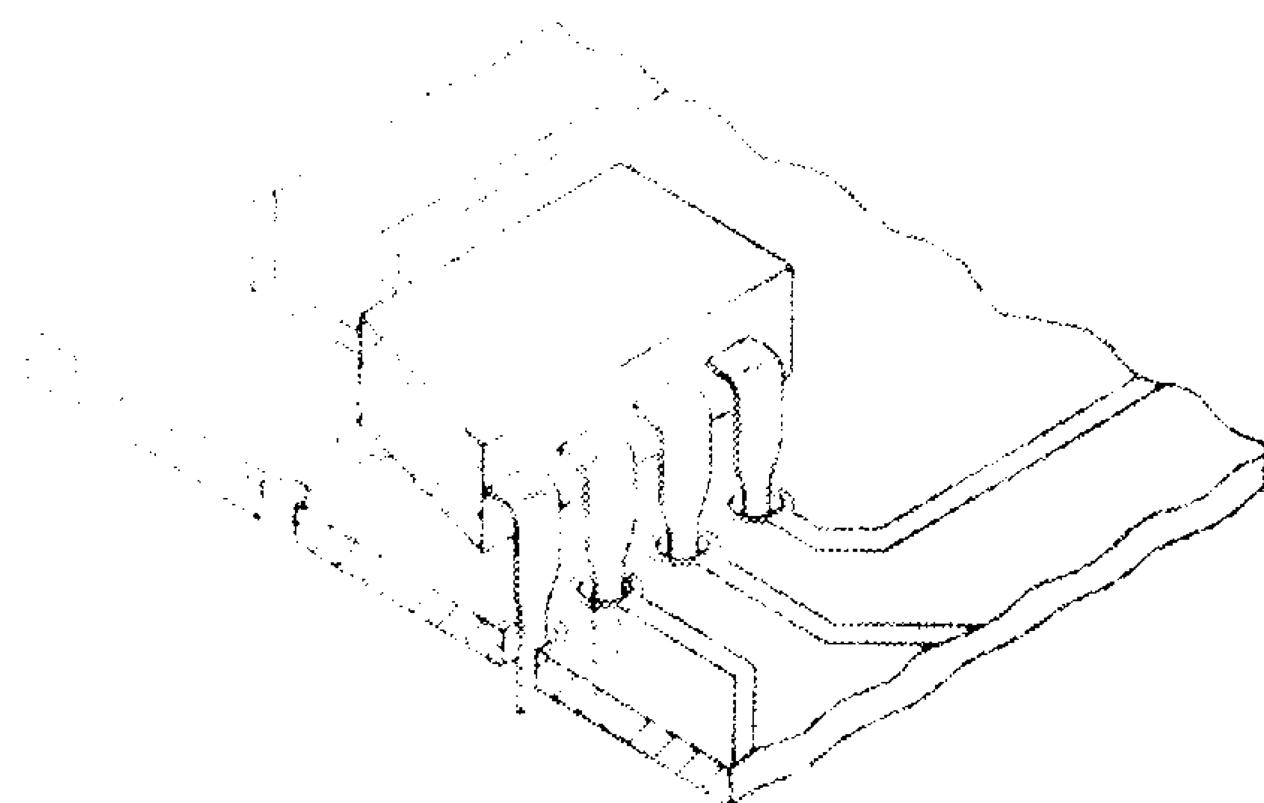

Fig. 4.7 Chip carriers with leads for through-hole mounting

Metal Cans

The TO can is the oldest type of chip carrier and its shape reflects the transition from vacuum tubes to the design of packages to house low I/O count transistors on very small silicon chips. The pins emerge from bottom of the package on a pin circle. TO cans are still used today to house discrete devices, such as chips intended for power transistors or silicon control rectifiers where power dissipation is very high and the lead count is small. In some instances, the TO can is fitted with a flange that serves as a heat sink as shown in Fig. 4.8. The flange provides a large contact area for heat dissipation, and is bolted directly to a heat frame to complete a low resistance thermal path from the chip to the heat frame.

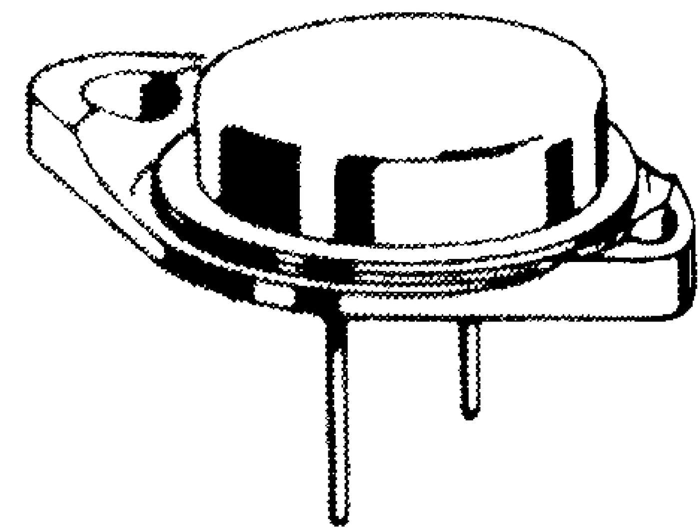

Fig. 4.8 A TO can with a heavy flange to enhance heat transfer from its base.

The DIP

One of the oldest types of chip carrier found in electronic packaging today is the DIP (dual in-line package) that is illustrated in Fig. 4.9. The DIP incorporates two rows of pins which are arranged on 100 mil (2.54 mm) centers along the longer side of the rectangular package. The standard DIP family of chip carriers is available in different sizes and accommodates I/O count from 8 to 64. The pins are short and relatively large in cross sectional dimension, which makes them stiff and robust. This robustness is an advantage in automatic assembly as the leads are inserted into holes on the circuit board by pick and place machines. The pins inserted through the circuit board are all soldered from the underside of the board by passing the assembled PCB through a standing wave of molten solder. With this wave soldering process, all of the solder joints on the board are made quickly and efficiently in a single pass through the wave. The width of the pins is increased near the body of the chip carrier to provide a shoulder that serves to seat the DIP a distance 20 to 40 mil[1] (0.51 to 1.02 mm) from the top surface of the circuit card. This stand off is necessary to provide a space under the carrier so that solder fluxes can be cleaned from the board after assembly is complete. Removal of the solder flux is important to prevent corrosion of the exposed metal on the PCB.

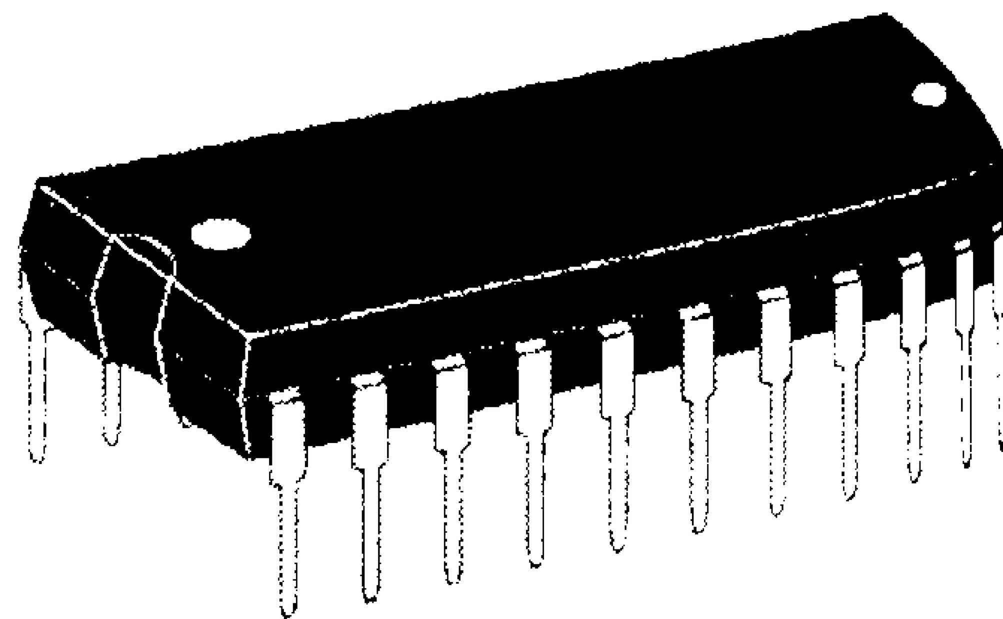

Fig. 4.9 Illustration of a 22 pin dual-in-line-package (DIP).

The internal details of the DIP are presented in the cut away view shown in Fig. 4.10. The chip is bonded, back side down, to a lead frame using an adhesive such as epoxy. The I/O pads on the chip are connected[2] to the leads with wire bonding. The chip is then tested to insure that it is functioning correctly. The assembly is then placed in a two side mold and a silica-filled epoxy is injection molded about the chip, bonding wires and leads. The leads are then clipped to size and plated to prevent corrosion during storage.

[1] Mil is still commonly used as a unit in specifying dimensions in the packaging business. One mil is equal to 0.001 in., or 0.0254 mm or 25.4 μm.

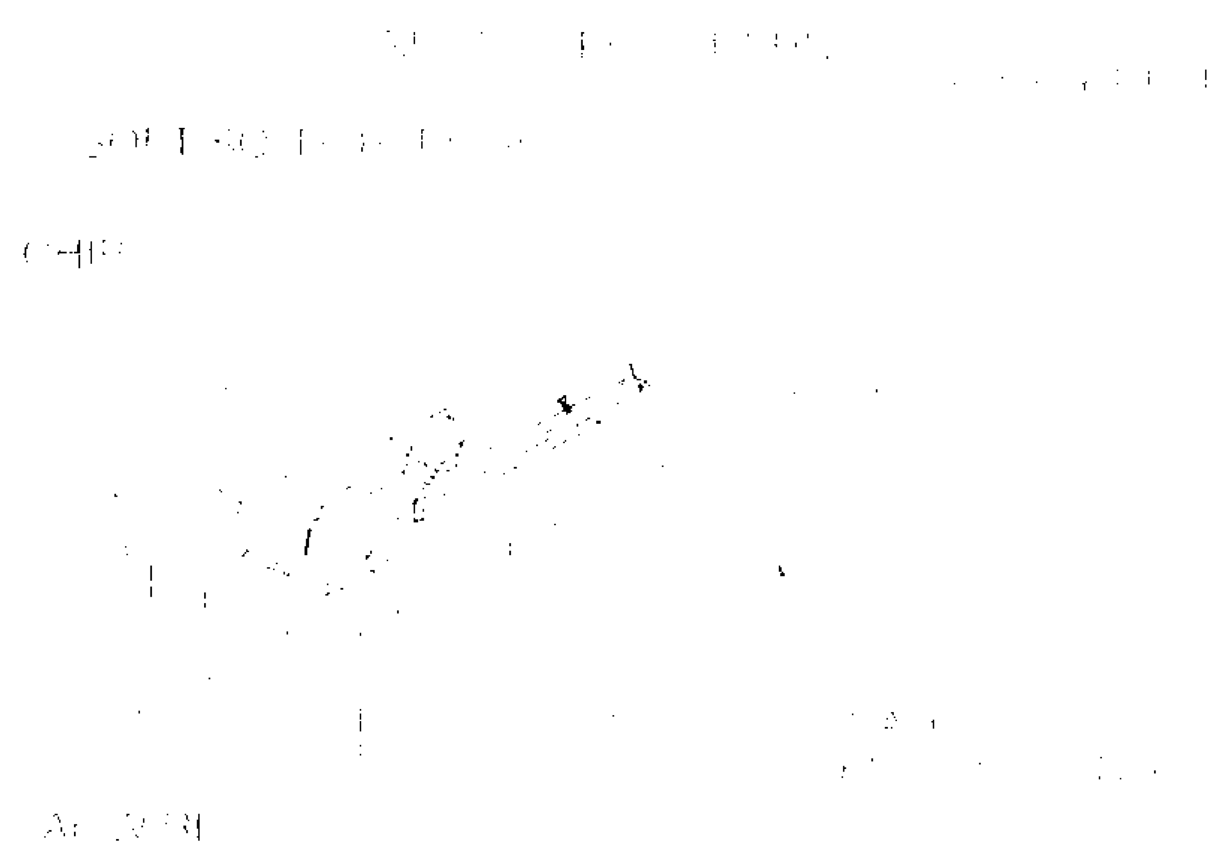

Fig. 4.10 Cut away view showing construction details of a DIP.

The standard DIPs have a lead pitch specified as 0.100 (2.54 mm) and the row spacing of 0.300 in. (7.62 mm). However, several DIP variants exist, mostly differentiated by packaging material and lead pitch.

- Ceramic Dual In-line Package (CERDIP)
- Plastic Dual In-line Package (PDIP)
- Shrink Plastic Dual In-line Package (SPDIP) – A shrink version of the PDIP with a 70 mil (1.778 mm) lead pitch

Plastic cases formed by injection molding are low cost and provide suitable housings for low and moderate cost product. Ceramic cases are used for product which has stringent hermeticity requirements. These ceramic cases are much more costly than molded plastic packages and their application is usually limited to military products that require a high degree of hermeticity to achieve the high reliabilities necessary for strategic systems. Ceramic chip carriers are also used with high performance commercial computers and signal processors where system availability is essential.

The DIP family has some disadvantages which include poor area efficiency, limited I/O count and poor wirability that limit its usefulness in housing modern high density logic chips. The area efficiency is poor because in most cases the pins are on 100 mil (2.54 mm) centers and deployed on only two sides of the package. In more area efficient chip carriers, the pins are on 50 mil (1.27 mm) centers (or less) and are deployed on all four sides of the package. The maximum I/O count on a standard DIP is limited to 64. To increase this I/O count without changing the pin pitch would require prohibitively long packages with significant lead lengths within the chip carrier. Wirability is poor because the through-hole mounting requires annular solder pads on the circuit board with an outside diameter of about 50 mil (1.27 mm). These pads leave only 50 mil (1.27 mm) for the wiring channel between pins, which cause a problem in providing for more than three wiring traces per wiring channel. A detailed description of wiring channels is presented in Chapter 5.

Other In-line Chip Carriers

The single-in-line package (SIP) is presented in Fig. 4.11. This package is similar to the DIP except it features a single row of pins on 100 mil (2.54 mm) centers. The chip in the SIP is mounted on a metal lead frame and encased with a filled plastic. It is used to house chips with relatively low I/O count.

Fig. 4.11 Single-in-line package (SIP).

Another through-hole chip carrier, known as a ZIP, is shown in Fig. 4.12. The ZIP is similar to the SIP because the chip is mounted perpendicular to the surface of the printed circuit board. However, with the ZIP the pins are narrow and staggered. While the pins are on 100 mil (2.54 mm) centers, the staggered pattern essentially reduces the projected pitch to 50 mil (1.27 mm).

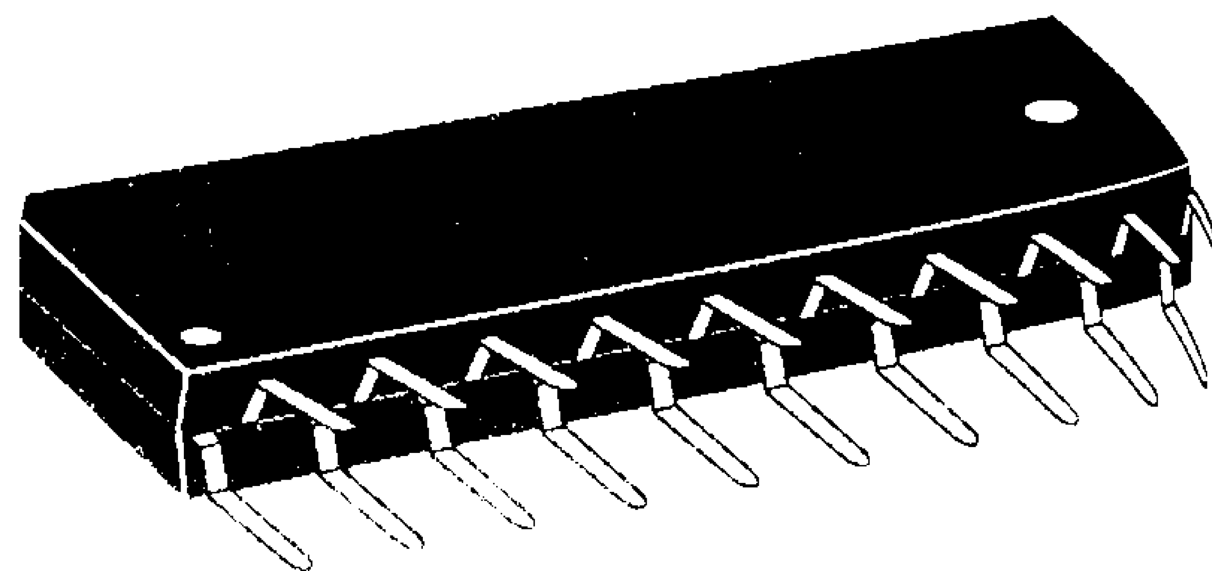

Fig. 4.12 Zigzag in line package (ZIP) utilizes staggered pins to reduce their effective pitch to 50 mil (1.27 mm)

The Pin-Grid-Array

Pin-grid-array carriers are employed as a substitute for DIP's when additional I/O count is required or if lower thermal resistance is necessary. The pin array carrier, illustrated in Fig. 4.13, shows the general features of this design. The body of the package is fabricated from either organic laminate or ceramic (usually a multi-layer alumina) depending on hermeticity requirements. The body provides a cavity for the chip. A ledge around the cavity is used as the support surface for bonding pads that are the connections for the bonding wires which lead to the chip. Vias (holes containing conductors) lead from these pads to intermediate signal and power planes which carry the wiring traces from the vias to the pin locations. The pins which are 20 to 25 mil (0.51 to 0.64 mm) in diameter are brazed into the ceramic substrate[2]. After the chip is bonded in the package, a ceramic or Kovar (an alloy with a low coefficient of thermal expansion) lid is placed over the cavity and sealed using inorganic solders that do not outgas.

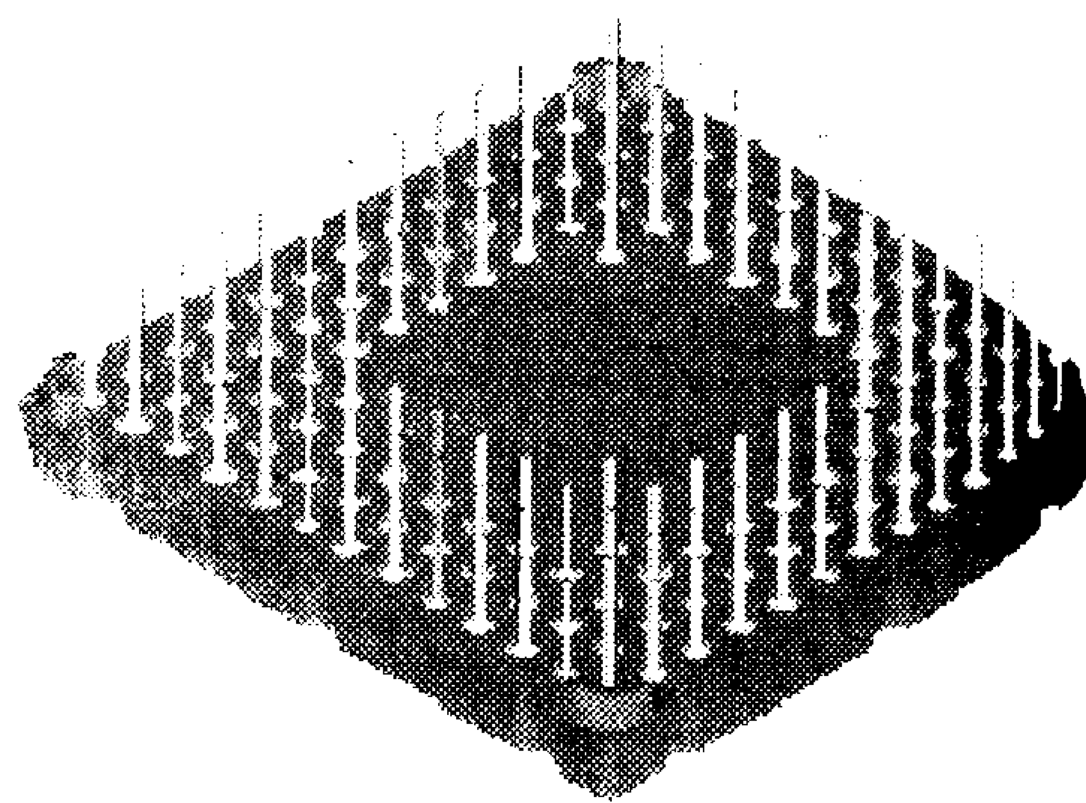

Fig. 4.13 Photograph of a pin-grid-array (PGA) showing pins deployed over the bottom surface of the chip carrier.

There are several variations in the design of the PGAs, mostly differentiated by packaging material and lead pitch.

- Ceramic Pin grid-array (CPGA)
- Ceramic Micro Pin grid array (CµPGA)
- Organic Pin-grid-array (OPGA)
- Organic Micro Pin-grid-array (OµPGA)

[2] If the pin grid array (PGA) is fabricated from plastic, the pins are molded into the body of the package.

With the ceramic pin-grid-array, flip chip with C4 connections provide several advantages—increased I/O count, smaller chip size because the perimeter pads are not necessary, shorter electrical connections and improved manufacturing efficiency. The micro pin-grid-arrays are on 50 mil (1.27 mm) centers and consequently pin counts are increased by a factor of four for the same package size. The CμPGA are available with pin counts up to 940 in a package with dimensions of $7 \times 40 \times 40$ mm.

Organic chip carriers are built with resin based materials such as the higher grade epoxy bismaleimide triazine (BT) reinforced with glass fibers, or the more traditional epoxy-glass circuit boards. The BT carriers evolved from printed wiring board technology and utilize plated-through-hole vias for their layer to layer connections. Another type of substrate for chip carriers, developed by IBM, is the called a surface laminar circuit, which uses a standard PCB to provide a high-density surface layer. This density is achieved by substituting microvias for the plated-through-hole vias thereby providing a two- to three-times reduction in the land diameter. This substrate design eliminates the relatively thick surface layer of copper foil that is used in the standard PCB design. With a lower total external copper thickness, finer lines and spaces can be used on package fan-outs as illustrated in Fig. 4.14. Organic chip carriers can achieve pin counts exceeding 1,000. Chips are attached either by thin gold wires with bond pad pitch spacings as low as 60 μm or less or by flip chip.

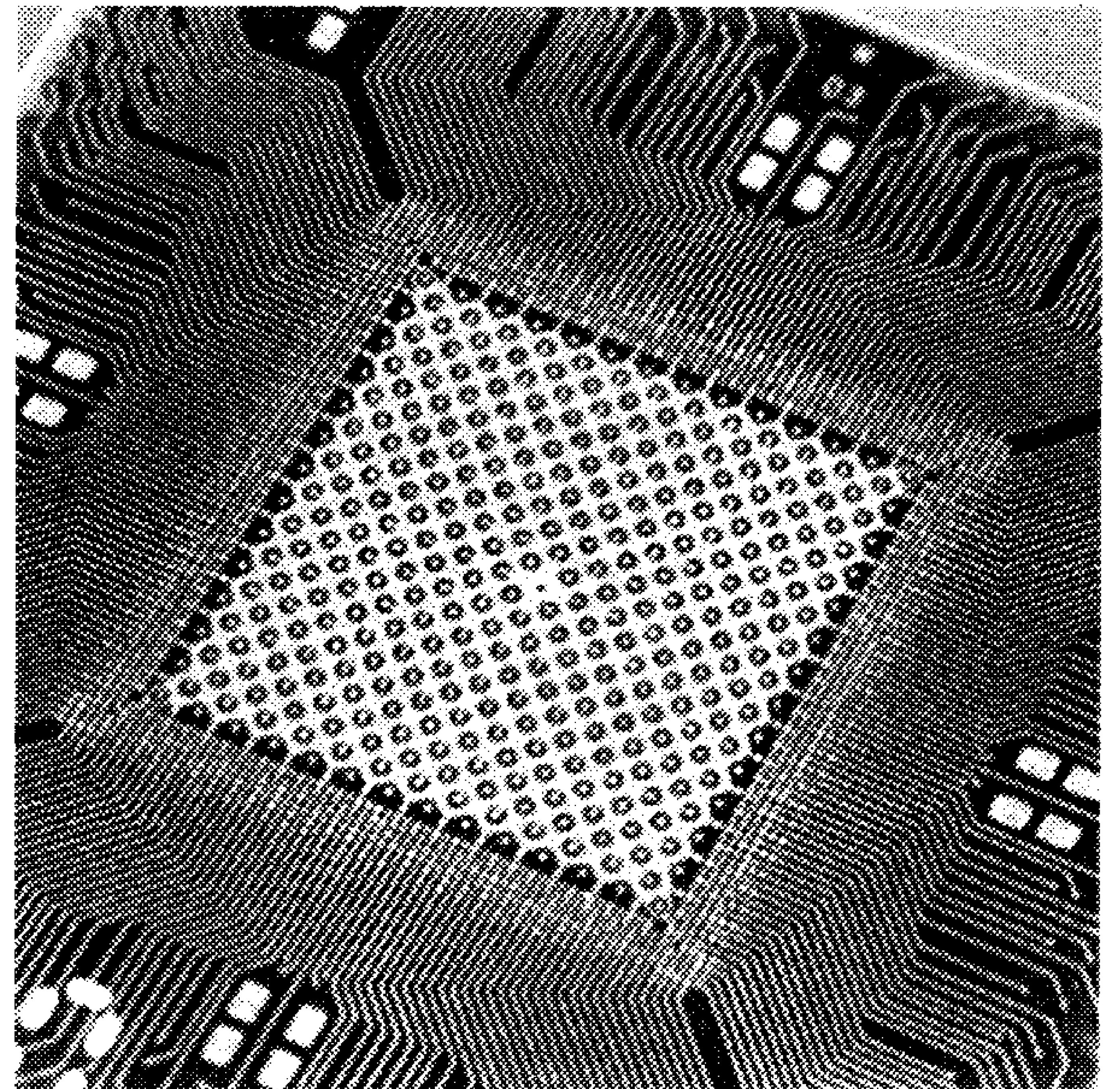

Fig. 4.14 Fine pitch circuit lines etched on organic laminate to produce the fan-out required for a OμPGA.

With pin-grid-arrays, intended for chips having a high power rating, the surface area directly below the chip is not used for pins. Instead, this area is reserved for a low resistance thermal path leading to a heat frame. The method of coupling the heat frame to the package is illustrated in Fig. 4.15. Through vias, located directly beneath the chip are filled with solder to provide a high conduction path to the bottom surface of the chip carrier. A heat sink is employed that contacts the bottom of the package and extends completely through the PCB to the heat frame. While pin-grid-arrays handle very large I/O count and can be designed to couple directly with a heat frame, they have two disadvantages. Firstly, they are relatively high in cost because the production processes for multi-layered ceramics are limited to a very few companies and the market is not competitive. The ceramic PGAs are usually employed on only high-end applications where hermeticity is important. Second, the cost of the PCB is elevated because of the need to drill and plate the large number of holes required for the pins. Lower cost chip carriers using solder balls instead of pins offer a lower cost alternative in many applications.

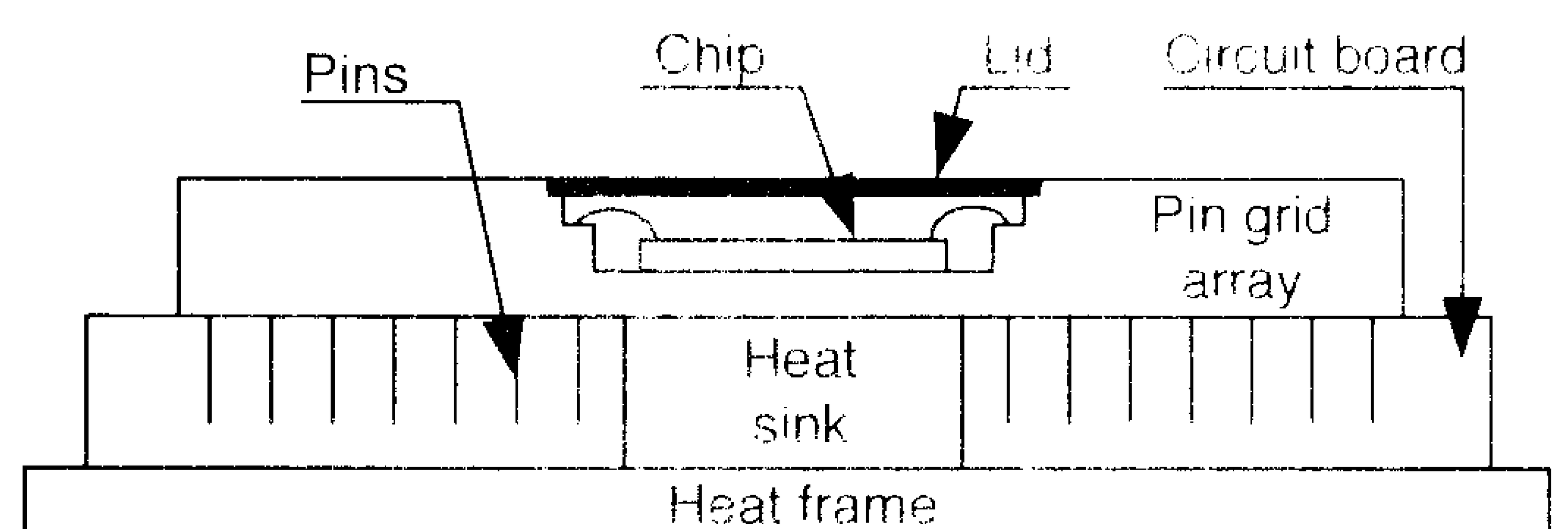

Fig. 4.15 Placing a heat sink directly below a PGA chip carrier facilitates heat flow through the circuit board to the heat frame.