CHAPTER 4

FIRST LEVEL PACKAGING--- THE CHIP CARRIER

4.1 INTRODUCTION

The chip carrier is the housing for a thin and fragile silicon chip. The chip carrier serves several purposes. Firstly, it protects the chip from the detrimental effects of the environment (humidity and dust). Second it protects the chip from damage due to abusive handling in assembly. Third, it isolates the chip from the forces due to either shock or vibration that may occur in service. Fourth, it serves to facilitate the interconnection of the circuits on the chip which are extremely compact to the more widely spaced interconnecting pads or holes located on the circuit boards. Package design has a major impact on chip performance and functionality. Finally, the chip carrier serves to facilitate the assembly process by providing a rugged housing which can be handled with automatic machinery without endangering the chip. The chip carrier also provides pins, leads or pads which serve as bases for solder joints. These pins, leads and/or pads are designed so that the solder joints can be made with automatic soldering processes without danger of solder defects such as solder bridges between leads, joints with insufficient solder, solder splatter, or voids of significant size in the solder. The chip carrier is also involved in the heat transfer process. The heat generated on the circuit surface of the chip must pass through the chip and then through the carrier as the first step in the path of heat flow from the source to the heat sink.

There are several markedly different approaches to the design of a first level package. The two main stems of the different design approach are illustrated in Fig. 4.1.

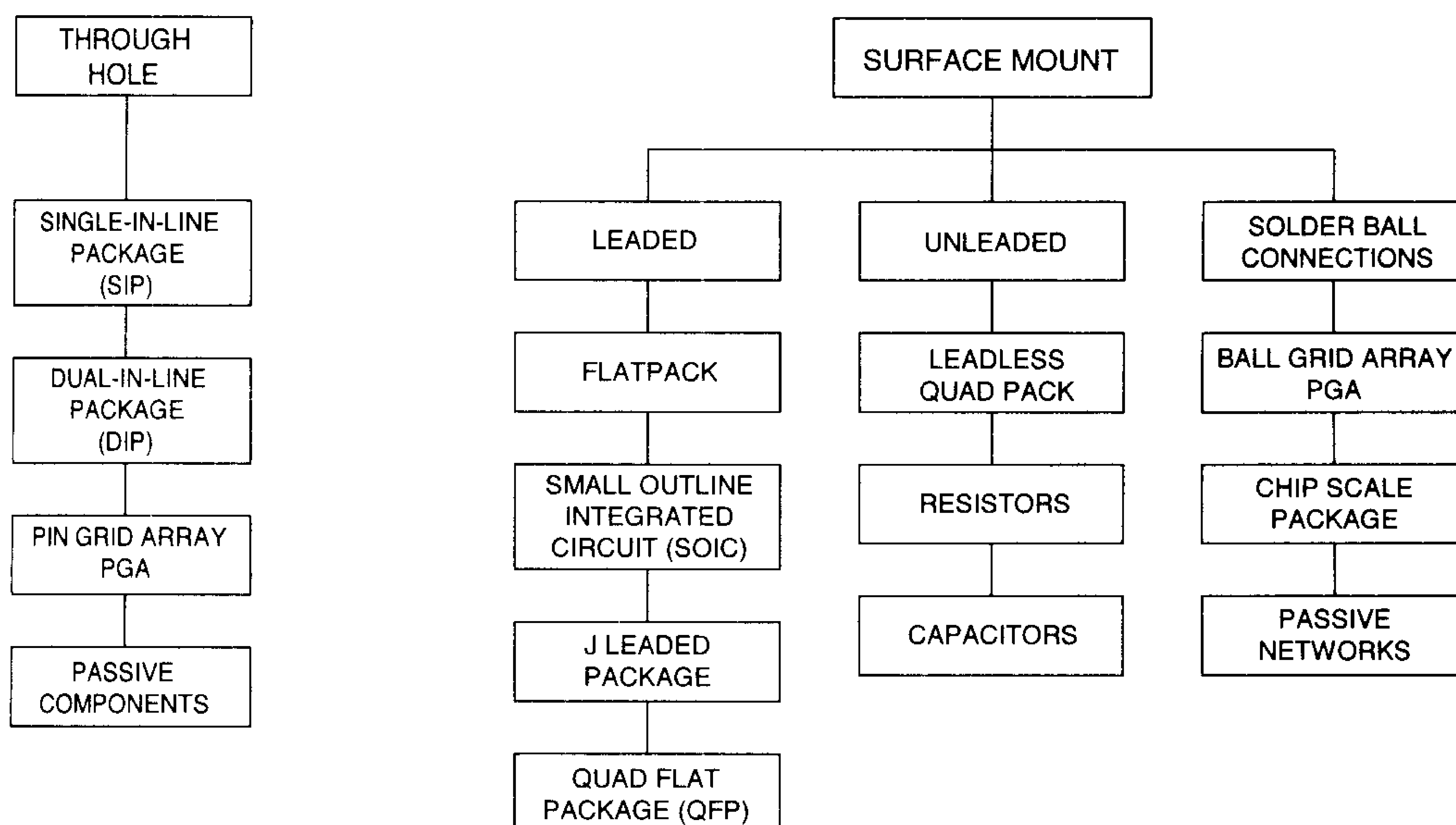

Fig. 4.1 The first level packages can be divided in two classes—through-hole and surface mount.

The materials used to fabricate the packages are also different depending on the application. Some chip carriers are made from molded plastic, others from ceramic and some modern chip carriers are constructed with laminated organic materials.

Still another distinguishing feature is the method of connecting the I/O pads on the chip to the first level package. The older method, still widely used, is wire bonding thin gold, aluminum or copper wires to connect the pads. In more modern approaches, the chip is flipped and C4 (controlled collapsible chip connections) are made between the pads deployed over the area of the chip and those on the chip carrier.

A final feature in the design of a chip carrier is its thermal resistance. Many logic type chips generate significant amount of heat (tens of watts) that must be dissipated without a large increase in the temperature of the chip. Some chip carriers are design with thermal vias and others with metal lids that contact the back of the chip and allow for attachment of a heat exchanger.

In more mature designs, the parts of the chip carrier include the chip as the central element, the case, the leads and lead frame, the chip to package bond, the bonding wires and the lid, as indicated in Fig. 4.2. In this chip carrier, the bonding wires are welded to bonding pads distributed around the perimeter of the chip. Many different types of chip carriers in use today conform closely in concept to the design shown in this figure. Unfortunately this concept, while commonly utilized, is deficient from two different view points. First, the flow of heat from the chip is severely limited as both the top and bottom surfaces are bounded by wiring planes which are thermal insulators. The dissipation of heat from this type of chip carrier is difficult and severe thermal penalties are encountered with chip carriers having wiring schemes that thermally isolate the chip. Second, the single row of bonding pads about the perimeter of the chip limit the number of I/O that this type of chip carrier can accommodate. As a consequence it is not suitable for many high performance chips with millions of transistors that require a very high I/O count.

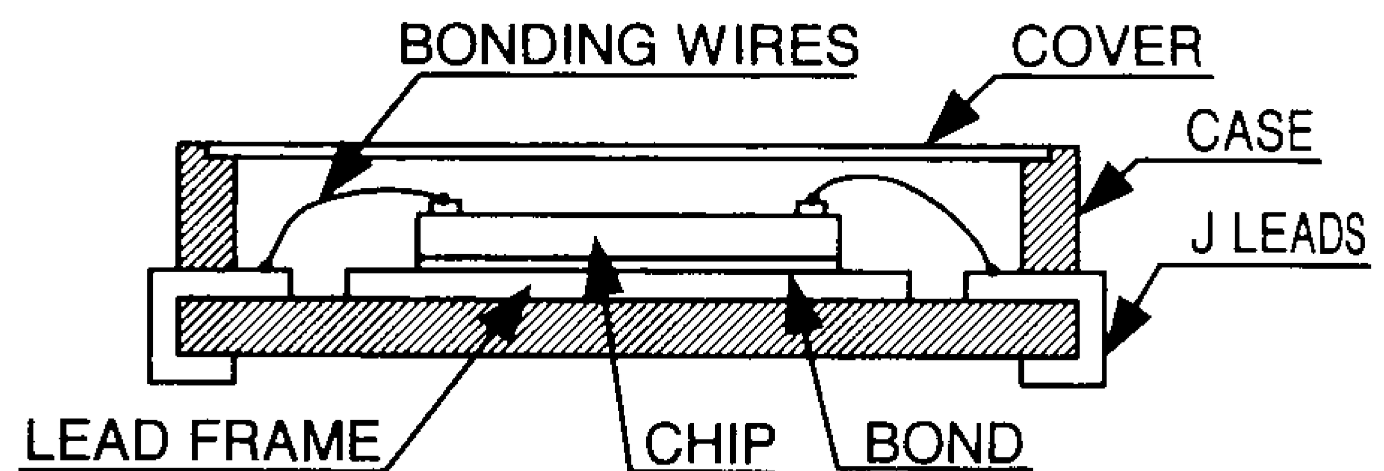

Fig. 4.2 Typical features of a traditional chip carrier with perimeter wiring connections.

Another design approach is illustrated schematically in Fig. 4.3, where the bonding pads on the chip are deployed over most of its area. In this design, the circuit surface of the chip is placed face down. The area deployed bonding pads on the chip are connected to a multilayer circuit board with controlled collapsible chip connections (C4) that are described later in this chapter. Area deployed connections to the printed circuit board (PCB) are made using more widely spaced solder balls. This type of a first level package is called a Ball-grid-array (BGA). The BGA involves more advanced manufacturing methods to produce the C4 connections and to successfully mount it onto the PCBs. However, the design can accommodate high I/O count. The BGA also has improved heat transfer characteristics because the back side of the chip is available for connection to a heat exchanger. In addition, the C4 connections are dense and provide a second path for heat flow.

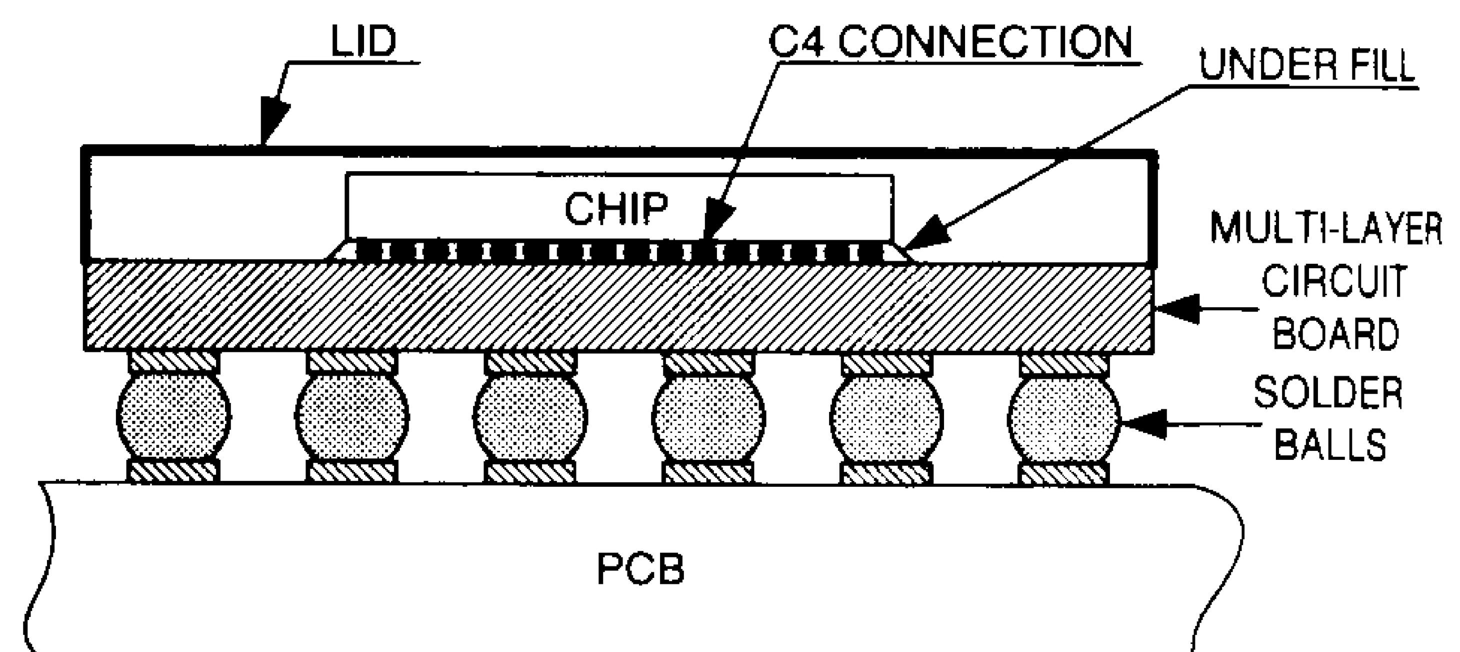

Fig. 4.3 Schematic illustration of the more advanced design for first level packaging.

Key design features for a chip carrier involve I/O count, package size (area and height), heat dissipation or thermal resistance, hermeticity and cost. I/O count is extremely important in housing modern Ultra Large Scale Integration (ULSI) chips which contain tens of millions of gates. Access to these gates through a high I/O count is required to fully utilize a high percentage of the capacity of the chip. These modern high-gate logic chips dissipate large quantities of heat and reliable operation of these dense chips requires that the chip carrier facilitate rather than impede the transfer of heat from the chip to a heat sink. Hermeticity is required to insure reliable operation of the chip over very long periods of time. Very small amounts of moisture which gain entry into the chip cavity of the carrier during assembly or by diffusion during operation permits corrosion of the metal wiring on the surface of the chip to occur. The presence of corrosion seriously degrades the chip circuits and reduces the life of the component. To eliminate the detrimental effects of moisture induced corrosion, some chip carriers are made of ceramic or glass-ceramic materials that prevent moisture entry by diffusion. Also, organic materials will outgas (release volatiles) with time; hence, they are prohibited within the chip cavity because the chemicals released when organics outgas can induce corrosion.

The common denominator of price and performance, typical of all of design philosophy for electronic systems, holds for chip carriers. Very low cost plastic chip carriers are available that are quite suitable for chips which dissipate low power, require modest I/O count to achieve maximum performance and do not require a high degree of hermeticity to insure suitable reliability for the product involved. However, for high performance systems operating at very high speed, the low cost plastic chip carrier is not adequate because it often does not have sufficient I/O count, its thermal resistance is much too high to handle the high power level required and its hermeticity is not sufficient to insure the degree of reliability required. At this time, significant research and development is underway to produce new chip carriers that are capable of housing modern high-speed, high-powered and high-I/O features found in the ultra-large-scale-integration (ULSI) chips which are currently under development.

4.2 TYPES OF CHIP CARRIERS

There are three general classifications used to describe chip carriers, which include:

1. Direct chip attachment to the printed circuit board
   - Chip and wire bonding
   - Flip-chip
2. Through-hole chip carriers
   - DIP
   - Pin-grid-array
3. Surface mount chip carriers
   - Leaded
   - Leadless
   - Ball-grid-arrays
   - Chip scale packages

Let's consider each of these classifications describing typical chip carriers that are currently employed.

4.2.1 Direct Die Attachment

Direct die attachment (DDA) sometimes called Chip-on-Board (CoB) or Wafer Level Packaging (WLP), involves an assembly process where the die is directly mounted on and electrically connected to the printed circuit board (PCB). The traditional first level package is eliminated. This process

simplifies the design and manufacturing of the product, and improves its performance because of the shorter interconnection paths that result due to direct attachment.

There are two methods commonly employed to attach a chip directly to a printed wiring board—direct die attach with wire bonding and flip-chip. Direct chip attachment with these bonding techniques is described in the next subsections.

Chip on Board with Wire Bonding

One approach followed in eliminating the first level package is the Chip-on-Board (COB) that is illustrated in Fig. 4.4. In this approach, the back side of the chip is bonded directly to the printed circuit board using an adhesive. After the adhesive has cured, wire bonding, described later in this chapter, is used to make the electrical connections from the perimeter chip bonding pads to the bonding pads on the circuit board. After the chip has been tested to insure it is functioning satisfactorily, the chip and bonding wires are encapsulated with a plastic glob. This approach is low in cost and is often employed on low end products that are disposable. One difficulty is the possibility of failure due to differences in the thermal expansion of the silicon chip and the printed circuit board. To mitigate the differences in these thermal expansions, a compliant adhesive is usually employed to bonds the chip to the board.

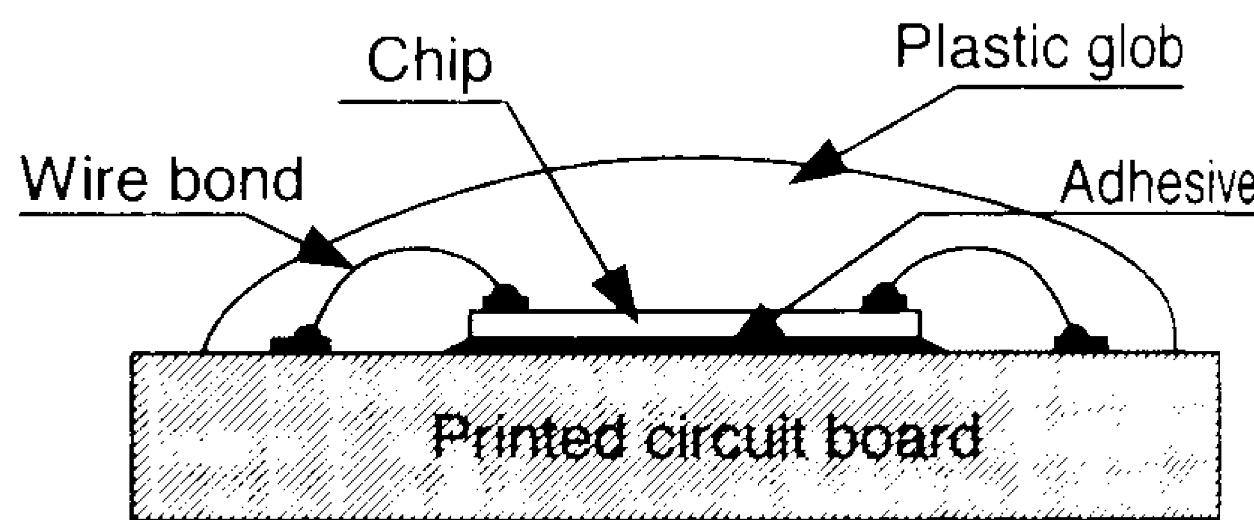

Fig. 4.4 Illustration of chip-on-board packaging that eliminates the first level chip carrier.

Flip-chip on-Board

Chips that have been processed with flip-chip bumps may be attached directly to a printed circuit board as illustrated in Fig. 4.5. The small solder balls on the back side of the chip produced by the bumping process (see Fig. 2.36) are placed over the corresponding bonding pads on the circuit board. The solder joint is made in a reflow oven that melts the solder balls forming joints that encase the solder pads. The solder mask prevents solder bridging. To mitigate the possibility of failure due to differences in the thermal expansion of the silicon chip and the printed circuit board, an underfill adhesive is placed between the chip and the board. The underfill adhesive is drawn into the small gap between the chip and the board by capillary action. After curing, the underfill adhesive also serves to seal the circuits from the environment. Hence it is not necessary to use an adhesive glob over the assembly. Because the solder bumping process enables the placement of solder balls on close centers over the entire area of the chip, higher I/O counts can be achieved than with the chip-on-board approach described above.

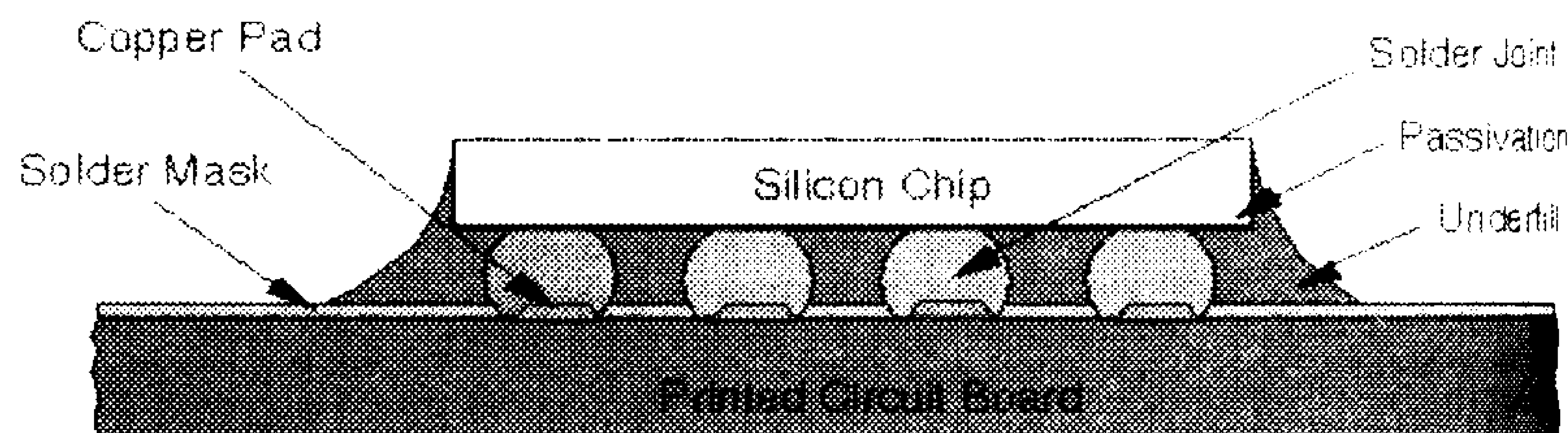

Fig. 4.5 Illustration showing the essential features used to eliminate the first level chip carrier by employing the flip-chip on-board approach.

The dies are prepared for direct attachment at the wafer level by forming small solder balls over the entire area of the chip. When the wafer fabrication process is complete, the wafers are re-passivated and a copper redistribution metal layer is patterned and sandwiched between layers of a low-dielectric

passivation material. Then the wafer bumping process, illustrated in Fig. 4.6, involves the placement of small solder bumps directly to the circuit area of the dies. These solder bumps (small balls) are utilized to make solder connections to the pads on the PCB.

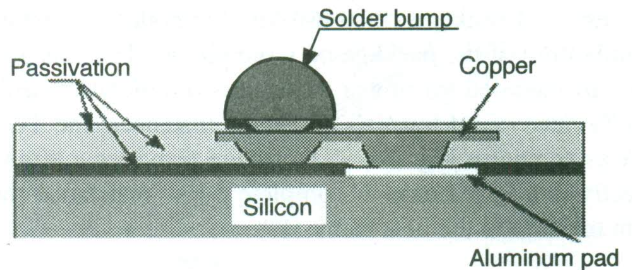

Fig. 4.6 Placement of a solder bump directly on a chip to facilitate direct attachment to a PCB.

Several different substrates are employed with direct die attachment. Ceramic and glass-ceramic substrates exhibit excellent dielectric and thermal properties. Organic substrates that weigh and cost less than the ceramic and glass-ceramic substrates are also used. These organic substrates have the advantage of lower dielectric constant. Flexible substrates that are pliable, have the ability to bend and support relatively dense circuits are used in some products.

The DDA process consists of only a few steps. For DDA with wire bonding, the chip is adhesively bonded to the PCB with its face up. The connections from the chip to the PCB are made with wire bonding. Then the die and wires are encapsulated with a plastic to protect it from the environment. For flip-chip bonding, solder bumps on the chip are aligned with the pads on the PCB and the mechanical and electrical connections are made by melting (reflowing) the solder bumps. If the PCB is made from an organic laminate, it is necessary to fill the small gap between the chip and the PCB. This process, known as underfilling, reduces the thermally induced shear strain on the solder bumps and extends the cyclic life of the product. The installation may be encapsulated to further protect the chip from mechanical and chemical damage.

4.2.2 Through-Hole Chip Carriers

The concept of through-hole chip carriers is illustrated in Fig. 4.7 where a cut away view of the chip carrier and circuit board is shown. With this approach the bonding pads on the chip are connected to leads that extend from the chip carrier. These leads are then inserted into plated-through-holes found on the circuit board. After insertion the leads are clinched and cut. The clenched leads hold the chip carriers in place on the PCB prior to soldering. The solder joints are made in a wave soldering process that is described in Chapter 6. The solder joints serve to mechanical fasten the chip carrier to the circuit board and to make the required electrical connections.

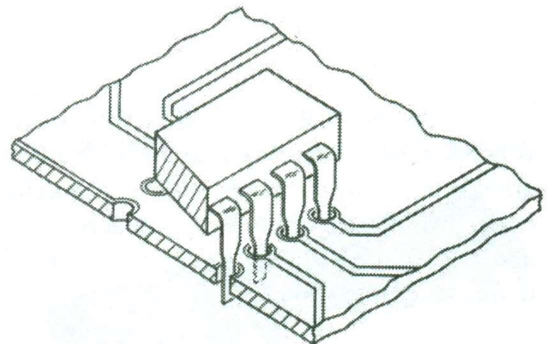

Fig. 4.7 Chip carriers with leads for through-hole mounting.