Zo: Transmission Lines, Reflections, and Termination

Nothing happens instantly, especially where digital circuits are concerned. In particular, consider the fact that the "speed-of-light" propagation delay of electrical signals in *wire* is on the order of 1.5–2 ns per foot (the exact delay depends on characteristics of the wire). When wire delays are similar to the transition times of the signals that they carry, we must treat wires not as zero-delay, perfect conductors, but as the "transmission lines" that they really are.

Transmission-line behavior includes signal changes that would not be predicted by a "DC" analysis of circuit operation. The most significant changes occur during an interval of approximately $2T$ after an output changes state, where T is the delay from the output to the far end of the wire that it drives.

Transmission-line behavior usually doesn't affect the logical operation of devices whose signal transition times and propagation delays are much longer than $2T$. Thus, transmission-line behavior typically is considered only for TTL, 74AC, and 74ACT connections over a foot, and for 74FCT and ECL connections over 3–6 inches. Naturally, you can sometimes get away with longer connections depending on the application, but there are also situations where transmission-line theory must be applied to even shorter connections. Many VLSI chips achieve high enough speeds that transmission-line behavior must be considered in the internal chip design.

Zo.1 Basic Transmission-Line Theory

Two conductors in parallel constitute the simplest *transmission line*. Consider a pair of conductors with infinite length, as shown in Figure Zo-1(a) on the next page. If we instantaneously put a voltage source across the pair, a certain current flows to create a voltage wave that travels along the pair. The ratio of voltage to current, V_{out}/I_{out}, depends on the physical characteristics of the conductors and is called the *characteristic impedance* Z_0 of the conductor pair. *transmission line*
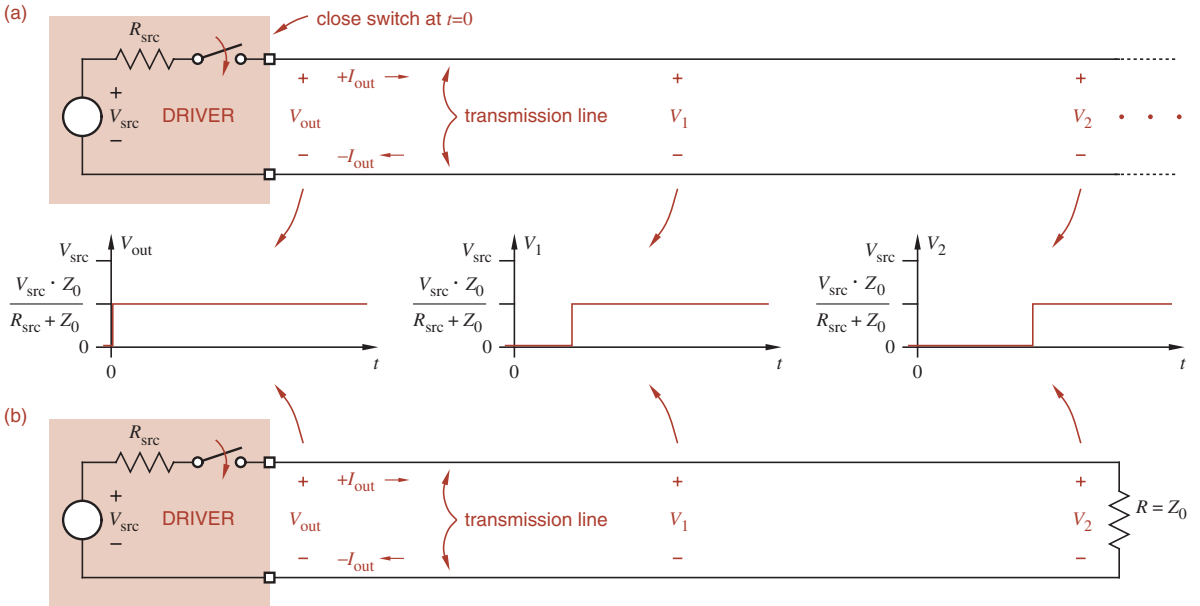
characteristic impedance Z_0

The magnitude of V_{out} is determined by viewing the series combination of R_{src} and Z_0 as a voltage divider, so that

$$V_{out} = V_{src} \cdot \frac{Z_0}{R_{src} + Z_0}$$

Of course, we don't have any infinitely long conductors. However, suppose that we have a 5-foot-long pair of conductors, and we place a resistance equal to Z_0 across the far end. If we instantaneously place a voltage source across the pair as shown in (b), the same current flows forever as in the infinite-length case. Thus, when a line is terminated by its characteristic impedance, we needn't consider transmission-line effects any further.

The situation is different for a transmission line of finite length that is not terminated in its characteristic impedance. An extreme case, in which the far end is short-circuited, is shown in Figure Zo-2(a). For simplicity, we assume that

Figure Zo-1 Transmission lines: (a) with infinite length; (b) with finite length, terminated with characteristic impedance.

$R_{src} = Z_0$ in this example. Initially, all the driver sees is the line's characteristic impedance, and a voltage wave with amplitude $V_{src}/2$ happily propagates down the line. However, when the wave hits the far end at time T, it sees the short-circuit. In order to satisfy Kirchhoff's laws, a voltage wave of the *opposite* polarity propagates back down the line, canceling the original wave. The far end has *reflected* the original wave, and the driver sees the short-circuit at time $2T$.   *reflection*

Another extreme case, in which the far end is open-circuited, is shown in (b). Everything starts out as before. However, when the initial voltage wave hits the far end, the current has nowhere to go, and so a voltage wave of the *same* polarity propagates back up the line, adding to the original voltage. When the reflected wave reaches the driver at time $2T$, the voltage everywhere is V_{src}, and nothing more happens.

In the general case, the amplitude of the wave reflected at the end of a transmission line is determined by the *reflection coefficient, ρ* (rho). The value   *reflection coefficient, ρ*
of ρ depends on Z_0 and Z_{term}, the *termination impedance* at the end of the line: *termination impedance*

$$\rho = \frac{Z_{term} - Z_0}{Z_{term} + Z_0}$$

When a voltage wave with amplitude V_{wave} hits the end of a transmission line, a wave with amplitude $\rho \cdot V_{wave}$ is reflected. Note that three simple cases match our previous discussion:
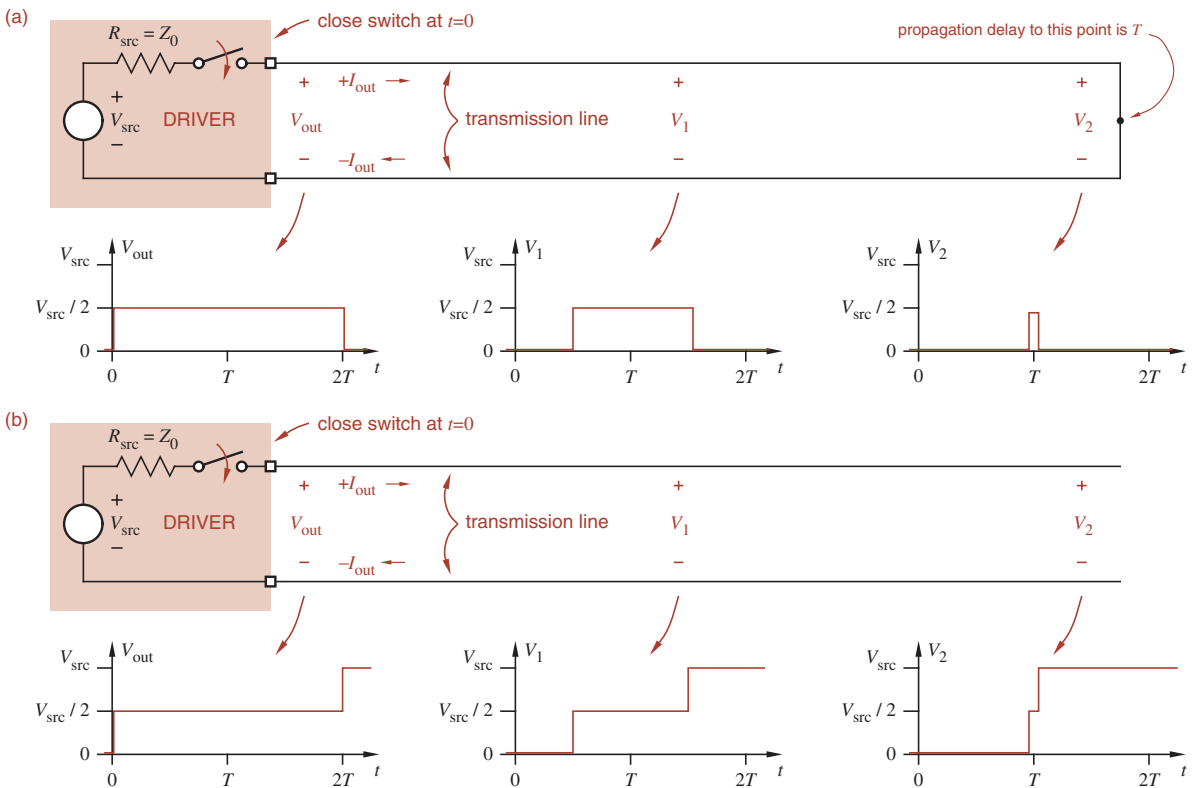
Figure Zo-2 Transmission lines: (a) short-circuited; (b) open-circuited.

$Z_{term} = Z_0$ When a transmission line is terminated in its characteristic imped-
ance, the reflection coefficient is 0.

$Z_{term} = 0$ The reflection coefficient of a short-circuited line is −1, producing a
reflection of equal magnitude and opposite polarity.

$Z_{term} = \infty$ The reflection coefficient of an open-circuited line is +1, producing a
reflection of equal magnitude and the same polarity.

If the source impedance (R_{src}) does not equal Z_0, then reflections occur at
the near end of the line as well as at the far end. Each end of the line has its own
value of ρ. The *principle of superposition* applies, so that voltage at any point on
the line and instant in time is the sum of that point's initial condition and all
waves that have passed it so far. The end of a transmission line is said to be
matched if it is terminated with its characteristic impedance.

principle of superposition

transmission-line matching

Figure Zo-3 on the next page shows the behavior of a transmission line that
is not matched at either end. (Note that the driver's ideal voltage source V_{src} is
considered to have a resistance of 0 Ω for this analysis.) Reflections occur at
both ends of the line, with smaller and smaller waves reflecting back and forth.
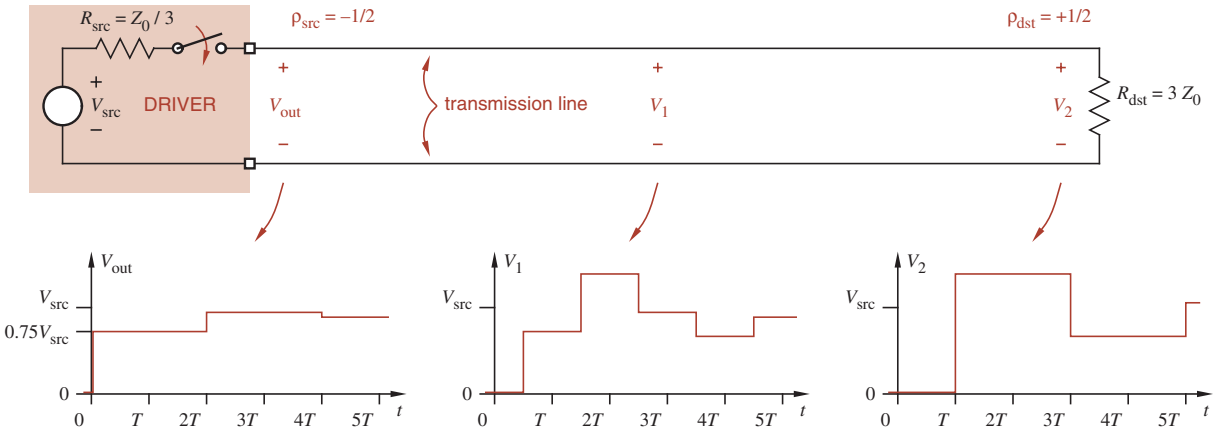
Figure Zo-3 A transmission line that is not matched at either end.

The voltage everywhere on the line asymptotically approaches $0.9V_{src}$, the value that would be predicted by a "DC" analysis of the circuit using Ohm's law.

Zo.2 Logic-Signal Interconnections as Transmission Lines

So, how does transmission-line theory affect logic signals? Let's consider the case of a 74HC CMOS output driving a CMOS input at the end of a transmission line consisting of a signal line and ground, as shown in Figure Zo-4. An "on" p-channel or n-channel output transistor in the HCT family has resistance of roughly 100–200 Ω; for simplicity let's assume 150 Ω in either the HIGH or the LOW state. The characteristic impedance of a typical PCB trace with respect to ground is on the order of 100–150 Ω; let's assume 150 Ω for convenience, so the reflection coefficient on the driving end of the line is 0. A typical CMOS input has an impedance over 1 MΩ, so the reflection coefficient on the receiving end is effectively +1.

Figure Zo-4 Reflections on a logic signal line changing from LOW to HIGH.
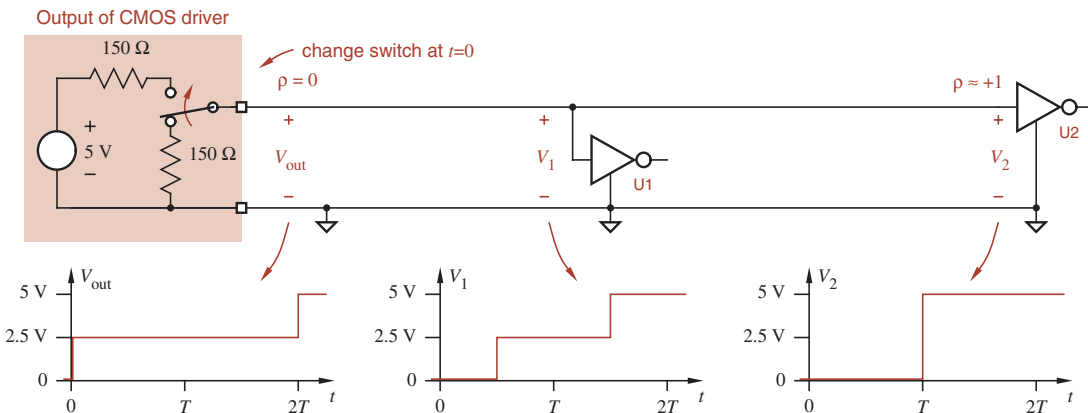
In the figure, we consider the case of a LOW-to-HIGH transition. When the CMOS driver switches from LOW to HIGH, the 5 V source in the driver sees the 150-Ω resistance of the driver in series with the 150-Ω Z_0 of the line, so a 2.5-V wave propagates down the line. After time T, this wave reaches the receiving gate U2 on the far end and is reflected. After time $2T$, the reflected wave reaches the sending end and is absorbed without a reflection, because $\rho = 0$ at that end.

Everything works fine as far as receiving gate U2 is concerned—it sees an instantaneous transition from 0 V to 5 V at time T after the driver switches. However, consider the waveform seen by another receiving gate U1 positioned halfway between the driver and U2. As shown in the figure, U1 sees an input of only 2.5 V for an interval T. A receiving gate positioned closer to the driver would see this input voltage even longer. This is a problem, because 2.5 V is right at the switching threshold for 5-V CMOS inputs. If this input voltage were maintained for long, U1's output could oscillate or produce a nonlogic voltage.

Any logic-signal connection, no matter how long or how short, is a transmission line. However, the foregoing analysis is quite idealized. In practice, transmission-line behavior causes no problem if T is somewhat shorter than the transition times of logic signals or the propagation delays of logic gates. In such a case, the reflections typically settle out before the receivers on the line have a chance to notice them.

A somewhat nastier case occurs when a high-performance output switches from HIGH to LOW. For example, as shown in Figure Zo-5 on the next page, in the LOW state an FCT CMOS output looks roughly like a 10-Ω resistor to ground. Thus, the reflection coefficient on the sending end is about −0.88. When the output is first switched LOW, it sees a voltage divider consisting of the 10-Ω resistor in series with the line impedance of 150 Ω. Since the line was originally at 5 V, the new voltage at the output of the divider must be

$$V_{out} = \frac{10\Omega}{150\Omega + 10\Omega} \cdot 5 \text{ V} = 0.31 \text{ V}$$

Therefore, a voltage wave $(0.31 - 5.0) = -4.69$ V is propagated down the line. When this wave hits the receiving end at time T, it produces a reflection of equal sign and magnitude (since $\rho = 1$). Thus, the voltage at the receiving end is now $V_2 = 5.0 - 4.69 - 4.69 = -4.38$ V, a negative voltage! This is called *undershoot*.   *undershoot*

When the −4.69 V reflection gets back to the sending end at time $2T$, yet another reflection occurs. This time, since ρ is negative, the reflected wave has a positive amplitude, $-0.88 \cdot -4.69 = +4.10$ V. The output voltage is now modified by the sum of the incoming reflection and the new outgoing reflection: $V_{out} = 0.31 - 4.49 + 4.10 = -0.08$ V. This is no problem. However, when the +4.10 V reflection reaches the receiving end at time $3T$, the ensuing positive reflection yields $V_2 = -4.38 + 4.10 + 4.10 = 3.82$ V, back to positive again!

As suggested by the figure, the reflections continue, with the voltage at both the sending and receiving ends asymptotically approaching 0 V, the value
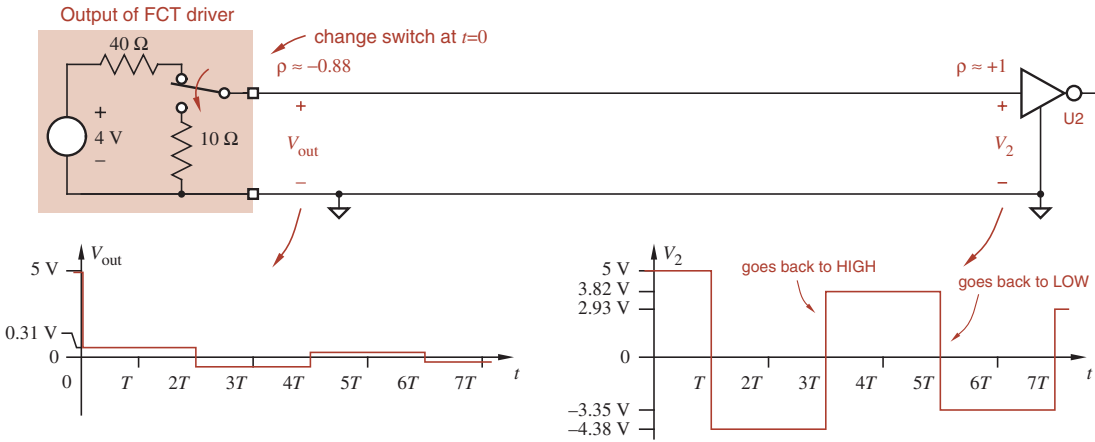
Figure Zo-5 Reflections on a logic signal line changing from HIGH to LOW.

one would predict with a "DC" analysis of the circuit. This oscillating pattern is called *ringing*.   *ringing*

The large magnitude of the ringing on the receiving end may be a problem, since V_2 does not settle to a range that is less than the LOW-state input voltage (0.8 V) until time $27T$. Thus, the effective propagation delay of the circuit has been increased by many times the wire delay. Worse, if the signal is a clock, extra edges will be detected on the ringing transitions, falsely clocking the flip-flops at the receiving end.

Once again, the transmission-line behavior that we've described causes no problems if T is much shorter than the transition times of logic signals or the propagation delays of logic gates. In addition, TTL and many CMOS input structures include *clamp diodes,* the normally reverse-biased diodes from each input to ground that we showed in Figure 3-71 on page 161. Since these diodes change the receiver's input impedance from very high to very low for negative voltages, they limit the negative excursion at time T to about 1 V. This reduces the reflection back to the sending end, which in turn reduces the excursion at time $3T$ to less than 1 V. The inputs of some devices also have diodes connected to V_{CC} to handle the overshoot that occurs when low-impedance drivers make a LOW-to-HIGH transition.   *clamp diodes*

Zo.3 Logic-Signal Terminations

Reflections can be eliminated by terminating transmission lines in their characteristic impedance. Two methods are commonly used.

In a *Thévenin termination*, a pair of resistors is placed at the end of the line as shown in Figure Zo-6(a). This termination has the Thévenin equivalent circuit shown in (b). Several factors are considered when choosing the resistor values: *Thévenin termination*
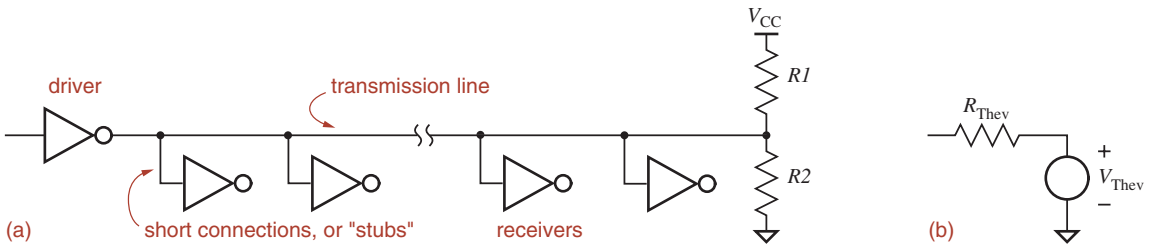
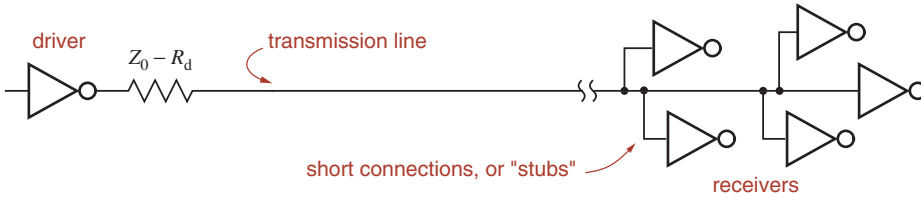**Figure Zo-6** Thévenin termination: (a) circuit; (b) equivalent circuit for termination.

1. The Thévenin equivalent resistance R_{Thev} should equal or be close to the line's characteristic impedance, Z_0. The Thévenin resistance is the parallel combination of $R1$ and $R2$, that is, $(R1 \cdot R2)/(R1 + R2)$.

2. The Thévenin equivalent voltage V_{Thev} may be chosen to optimize the current sinking and sourcing requirements of the driving gate. Here, V_{Thev} equals $V_{CC} \cdot R2/(R1 + R2)$.

   – For example, if the driving gate can source and sink equal amounts of current in the HIGH and LOW states (as in standard CMOS, not TTL compatible), then V_{Thev} can be halfway between V_{OL} and V_{OH}.

   – On the other hand, if the driving gate can sink more current than it can source (as in TTL and TTL-compatible CMOS), then a higher value of V_{Thev} is chosen to lessen the driver's current sourcing requirements in the HIGH state, at the expense of increasing its current sinking requirements in the LOW state.

3. For three-state buses, the Thévenin equivalent voltage V_{Thev} may be chosen to yield a valid logic level when the bus is not being driven. It is especially important in this case to choose a voltage that is not close to the switching threshold of the receivers, lest they draw excessive current or oscillate.

4. The final resistor values are chosen to match standard component values (e.g., 150, 220, 270, 330, 390, 470 ohms).

For example, a "standard" termination in some TTL applications has $R1 = 220\ \Omega$ and $R2 = 330\ \Omega$, yielding $R_{Thev} = 132\ \Omega$ and $V_{Thev} = 3.0$ V. In the LOW state, a driver must sink $(3.0\text{ V})/(132\ \Omega) = 22.7$ mA, and in the HIGH state, no current is needed to maintain a valid logic level.

　　With a well-matched Thévenin termination at the end of a transmission line, little or no reflection will occur. The downside of this termination is that it consumes DC power at all times, and relatively high driver currents are required.

　　A *source termination* (sometimes called a *series termination*) overcomes these problems. As shown in Figure Zo-7 on the next page, a resistance equal to Z_0 minus R_d, the typical output impedance of the driver, is placed in series with the output, physically close to the output itself.

source termination
series termination

Timing waveforms for a source termination are illustrated in Figure Zo-8. On a transition from V_{CC} to 0 (or vice versa), the driver sees a series resistance of $2Z_0$—the series resistor plus the line itself. Half of the voltage change is developed across the series resistor and the other half across the line itself. Thus, after a one-way transmission delay T, the far-end receiver U2 sees a voltage change of $V_{CC}/2$. Assuming a reflection coefficient of 1, this full value is immediately reflected back toward the driver, bringing the voltage at U2 all the way up to V_{CC}. When this reflection reaches the driver, it is absorbed in the matched series resistance Z_0, and the line is stable.

Source termination works well for drivers whose output impedances in the LOW and HIGH states are close to equal for practical purposes (e.g., CMOS). Typical designs use series resistors of 15–40 Ω for 50–100-Ω transmission lines.

Source termination is undesirable if any receiving gates, such as U1 in the figure, are positioned only partway down the transmission line. On a transition, these "middle" gates see an initial transition of only $V_{CC}/2$; they see the full transition only after the reflection from the far end goes by. Since $V_{CC}/2$ is likely to be near the switching threshold of the receiving gates, this is not a good place to be for very long. Therefore, source termination is normally used only when a PCB is physically laid out in a way similar to Figure Zo-7, with a relatively long line driving one load or a few that are clustered close together.

Figure Zo-8 Reflections on a source-terminated line changing from LOW to HIGH.
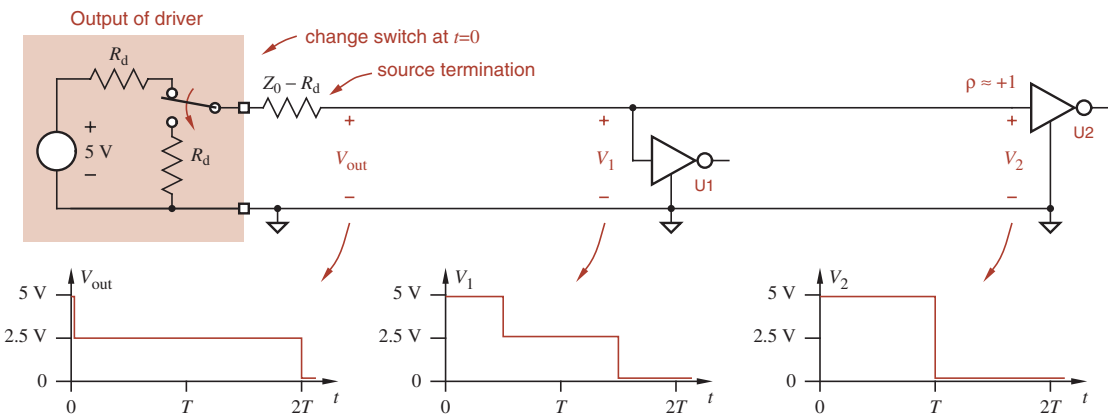
References

The basics and more about transmission lines, reflections, and terminations can be found in *High-Speed Digital Design: A Handbook of Black Magic*, by Howard Johnson and Martin Graham (Prentice Hall, 1993). This book combines solid electronics principles with tremendous insight and experience in the design of practical digital systems. Johnson's later companion book, *High-Speed Signal Propagation: Advanced Black Magic* (Prentice Hall, 2003), does a deep dive into transmission line theory and practice for circuits operating at the upper limit of what's possible.