Verification

System/Chip Design

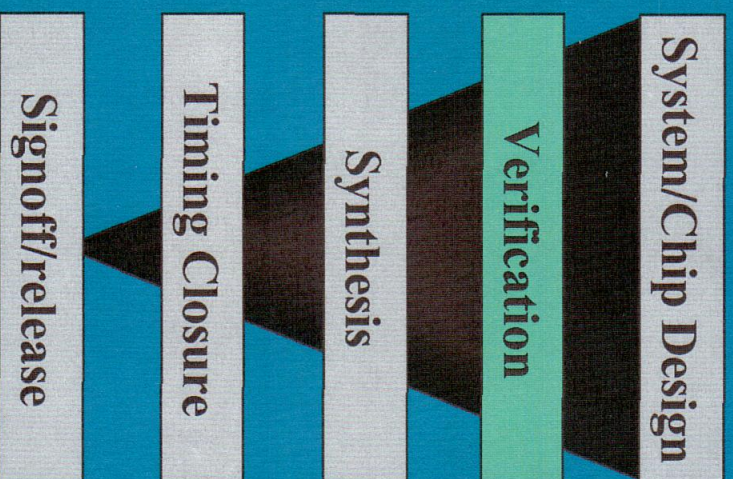**Verification**

Synthesis

Timing Closure

Signoff/release

✍ What is Verification?

Proof the design meets the _functional_ intent.

✍ What is timing closure?

Proof the design meets the timing restrictions.

✍ What is test?

Proof the design is manufactured without flaws.

EDA vendors claim 70% of design effort is now verification