ures

- OS for optimum speed/power
- h speed
- 25 ns (commercial)
- 30 ns (military)
- v power
- 495 mW (commercial)
- 660 mW (military)
- ROM technology 100% programmable
- n 300-mil or standard 600-mil DIP or 28-pin LCC
- ±10% V_{CC}, commercial and military
- -compatible I/O
- ect replacement for bipolar PROMs
- able of withstanding >2001V static discharge

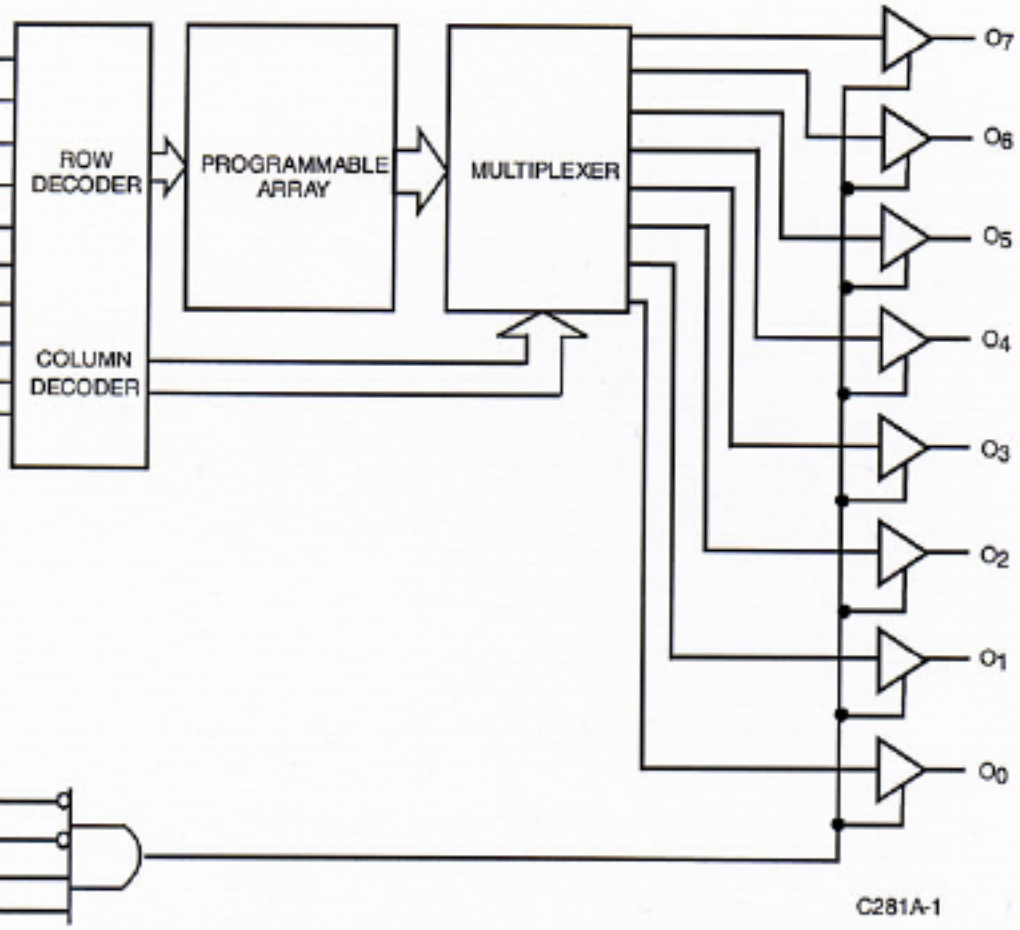
tional Description

CY7C281A and CY7C282A are high-performance word by 8-bit CMOS PROMs. They are functionally identical, but are packaged in 300-mil and 600-mil-wide pa respectively. The CY7C281A is also available in a 28-p less chip carrier. The memory cells utilize proven E floating-gate technology and byte-wide intelligent pr ming algorithms.

The CY7C281A and CY7C282A are plug-in replacem bipolar devices and offer the advantages of lower pow perior performance, and programming yield. The EPR requires only 12.5V for the super voltage, and low cur quirements allow for gang programming. The EPRO allow each memory location to be tested 100% becaus location is written into, erased, and repeatedly exercis to encapsulation. Each PROM is also tested for AC mance to guarantee that after customer programmi product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW si $\overline{CS}_1$ and $\overline{CS}_2$, and active HIGH signals on CS_3 and C contents of the memory location addressed by the a lines ($A_0 - A_9$) will become available on the output line O_7).

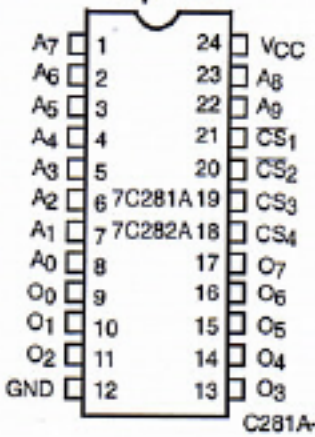
gicBlockDiagram



C281A-1

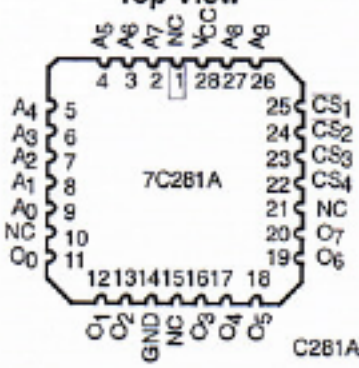
Pin Configurations

DIP
Top View



C281A-2

LCC/PLCC
Top View



C281A-3

tion Guide

	7C281A-25 7C282A-25	7C281A-30 7C282A-30	7C281A-45 7C282A-45
um Access Time (ns)	25	30	45