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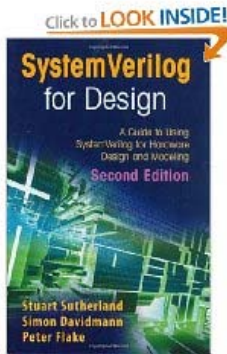
SystemVerilog for Design Second Edition: A Guide to Using SystemVerilog for Hardware Design and Modeling (Hardcover)

~ Stuart Sutherland (Author), Simon Davidmann (Author), Peter Flake (Author), P. Moorby (Foreword)

Key Phrases: case selection items, enum logic, unpacked arrays, Master State, Rdy Dtack, Design Example (more…)

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SystemVerilog is a rich set of extensions to the IEEE 1364-2001 Verilog Hardware Description Language (Verilog HDL). These extensions address two major aspects of HDL-based design. First, modeling very large designs with concise, accurate, and intuitive code. Second, writing high-level test programs to efficiently and effectively verify these large designs.

The first edition of this book addressed the first aspect of the SystemVerilog extensions to Verilog. Important modeling features were presented, such as two-state data types, enumerated types, user-degined types, structures, unions, and interfaces. Emphasis was placed on the proper usage of these enhancements for simulation and synthesis.

SystemVerilog for Design, Second Edition has been extensively revised on a chapter by chapter basis to include the many text and example updates needed to reflect changes that were made between the first edition of this book was written and the finalization of the new standard. It is important that the book reflect these syntax and semantic changes to the SystemVerilog language.

In addition, the second edition features a new chapter that explanis the SystemVerilog "packages", a new appendix that summarizes the synthesis guidelines presented throughout the book, and all of the code examples have been updated to the final syntax and rerun using the latest version of the Synopsys, Mentor, and Cadance tools.

Product Details

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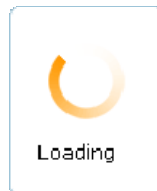
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4 of 4 people found the following review helpful:

Good book for experienced Verilog designers,
March 24, 2007

By **hummingbird lover**   (California) - See all my reviews

(My review is about the 2006 2nd-edition, not the older 1st edition!)

In general, I agree with the other reviews. This book is written for an audience of Verilog designers, who know the Verilog language (and its limitations) all to well. The book covers Systemverilog's new features like, enum, struct, interfaces, etc., from the perspective of "how to write better RTL-code using Systemverilog instead of Verilog.' For example, it explains the pros/cons of the (Systemverilog) "interface" construct, vs a flat group of (Verilog) module-port declarations. The discussion helps designers appreciate RTL-coding from a (slightly) higher levle of abstraction.

You don't need a specific background (i.e. design-engineer) to benefit from this book; you just need a good familiarity with conventional

Verilog.

As others have said, this book is not suitable as a reference. The paragraphs flow well, but it's hard to lookup an arbitrary topic from the index. So far, no hardcover-book can displace the official IEEE Systemverilog LRM as the best reference.

And since the book focuses on the 'design' (synthesizeable) aspect of Systemverilog, it doesn't cover non-synthesizeable language features (like classes, constrained random variables, etc.)

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As I make the transition to System Verilog, this book sits at my left hand, October 14, 2009

By **Gary "Tool Geek"**   (Rochester, MN United States) - See all my reviews

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I am using the book and getting value from it. the examples are not complete, but in a week I have scanned the book and had it open to review several times a day as I write and debug code.

On choosing which books to get to start with System Verilog: This one is focused on design, so has pointers on synthesizable descriptions and types. If you are doing verification you need both this and its companion, SystemVerilog for Verification: A Guide to Learning the Testbench Language Features by Chris Spear

You also need a verilog starter book, I may come back with an update on a recommendation.

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Great Book, October 11, 2009

By **C. Dearing**   (Dallas, TX) - See all my reviews

I use SystemVerilog for test bench coding. Nice to see a revised edition to correct and improve the original. This book is fantastic: good examples, well thought out. The topics flow well and are well written. Don't waste your time or money with any other SV book - this is it.

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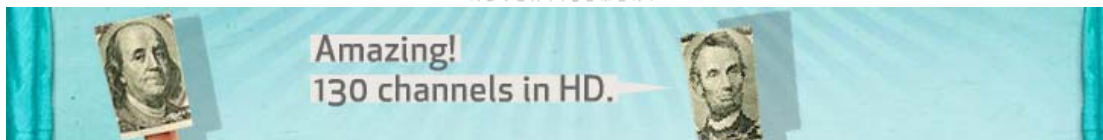
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