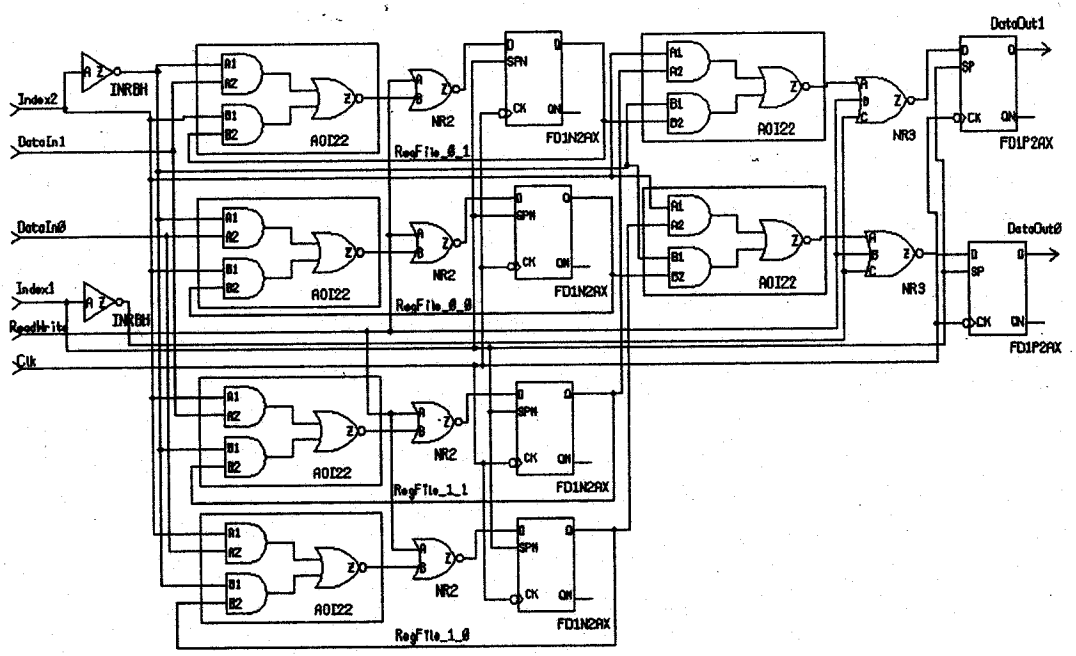
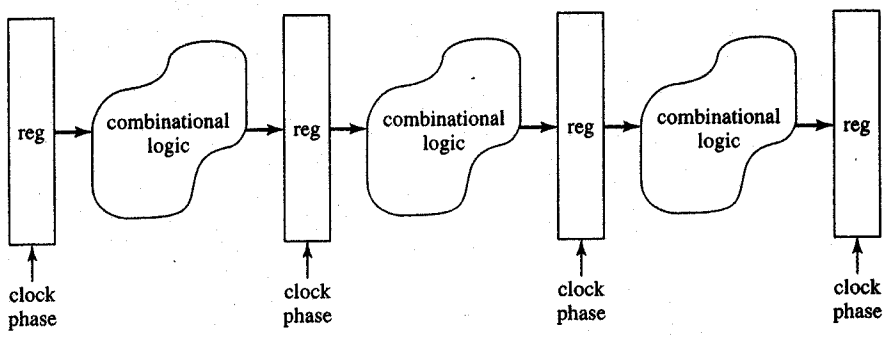
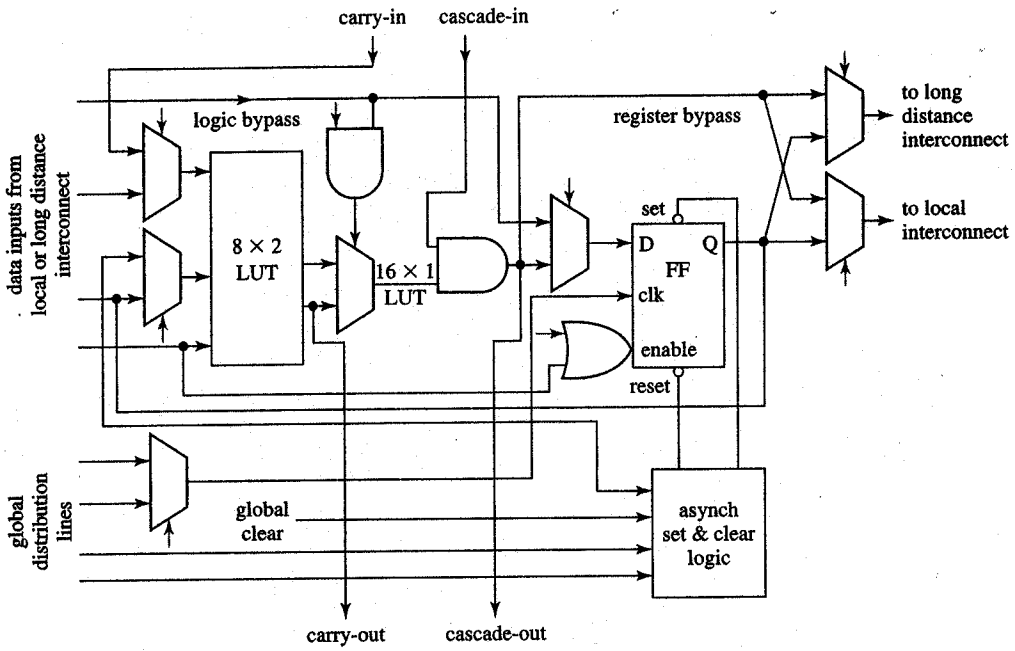


A 2-by-2 register file.



General Synchronous Design Paradigm.



Generic FPGA Logical Element (Simplified).

14-1/2

Table 14.1 *Xilinx Memory Primitives.*

Name	*Remarks*	*Augmented Ports*
RAM16X1		WE
RAM16X1D	dual port, synch write, asynch read	DPRA3,2,1,0,WCLK,WE
RAM16X1S	dual port, synch write, asynch read	WCLK
RAM32X1		A4
RAM32X1S	dual port, synch write, asynch read	A4, WCLK
ROM16X1	read only	
ROM32X1	read only	A4

```
module TPRX(clk, Din, raddr, waddr, we, Dout); //wrapper for synthesis to Xilinx LUT's
 input clk, we;
 input [3:0] raddr, waddr;
 input [7:0] Din;
 output [7:0] Dout;
 wire  [7:0] Dout, Din;
 // invoke 8 of the two port ram primitives from table 14 -1:
 RAM16X1D u0(.WCLK(clk),  .SPO(Din[0]), .WE(we), .DPO(Dout[0],
          .A0(waddr[0]),     .A1(waddr[1]),     .A2(waddr[2]),    .A3(waddr[3]),
        .DPRA0(raddr[0]), .DPRA1(raddr[1]), .DPRA2(raddr[2]), .DPRA3(raddr[3]) );
 RAM16X1D u1(.WCLK(clk),  .SPO(Din[1]), .WE(we), .DPO(Dout[1],
          .A0(waddr[0]),     .A1(waddr[1]),     .A2(waddr[2]),   .A3(waddr[3]),
       .DPRA0(raddr[0]), .DPRA1(raddr[1]), .DPRA2(raddr[2]), .DPRA3(raddr[3])  );
 RAM16X1D u2(.WCLK(clk),  .SPO(Din[2]), .WE(we), .DPO(Dout[2],
          .A0(waddr[0]),     .A1(waddr[1]),     .A2(waddr[2]),   .A3(waddr[3]),
       .DPRA0(raddr[0]), .DPRA1(raddr[1]),.DPRA2(raddr[2]),  .DPRA3(raddr[3]) );
 RAM16X1D u3(.WCLK(clk),  .SPO(Din[3]), .WE(we),  .DPO(Dout[3],
          .A0(waddr[0]),     .A1(waddr[1]),     .A2(waddr[2]),   .A3(waddr[3]),
        .DPRA0(raddr[0]), .DPRA1(raddr[1]),.DPRA2(raddr[2]), .DPRA3(raddr[3])  );
 RAM16X1D u4(.WCLK(clk),  .SPO(Din[4]), .WE(we),  .DPO(Dout[4],
          .A0(waddr[0]),     .A1(waddr[1]),     .A2(waddr[2]),   .A3(waddr[3]),
        .DPRA0(raddr[0]), .DPRA1(raddr[1]),.DPRA2(raddr[2]), .DPRA3(raddr[3]) );
 RAM16X1D u5(.WCLK(clk),  .SPO(Din[5]), .WE(we),  .DPO(Dout[5],
          .A0(waddr[0]),     .A1(waddr[1]),     .A2(waddr[2]),   .A3(waddr[3]),
        .DPRA0(raddr[0]), .DPRA1(raddr[1]),.DPRA2(raddr[2]), .DPRA3(raddr[3])  );
 RAM16X1D u6(.WCLK(clk),  .SPO(Din[6]), .WE(we),  .DPO(Dout[6],
          .A0(waddr[0]),     .A1(waddr[1]),     .A2(waddr[2]),   .A3(waddr[3]),
        .DPRA0(raddr[0]), .DPRA1(raddr[1]),.DPRA2(raddr[2]), .DPRA3(raddr[3])  );
 RAM16X1D u7(.WCLK(clk),  .SPO(Din[7]), .WE(we),  .DPO(Dout[7],
          .A0(waddr[0]),     .A1(waddr[1]),     .A2(waddr[2]),   .A3(waddr[3]),
        .DPRA0(raddr[0]), .DPRA1(raddr[1]),.DPRA2(raddr[2]), .DPRA3(raddr[3])  );
endmodule
```

Specification #2: RAM Wrapper for Xilinx.