ECE 172
(Winter 2023)

Instructor: Dr. Garrison Greenwood
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Office: FAB 20-12
Office hours: W 1230–1330

Prerequisites: ECE 171 (or equivalent)

Textbook: None required

Course Objectives: Students must demonstrate the ability to

- Obtain appropriate design information such as function, input and output voltage levels and propagation delays from logic device data sheets.
- Apply appropriate engineering techniques to design counter circuits from specified count sequences.
- Apply Karnaugh maps and implication tables to design both Moore and Mealy finite state machines.
- Describe how SRAM and DRAM devices are used to design memory systems
- Describe the architecture and capabilities of PLDs (PALs, GALs, FPGAs)
- State and illustrate how design-for-testability affects digital circuit designs

1. The course will be supplemented with material (datasheets, etc.) which will be posted on CANVAS. Supplemental material is testable.
2. You will take two 90 minute tests (15 pts each), have weekly homework assignments (25 pts total), labs (25 pts total) and take a comprehensive final exam (20 pts).
3. The grade scale is

   A $\rightarrow$ 92–100 pts A- $\rightarrow$ 90–92 pts

   B+ $\rightarrow$ 88–89 pts B $\rightarrow$ 83–87 pts B- $\rightarrow$ 80–82 pts

   C+ $\rightarrow$ 78–79 pts C $\rightarrow$ 73–77 pts C- $\rightarrow$ 70–72 pts

   D $\rightarrow$ 60-69 pts

   F $\rightarrow$ $<$ 60 pts

4. Notes:

   - No curve is used in determining grades.
   - There are no extra credit assignments of any kind.
   - Study guides for the tests will be posted on CANVAS.
   - Any form of cheating on tests or the final exam will not be tolerated. *If you cheat on an test, you get a score of zero on that test.* Character does matter.
   - The 90 minute tests are scheduled for 8 Feb and 8 Mar (both Wednesdays). The final exam is scheduled from 1230–1420 on Wed, 22 Mar
   - You cannot take the final exam (or any other test) prior to the date it is administered in class.
   - Homework is assigned each week on Wednesday and due the following week on Wednesday. All assignments will be posted on the CANVAS.
   - Copying homework is considered cheating. Copied homework receives a score of 0 points.
   - Do not submit homework via CANVAS. Homework must be turned in hardcopy, in class, on the date due.
   - Late homework is not accepted.
   - Any homework assignment turned in directly to the TA will automatically be classified as late. No exceptions.
   - Homework must be submitted on 8.5 x 11 inch paper. Homework submitted on any other size paper will not be graded.
   - Only the lecture CANVAS site is active; the lab CANVAS sites will not be used. Your labs will be posted on the CANVAS lecture site.
   - Labs are not necessarily held each week. An announcement will be made on the CANVAS if a lab session will be held during a given week.
   - Lab reports are to be turned directly to the TA (NOT me!). The due date will be indicated on the lab instructions.
   - CANVAS gives you access to various device datasheets and other literature that will be part of the lectures and will be testable. Be sure to check CANVAS frequently as new material is added from time to time.
   - Accommodations are collaborative efforts between students, faculty, and the Disability Resource Center. Students with accommodations approved through the DRC are responsible for contacting the faculty member in charge of the course prior to or during the first week of the term to discuss accommodations. Students who believe they are eligible for accommodations but who have not yet obtained approval through the DRC should contact the DRC immediately.

- If you are already registered with DRC for this class contact me via email as soon as possible so we can discuss your accommodations.
- Exams taken at the testing center must be scheduled on the same day the exam is administered in class and must be scheduled to overlap with the time the exam is administrated in class.