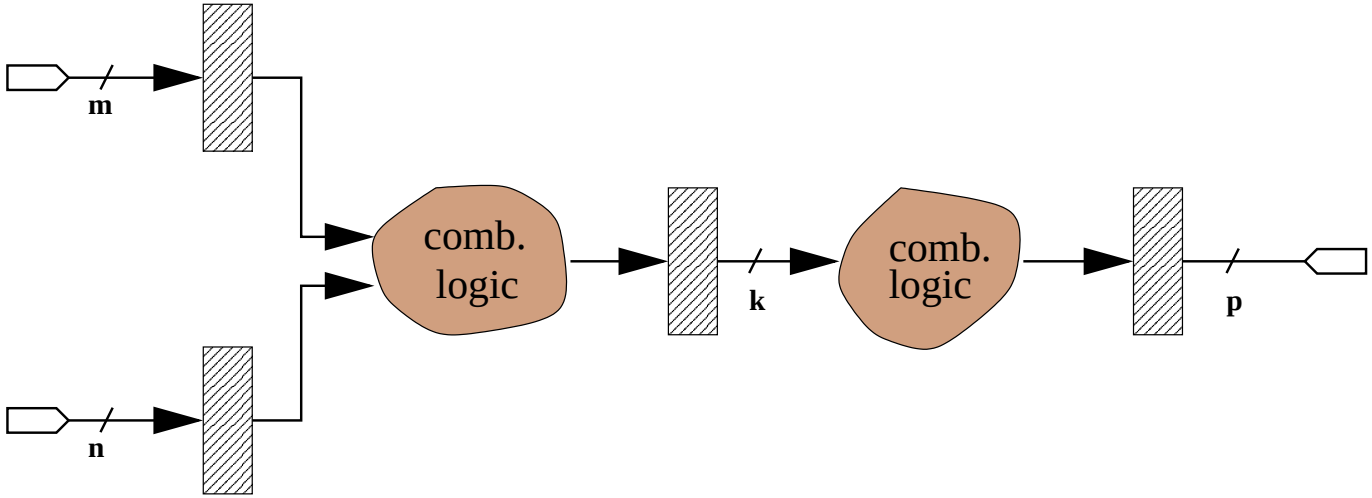
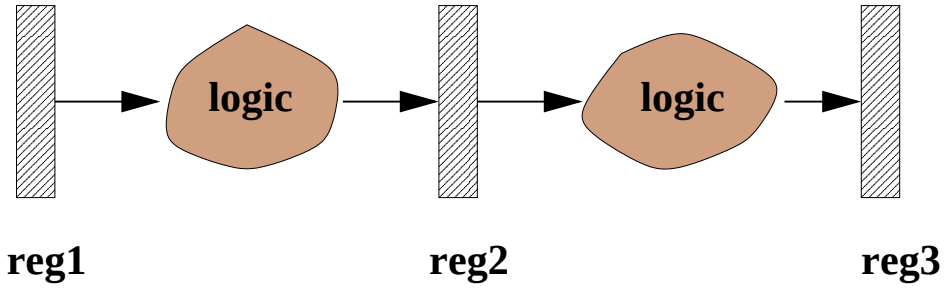
Definition of Register Transfer Level



- inputs & outputs defined
- registers serve as memory elements
- combinational logic between registers processes data
- circuit specified by operations and data transfers between registers
- defined timing (i.e., operations occur at specified times)

THE RTL MODEL



$$\mathbf{reg2} \leftarrow f_1(\mathbf{reg1})$$

$$\mathbf{reg3} \leftarrow f_2(\mathbf{reg2})$$

- combinational logic implements the functions
- RTL model shows data movements, but no details about the control structure*

* the control structure generates signals such as decoder enables or mux select line inputs