Port Connection Rules

One can visualize a port as consisting of two units, one unit that is *internal* to the module and another that is *external* to the module. The internal and external units are connected. There are rules governing port connections when modules are instantiated within other modules. The Verilog simulator complains if any port connection rules are violated. These rules are summarized in Figure 4-4.

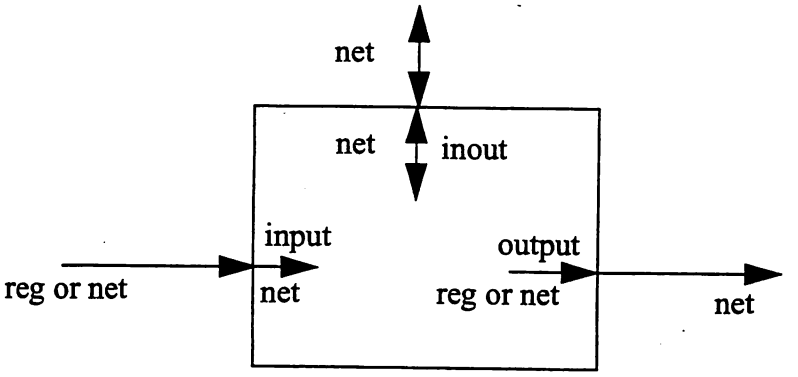

Figure 4-4 Port Connection Rules

Inputs

Internally, input ports must always be of the type *net*. Externally, the inputs can be connected to a variable which is a `reg` or a *net*.

Outputs

Internally, outputs ports can be of the type `reg` or *net*. Externally, outputs must always be connected to a *net*. They cannot be connected to a `reg`.

Inouts

Internally, inout ports must always be of the type *net*. Externally, inout ports must always be connected to a *net*.

Width matching

It is legal to connect internal and external items of different sizes when making inter-module port connections. However, a warning is typically issued that the widths do not match.