Signal pin-outs with respect to the FPGA.

Pin #	Type	Description	Pin #	Type	Description
B13	IO	GPIO 0	K15	I	DIP Switch, Switch #1 (Note 1)
A13	IO	GPIO 1	K16	I	DIP Switch, Switch #2 (Note 1)
B12	IO	GPIO 2	L15	I	DIP Switch, Switch #3 (Note 1)
A12	IO	GPIO 3	L16	I	DIP Switch, Switch #4 (Note 1)
B11	IO	GPIO 4	M15	I	DIP Switch, Switch #5 (Note 1)
A11	IO	GPIO 5	M16	I	DIP Switch, Switch #6 (Note 1)
B10	IO	GPIO 6	N15	I	DIP Switch, Switch #7 (Note 1)
A10	IO	GPIO 7	N16	I	DIP Switch, Switch #8 (Note 1)
B9	IO	GPIO 8			
A9	IO	GPIO 9	D16	O	LED 8
B8	IO	GPIO 10	D15	O	LED 7
A8	IO	GPIO 11	G15	O	LED 6
B7	IO	GPIO 12	E16	O	LED 5
A7	IO	GPIO 13	E15	O	LED 4
B6	IO	GPIO 14	G16	O	LED 3
A6	IO	GPIO 15	F14	O	LED 2
B5	IO	GPIO 16	F15	O	LED 1
A5	IO	GPIO 17			
B4	IO	GPIO 18	R4	O	7Seg #1 Segment A
A4	IO	GPIO 19	T5	O	7Seg #1 Segment B
C1	IO	GPIO 20	R5	O	7Seg #1 Segment C
C2	IO	GPIO 21	T6	O	7Seg #1 Segment D
D1	IO	GPIO 22	R6	O	7Seg #1 Segment E
D2	IO	GPIO 23	T7	O	7Seg #1 Segment F
E1	IO	GPIO 24	R7	O	7Seg #1 Segment G
E2	IO	GPIO 25	T8	O	7Seg #1 Segment DotPoint
F1	IO	GPIO 26			
F2	IO	GPIO 27	R8	O	7Seg #2 Segment A
G1	IO	GPIO 28	T9	O	7Seg #2 Segment B
G2	IO	GPIO 29	R9	O	7Seg #2 Segment C
H1	IO	GPIO 30	T10	O	7Seg #2 Segment D
H2	IO	GPIO 31	R10	O	7Seg #2 Segment E
			T11	O	7Seg #2 Segment F
T13	I	Reset	R11	O	7Seg #2 Segment G
G4	I	Clk (GCLK0, for PLL)			
H4	I	Ext_Clk (GCLK1, for PLL)	#T4	O	7Segment display enable (Note 3)
E4	I	Clk			
D3	I	Ext_Clk			

Type conventions:

I	Input
O	Output
IO	Input/Output

1) For revision 1.1 of the board, these pins are ACTIVE LOW. Rev 2.0 and newer, these pins are active high.

2) # at the pin name indicates an Active LOW signal.

3) This pin has been removed in revision 2.0 of the XFD351 development board.

Pin #		Description	Pin #		Description
J1	IO	Port1 IO0	N1	IO	Port 2 IO0
J2	I	Port1 CLK	N2	IO	Port 2 IO1
K1	IO	Port1 IO1	P1	IO	Port 2 IO2
K2	IO	Port1 IO2	P2	IO	Port 2 IO3
L1	IO	Port1 IO3	K3	IO	Port 2 IO4
L2	IO	Port1 IO4	K4	IO	Port 2 IO5
M1	IO	Port1 IO5	L3	IO	Port 2 IO6
M2	IO	Port1 IO6	L4	IO	Port 2 IO7

Connector Pin Designations: Bus Connector (JP4)					
Pin #		Description	Pin #		Description
1	P	+3.3v @ 400mA	21	IO	GPIO_12
2	P	+3.3v @ 400mA	22	IO	GPIO_13
3	GND	Ground/ref	23	IO	GPIO_14
4	GND	Ground/ref	24	IO	GPIO_15
5	Out	RST#	25	IO	GPIO_16
6	Out	CLK	26	IO	GPIO_17
7	Out	RST	27	IO	GPIO_18
8	Out	CLK_EXT	28	IO	GPIO_19
9	IO	GPIO_00	29	IO	GPIO_20
10	IO	GPIO_01	30	IO	GPIO_21
11	IO	GPIO_02	31	IO	GPIO_22
12	IO	GPIO_03	32	IO	GPIO_23
13	IO	GPIO_04	33	IO	GPIO_24
14	IO	GPIO_05	34	IO	GPIO_25
15	IO	GPIO_06	35	IO	GPIO_26
16	IO	GPIO_07	36	IO	GPIO_27
17	IO	GPIO_08	37	IO	GPIO_28
18	IO	GPIO_09	38	IO	GPIO_29
19	IO	GPIO_10	39	IO	GPIO_30
20	IO	GPIO_11	40	IO	GPIO_31

Type conventions:

P	Power (+3.3V)	GND	Ground
In	Input (+3.3v logic)	Out	Output (+3.3v logic)
IO	Input/Output		

1) For revision 1.1 of the board, these pins are ACTIVE LOW. Rev 2.0 and newer, these pins are active high.
2) # at the pin name indicates an Active LOW signal.
3) This pin has been removed in revision 2.0 of the XFD351 development board.