

List of the Standard Cells Distributed

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Cell Name	Function
buf_1	Noninverting buffer, drive strength 1
buf_2	Noninverting buffer, drive strength 2
buf_4	Noninverting buffer, drive strength 4
inv_1	Inverter, drive strength 1
inv_2	Inverter, drive strength 2
inv_4	Inverter, drive strength 4
and2_1	2-input AND gate, drive strength 1
and2_2	2-input AND gate, drive strength 2
and3_1	3-input AND gate, drive strength 1
and3_2	3-input AND gate, drive strength 2
or2_1	2-input OR gate, drive strength 1
or2_2	2-input OR gate, drive strength 2
or3_1	3-input OR gate, drive strength 1
or3_2	3-input OR gate, drive strength 2
nand2_1	2-input NAND gate, drive strength 1
nand2_2	2-input NAND gate, drive strength 2
nand3_1	3-input NAND gate, drive strength 1
nand3_2	3-input NAND gate, drive strength 2
nor2_1	2-input NOR gate, drive strength 1
nor2_2	2-input NOR gate, drive strength 2
nor3_1	3-input NOR gate, drive strength 1
nor3_2	3-input NOR gate, drive strength 2
xor2_2	2-input XOR gate, drive strength 2
mux2_2	2-to-1 multiplexer, drive strength 2
bufzp_2	noninverting tristate buffer, low-enabled, drive strength 2
invzp_1	inverting tristate buffer, low-enabled, drive strength 1
invzp_2	inverting tristate buffer, low-enabled, drive strength 2
cd_8	clock driver, drive strength 8
cd_12	clock driver, drive strength 12
cd_16	clock driver, drive strength 16
lp_2	high-active D latch, drive strength 2
lrp_2	high-active D latch with asynchronous low-active reset, drive strength 2
lrsp_2	high-active D latch with asynchronous low-active reset and asynchronous high-active set, drive strength 2
dp_2	rising-edge triggered D flip-flop, drive strength 2

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drp_2	rising-edge triggered D flip-flop with asynchronous low-active reset, drive strength 2
drsp_2	rising-edge triggered D flip-flop with asynchronous low-active reset and asynchronous high-active set, drive strength 2
filler	filler cell (empty cell with power and ground rails)