Synchronous FIFO Homework Problem

1 Preliminaries

Two computers must transfer data (see figure 1).

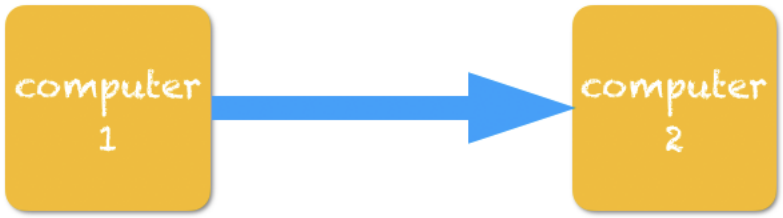

Figure 1:

Computer 1 sends the data at a rate computer 2 cannot accept. Figure 2 shows one possible solution: insert a first-in-first-out (FIFO) buffer between the two computers.

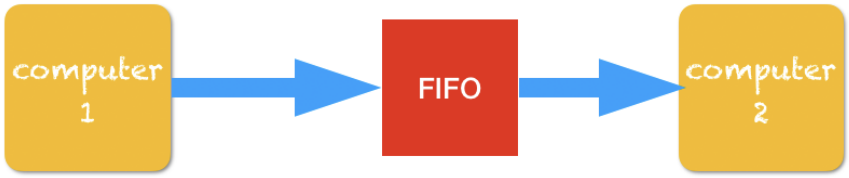

Figure 2:

The FIFO is a buffer with a depth and a width. The depth is the number of buffer (memory) locations and the width is the number of bits per location. The first data entering the FIFO buffer is the first data read from the FIFO buffer. (Computer 1 writes data into the FIFO; computer 2 reads data from the buffer.)

Figure 3 shows a block diagram of the FIFO. The data input (din) in bits is set by the FIFO width. The data output (dout) is the same width. . This

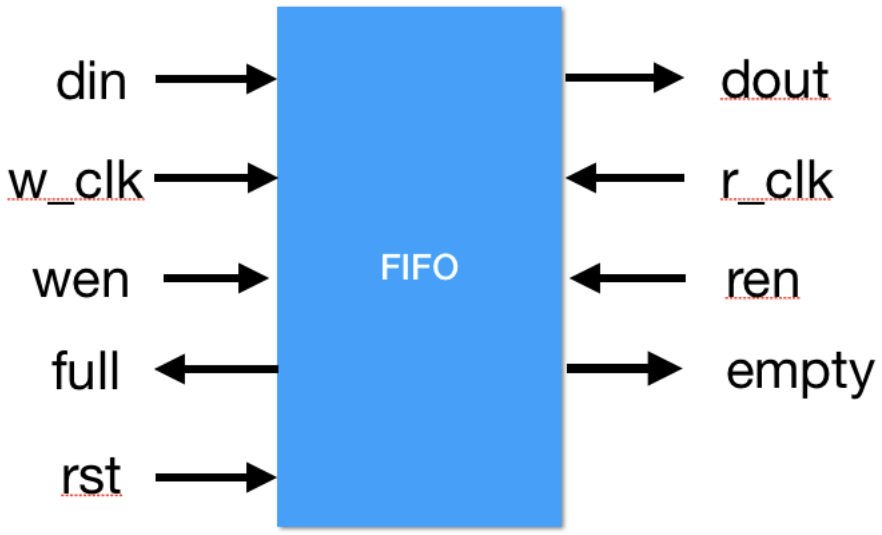

Figure 3:

FIFO is synchronous so the write clock (w_clk) and the read clock (r_clk) are the same clock signal. Data is put into the FIFO synchronously whenever the write enable (wen) is asserted. Similarly data is read synchronously from the FIFO whenever read enable (ren) is asserted. Clocks are positive edge triggered. The read and write enables are active high.

The FIFO depth equals the number buffer locations. Internally there are two k-bit pointers (w_ptr and r_ptr) where $k = \log_2(\text{depth})$. These pointers specify which buffer location is written to or read from. That is, w_ptr points to the location where the next data input will be stored while r_ptr which location data will be read from. The concept is shown in figure 4. After a write operation the w_ptr increments and the r_ptr increments after ever read operation. This is a circular buffer.

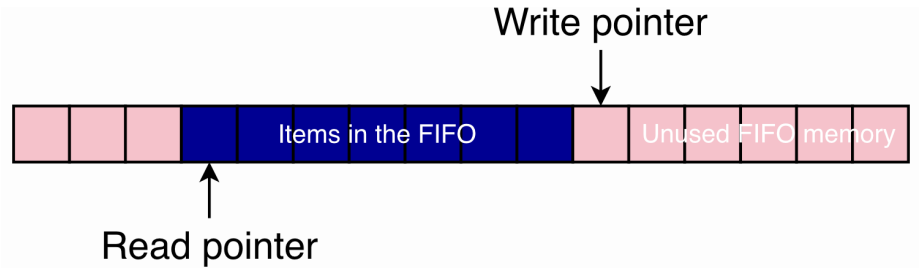

Figure 4:

Of course you should never write to a full FIFO or read from an empty FIFO. Two flags (status signals) are used. 'empty' indicates there is no data in the FIFO. This flag is read by computer 2 before beginning a read operation. 'full' indicates there are no available buffer locations left to store data. Computer 1 should check this flag before beginning a write operation. Both flags are active high.

The empty flag is asserted if w_ptr == r_ptr.

2 Assignment

You are to write a Verilog description of a synchronous FIFO with data width= 8. The FIFO has depth= 8.

You are also requireded to write a test bench to simulate your design. The test bench should perform the following tasks:

1. reset the FIFO and perform any required initialization
2. perform two write operations
3. perform one read operation
4. perform two write operations
5. perform two read operations
6. perform as many write operations as necessary to fill the FIFO
7. perform one read operation

The first write operation should store 00H, the second 55H, the third AAH and the fourth FFH. Repeat this sequence for any future write operations.

You then are to use QuestaSim and simulate your design using your testbench. Take a screenshot of the timing diagram. The timing diagram should show

- the reset signal
- the clock
- both read and write pointers
- both read and write enables
- data inputs
- data outputs
- the empty flag
- the full flag

Upload the timing diagram, the HDL description and the testbench to canvas