INFERENCE VS. INSTANTIATION

Hardware Inference

High-level RTL coding where the synthesis tool (Vivado) interprets behavioral intent and maps to physical logic blocks.

Hardware Instantiation

Directly referencing Xilinx primitives (e.g., RAMB36E1) in Verilog to achieve explicit control over silicon resources.

Strategic Choice

Balanced design requires choosing inference for portability and instantiation for peak performance/specialized features.

BEST PRACTICE METHODOLOGY

- **Start with Inference:** Always default to behavioral Verilog. Modern synthesis tools (Vivado) are highly sophisticated.
- **Validate via Reports:** Check the `Utilization Report` and `Timing Report` after synthesis to ensure the expected hardware was inferred.
- **Escalate to Instantiation:** Only move to direct instantiation if the tool fails to meet timing or if you require architecture-specific features (e.g., DSP Cascade).
- **Use Xilinx Macros:** Consider `XPM_MEMORY` as a middle ground for portable instantiation.

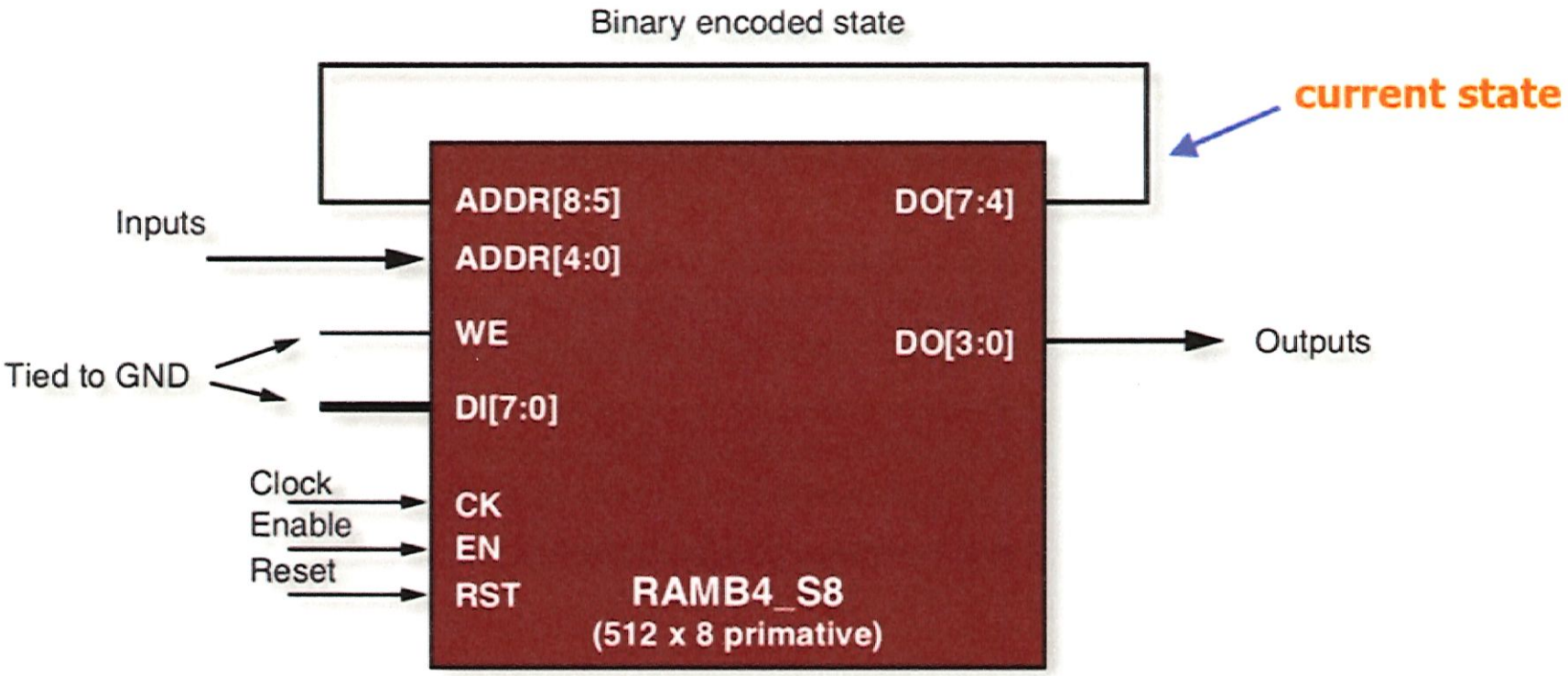
This shows using synthesizer attributes to force synthesis into hard IP

```
(* use_dsp = "yes" *)
module dsp_multiplier (
    input  wire                  clk,
    input  wire signed [17:0]    a,      // 18-bit signed input
    input  wire signed [24:0]    b,      // 25-bit signed input (native DSP size)
    output reg  signed [47:0]    p       // 48-bit full-precision output
);

    // Optional input registers (highly recommended for best DSP performance)
    reg signed [17:0] a_reg;
    reg signed [24:0] b_reg;

    always @(posedge clk) begin
        a_reg <= a;
        b_reg <= b;

        // Multiplication + optional accumulation/subtraction can map into one DSP48E2
        p <= a_reg * b_reg;          // Vivado will pack this into DSP48E2
    end

endmodule
```

```
// Only the multiplier is forced into a DSP slice
module partial_dsp_example (
    input  wire                 clk,
    input  wire signed [17:0]   a,       // 18-bit signed
    input  wire signed [17:0]   b,       // 18-bit signed
    input  wire signed [17:0]   c,       // another input for fabric logic
    output reg  signed [35:0]   product, // This signal will go into DSP
    output reg  signed [17:0]   sum      // This stays in fabric (LUTs)
);

    // Force ONLY this signal's operation into a DSP slice
    (* use_dsp = "yes" *) reg signed [35:0] dsp_product;

    // Optional pipeline registers (recommended for best DSP performance)
    reg signed [17:0] a_reg, b_reg;

    always @(posedge clk) begin
        a_reg <= a;
        b_reg <= b;

        // Multiplication forced into DSP48 slice via the attribute on the reg
        dsp_product <= a_reg * b_reg;     // <-- Only this uses DSP

        // The rest of the logic stays in normal fabric
        product <= dsp_product;           // registered output

        sum <= a_reg + b_reg + c;         // adder stays in LUTs + carry chain
    end

endmodule
```

Attribute	Target Resource	Common Values
ram_style	BRAM / URAM	"block", "distributed"
rom_style	ROM	"block", "distributed"
use_dsp	DSP48	"yes", "no"
shreg_extract	Shift registers	"yes", "no"

Table 1: Synthesis attributes for controlling hard block resources in Vivado. **shreg_extract** tells whether or not to implement in SRL.



Using fully synchronous RAM blocks for FSM implementation

```
module bram_fsm (clk, rst, in, out);
    input clk, rst, in;
    output reg out;

    // State Encoding using parameter statements
    parameter STATE_A = 2'b00, STATE_B = 2'b01, STATE_C =
2'b10;

    // Current state register
    reg [1:0] current_state;

    // BRAM Address layout: {current_state[1:0], in}
    wire [2:0] rom_addr;
    assign rom_addr = {current_state, in};

    // BRAM Data layout: {next_state[1:0], output_bit}
    reg [2:0] rom_data;

    // Synthesis attribute to force Block RAM implementation
    (* rom_style = "block" *) reg [2:0] fsm_rom [0:7];

    // Initialize the BRAM with the transition and output table
    initial begin
        // Address: {State, Input} -> Data: {Next State, Output}

        // State A (00), Output is 1
        fsm_rom[3'b000] = {STATE_A, 1'b1}; // in=0 -> stay at A
        fsm_rom[3'b001] = {STATE_B, 1'b1}; // in=1 -> go to B

        // State B (01), Output is 0
        fsm_rom[3'b010] = {STATE_A, 1'b0}; // in=0 -> go to A
        fsm_rom[3'b011] = {STATE_C, 1'b0}; // in=1 -> go to C

        // State C (10), Output is 1
        fsm_rom[3'b100] = {STATE_B, 1'b1}; // in=0 -> go to B
        fsm_rom[3'b101] = {STATE_A, 1'b1}; // in=1 -> go to A
```

```
        // Unused addresses (State 2'b11 / Don't cares)
        fsm_rom[3'b110] = {STATE_A, 1'b0};
        fsm_rom[3'b111] = {STATE_A, 1'b0};
    end

    // Synchronous BRAM read and State Update
    always @(posedge clk) begin
        if (rst) begin
            current_state <= STATE_A;
            out           <= 1'b1; // Initial state A output
        end else begin
            // Synchronous read required by BRAM blocks
            rom_data      <= fsm_rom[rom_addr];

            // Assign next state and output from the BRAM data word
            current_state <= rom_data[2:1];
            out           <= rom_data[0];
        end
    end

endmodule
```

7 Series FPGAs Data Sheet: Overview

DS180 (v2.6.1) September 8, 2020 **Product Specification**

General Description

Xilinx® 7 series FPGAs comprise four FPGA families that address the complete range of system requirements, ranging from low cost, small form factor, cost-sensitive, high-volume applications to ultra high-end connectivity bandwidth, logic capacity, and signal processing capability for the most demanding high-performance applications. The 7 series FPGAs include:

- Spartan®-7 Family: Optimized for low cost, lowest power, and high I/O performance. Available in low-cost, very small form-factor packaging for smallest PCB footprint.
- Artix®-7 Family: Optimized for low power applications requiring serial transceivers and high DSP and logic throughput. Provides the lowest total bill of materials cost for high-throughput, cost-sensitive applications.
- Kintex®-7 Family: Optimized for best price-performance with a 2X improvement compared to previous generation, enabling a new class of FPGAs.
- Virtex®-7 Family: Optimized for highest system performance and capacity with a 2X improvement in system performance. Highest capability devices enabled by stacked silicon interconnect (SSI) technology.

Built on a state-of-the-art, high-performance, low-power (HPL), 28 nm, high-k metal gate (HKMG) process technology, 7 series FPGAs enable an unparalleled increase in system performance with 2.9 Tb/s of I/O bandwidth, 2 million logic cell capacity, and 5.3 TMAC/s DSP, while consuming 50% less power than previous generation devices to offer a fully programmable alternative to ASSPs and ASICs.

Summary of 7 Series FPGA Features

- Advanced high-performance FPGA logic based on real 6-input look-up table (LUT) technology configurable as distributed memory.
- 36 Kb dual-port block RAM with built-in FIFO logic for on-chip data buffering.
- High-performance SelectIO™ technology with support for DDR3 interfaces up to 1,866 Mb/s.
- High-speed serial connectivity with built-in multi-gigabit transceivers from 600 Mb/s to max. rates of 6.6 Gb/s up to 28.05 Gb/s, offering a special low-power mode, optimized for chip-to-chip interfaces.
- A user configurable analog interface (XADC), incorporating dual 12-bit 1MSPS analog-to-digital converters with on-chip thermal and supply sensors.
- DSP slices with 25 x 18 multiplier, 48-bit accumulator, and pre-adder for high-performance filtering, including optimized symmetric coefficient filtering.
- Powerful clock management tiles (CMT), combining phase-locked loop (PLL) and mixed-mode clock manager (MMCM) blocks for high precision and low jitter.
- Quickly deploy embedded processing with MicroBlaze™ processor.
- Integrated block for PCI Express® (PCIe), for up to x8 Gen3 Endpoint and Root Port designs.
- Wide variety of configuration options, including support for commodity memories, 256-bit AES encryption with HMAC/SHA-256 authentication, and built-in SEU detection and correction.
- Low-cost, wire-bond, bare-die flip-chip, and high signal integrity flip-chip packaging offering easy migration between family members in the same package. All packages available in Pb-free and selected packages in Pb option.
- Designed for high performance and lowest power with 28 nm, HKMG, HPL process, 1.0V core voltage process technology and 0.9V core voltage option for even lower power.

Table 1: **7 Series Families Comparison**

Max. Capability	Spartan-7	Artix-7	Kintex-7	Virtex-7
Logic Cells	102K	215K	478K	1,955K
Block RAM(1)	4.2 Mb	13 Mb	34 Mb	68 Mb
DSP Slices	160	740	1,920	3,600
DSP Performance(2)	176 GMAC/s	929 GMAC/s	2,845 GMAC/s	5,335 GMAC/s
MicroBlaze CPU(3)	260 DMIPs	303 DMIPs	438 DMIPs	441 DMIPs
Transceivers	–	16	32	96
Transceiver Speed	–	6.6 Gb/s	12.5 Gb/s	28.05 Gb/s
Serial Bandwidth	–	211 Gb/s	800 Gb/s	2,784 Gb/s
PCIe Interface	–	x4 Gen2	x8 Gen2	x8 Gen3
Memory Interface	800 Mb/s	1,066 Mb/s	1,866 Mb/s	1,866 Mb/s
I/O Pins	400	500	500	1,200
I/O Voltage	1.2V–3.3V	1.2V–3.3V	1.2V–3.3V	1.2V–3.3V
Package Options	Low-Cost, Wire-Bond	Low-Cost, Wire-Bond, Bare-Die Flip-Chip	Bare-Die Flip-Chip and High-Performance Flip-Chip	Highest Performance Flip-Chip

Notes:

1. Additional memory available in the form of distributed RAM.
2. Peak DSP performance numbers are based on symmetrical filter implementation.
3. Peak MicroBlaze CPU performance numbers based on microcontroller preset.

Spartan-7 FPGA Feature Summary

Table 2: **Spartan-7 FPGA Feature Summary by Device**

Device	Logic Cells	CLB		DSP Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe	GT	XADC Blocks	Total I/O Banks[5]	Max User I/O
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7S6	6,000	938	70	10	10	5	180	2	0	0	0	2	100
XC7S15	12,800	2,000	150	20	20	10	360	2	0	0	0	2	100
XC7S25	23,360	3,650	313	80	90	45	1,620	3	0	0	1	3	150
XC7S50	52,160	8,150	600	120	150	75	2,700	5	0	0	1	5	250
XC7S75	76,800	12,000	832	140	180	90	3,240	8	0	0	1	8	400
XC7S100	102,400	16,000	1,100	160	240	120	4,320	8	0	0	1	8	400

Notes:

1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Does not include configuration Bank 0.

Table 3: **Spartan-7 FPGA Device-Package Combinations and Maximum I/Os**

Package	CPGA196	CSGA225	CSGA324	FTGB196	FGGA484	FGGA676
Size (mm)	8 x 8	13 x 13	15 x 15	15 x 15	23 x 23	27 x 27
Ball Pitch (mm)	0.5	0.8	0.8	1.0	1.0	1.0
Device	HR I/O[1]	HR I/O[1]	HR I/O[1]	HR I/O[1]	HR I/O[1]	HR I/O[1]
XC7S6	100	100		100		
XC7S15	100	100		100		
XC7S25		150	150	100		
XC7S50			210	100	250	
XC7S75					338	400
XC7S100					338	400

Notes:

1. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

Artix-7 FPGA Feature Summary

Table 4: **Artix-7 FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe[5]	GTPs	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7A12T	12,800	2,000	171	40	40	20	720	3	1	2	1	3	150
XC7A15T	16,640	2,600	200	45	50	25	900	5	1	4	1	5	250
XC7A25T	23,360	3,650	313	80	90	45	1,620	3	1	4	1	3	150
XC7A35T	33,280	5,200	400	90	100	50	1,800	5	1	4	1	5	250
XC7A50T	52,160	8,150	600	120	150	75	2,700	5	1	4	1	5	250
XC7A75T	75,520	11,800	892	180	210	105	3,780	6	1	8	1	6	300
XC7A100T	101,440	15,850	1,188	240	270	135	4,860	6	1	8	1	6	300
XC7A200T	215,360	33,650	2,888	740	730	365	13,140	10	1	16	1	10	500

Notes:
1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Artix-7 FPGA Interface Blocks for PCI Express support up to x4 Gen 2.
6. Does not include configuration Bank 0.
7. This number does not include GTP transceivers.

Table 5: **Artix-7 FPGA Device-Package Combinations and Maximum I/Os**

Package[1]	CPG236		CPG238		CSG324		CSG325		FTG256		SBG484		FGG484[2]		FBG484[2]		FGG676[3]		FBG676[3]		FFG1156	
Size (mm)	10 x 10		10 x 10		15 x 15		15 x 15		17 x 17		19 x 19		23 x 23		23 x 23		27 x 27		27 x 27		35 x 35	
Ball Pitch (mm)	0.5		0.5		0.8		0.8		1.0		0.8		1.0		1.0		1.0		1.0		1.0	
Device	GTP[4]	I/O HR[5]	GTP[4]	I/O HR[5]	GTP[4]	I/O HR[5]	GTP[4]	I/O HR[5]	GTP[4]	I/O HR[5]	GTP	I/O HR[5]	GTP[4]	I/O HR[5]	GTP	I/O HR[5]	GTP[4]	I/O HR[5]	GTP	I/O HR[5]	GTP	I/O HR[5]
XC7A12T			2	112			2	150														
XC7A15T	2	106			0	210	4	150	0	170			4	250								
XC7A25T			2	112			4	150														
XC7A35T	2	106			0	210	4	150	0	170			4	250								
XC7A50T	2	106			0	210	4	150	0	170			4	250								
XC7A75T					0	210			0	170			4	285			8	300				
XC7A100T					0	210			0	170			4	285			8	300				
XC7A200T											4	285			4	285			8	400	16	500

Notes:
1. All packages listed are Pb-free (SBG, FBG, FFG with exemption 15). Some packages are available in Pb option.
2. Devices in FGG484 and FBG484 are footprint compatible.
3. Devices in FGG676 and FBG676 are footprint compatible.
4. GTP transceivers in CP, CS, FT, and FG packages support data rates up to 6.25 Gb/s.
5. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

Kintex-7 FPGA Feature Summary

Table 6: **Kintex-7 FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe[5]	GTXs	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7K70T	65,600	10,250	838	240	270	135	4,860	6	1	8	1	6	300
XC7K160T	162,240	25,350	2,188	600	650	325	11,700	8	1	8	1	8	400
XC7K325T	326,080	50,950	4,000	840	890	445	16,020	10	1	16	1	10	500
XC7K355T	356,160	55,650	5,088	1,440	1,430	715	25,740	6	1	24	1	6	300
XC7K410T	406,720	63,550	5,663	1,540	1,590	795	28,620	10	1	16	1	10	500
XC7K420T	416,960	65,150	5,938	1,680	1,670	835	30,060	8	1	32	1	8	400
XC7K480T	477,760	74,650	6,788	1,920	1,910	955	34,380	8	1	32	1	8	400

Notes:
1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Kintex-7 FPGA Interface Blocks for PCI Express support up to x8 Gen 2.
6. Does not include configuration Bank 0.
7. This number does not include GTX transceivers.

Table 7: **Kintex-7 FPGA Device-Package Combinations and Maximum I/Os**

Package[1]	FBG484			FBG676[2]			FFG676[2]			FBG900[3]			FFG900[3]			FFG901			FFG1156		
Size (mm)	23 x 23			27 x 27			27 x 27			31 x 31			31 x 31			31 x 31			35 x 35		
Ball Pitch (mm)	1.0			1.0			1.0			1.0			1.0			1.0			1.0		
Device	GTX[4]	I/O		GTX[4]	I/O		GTX	I/O		GTX[4]	I/O		GTX	I/O		GTX	I/O		GTX	I/O	
		HR[5]	HP[6]		HR[5]	HP[6]		HR[5]	HP[6]		HR[5]	HP[6]		HR[5]	HP[6]		HR[5]	HP[6]		HR[5]	HP[6]
XC7K70T	4	185	100	8	200	100															
XC7K160T	4	185	100	8	250	150	8	250	150												
XC7K325T				8	250	150	8	250	150	16	350	150	16	350	150						
XC7K355T																24	300	0			
XC7K410T				8	250	150	8	250	150	16	350	150	16	350	150						
XC7K420T																28	380	0	32	400	0
XC7K480T																28	380	0	32	400	0

Notes:
1. All packages listed are Pb-free (FBG, FFG with exemption 15). Some packages are available in Pb option.
2. Devices in FBG676 and FFG676 are footprint compatible.
3. Devices in FBG900 and FFG900 are footprint compatible.
4. GTX transceivers in FB packages support the following maximum data rates: 10.3Gb/s in FBG484; 6.6Gb/s in FBG676 and FBG900. Refer to *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics* (DS182) for details.
5. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
6. HP = High-performance I/O with support for I/O voltage from 1.2V to 1.8V.

Virtex-7 FPGA Feature Summary

Table 8: **Virtex-7 FPGA Feature Summary**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe[5]	GTX	GTH	GTZ	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]	SLRs[8]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)									
XC7V585T	582,720	91,050	6,938	1,260	1,590	795	28,620	18	3	36	0	0	1	17	850	N/A
XC7V2000T	1,954,560	305,400	21,550	2,160	2,584	1,292	46,512	24	4	36	0	0	1	24	1,200	4
XC7VX330T	326,400	51,000	4,388	1,120	1,500	750	27,000	14	2	0	28	0	1	14	700	N/A
XC7VX415T	412,160	64,400	6,525	2,160	1,760	880	31,680	12	2	0	48	0	1	12	600	N/A
XC7VX485T	485,760	75,900	8,175	2,800	2,060	1,030	37,080	14	4	56	0	0	1	14	700	N/A
XC7VX550T	554,240	86,600	8,725	2,880	2,360	1,180	42,480	20	2	0	80	0	1	16	600	N/A
XC7VX690T	693,120	108,300	10,888	3,600	2,940	1,470	52,920	20	3	0	80	0	1	20	1,000	N/A
XC7VX980T	979,200	153,000	13,838	3,600	3,000	1,500	54,000	18	3	0	72	0	1	18	900	N/A
XC7VX1140T	1,139,200	178,000	17,700	3,360	3,760	1,880	67,680	24	4	0	96	0	1	22	1,100	4
XC7VH580T	580,480	90,700	8,850	1,680	1,880	940	33,840	12	2	0	48	8	1	12	600	2
XC7VH870T	876,160	136,900	13,275	2,520	2,820	1,410	50,760	18	3	0	72	16	1	6	300	3

Notes:

1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Virtex-7 T FPGA Interface Blocks for PCI Express support up to x8 Gen 2. Virtex-7 XT and Virtex-7 HT Interface Blocks for PCI Express support up to x8 Gen 3, with the exception of the XC7VX485T device, which supports x8 Gen 2.
6. Does not include configuration Bank 0.
7. This number does not include GTX, GTH, or GTZ transceivers.
8. Super logic regions (SLRs) are the constituent parts of FPGAs that use SSI technology. Virtex-7 HT devices use SSI technology to connect SLRs with 28.05 Gb/s transceivers.

Table 11: **Virtex-7 HT FPGA Device-Package Combinations and Maximum I/Os**

Package[1]	FLG1155			FLG1931			FLG1932		
Size (mm)	35 x 35			45 x 45			45 x 45		
Ball Pitch	1.0			1.0			1.0		
Device	GTH	GTZ	I/O HP[2]	GTH	GTZ	I/O HP[2]	GTH	GTZ	I/O HP[2]
XC7VH580T	24	8	400	48	8	600			
XC7VH870T							72	16	300

Notes:
1. All packages listed are Pb-free with exemption 15. Some packages are available in Pb option.
2. HP = High-performance I/O with support for I/O voltage from 1.2V to 1.8V.

Stacked Silicon Interconnect (SSI) Technology

There are many challenges associated with creating high capacity FPGAs that Xilinx addresses with the SSI technology. SSI technology enables multiple super logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders, to create a single FPGA with more than ten thousand inter-SLR connections, providing ultra-high bandwidth connectivity with low latency and low power consumption. There are two types of SLRs used in Virtex-7 FPGAs: a logic intensive SLR used in the Virtex-7 T devices and a DSP/block RAM/transceiver-rich SLR used in the Virtex-7 XT and HT devices. SSI technology enables the production of higher capability FPGAs than traditional manufacturing methods, enabling the highest capacity and highest performance FPGAs ever created to reach production more quickly and with less risk than would otherwise be possible. Thousands of super long line (SLL) routing resources and ultra-high performance clock lines that cross between the SLRs ensure that designs span seamlessly across these high-density programmable logic devices.

CLBs, Slices, and LUTs

Some key features of the CLB architecture include:

- Real 6-input look-up tables (LUTs)
- Memory capability within the LUT
- Register and shift register functionality

The LUTs in 7 series FPGAs can be configured as either one 6-input LUT (64-bit ROMs) with one output, or as two 5-input LUTs (32-bit ROMs) with separate outputs but common addresses or logic inputs. Each LUT output can optionally be registered in a flip-flop. Four such LUTs and their eight flip-flops as well as multiplexers and arithmetic carry logic form a slice, and two slices form a configurable logic block (CLB). Four of the eight flip-flops per slice (one per LUT) can optionally be configured as latches.

Between 25–50% of all slices can also use their LUTs as distributed 64-bit RAM or as 32-bit shift registers (SRL32) or as two SRL16s. Modern synthesis tools take advantage of these highly efficient logic, arithmetic, and memory features.

Clock Management

Some of the key highlights of the clock management architecture include:

- High-speed buffers and routing for low-skew clock distribution
- Frequency synthesis and phase shifting
- Low-jitter clock generation and jitter filtering

Each 7 series FPGA has up to 24 clock management tiles (CMTs), each consisting of one mixed-mode clock manager (MMCM) and one phase-locked loop (PLL).

Block RAM

Some of the key features of the block RAM include:

- Dual-port 36 Kb block RAM with port widths of up to 72
- Programmable FIFO logic
- Built-in optional error correction circuitry

Every 7 series FPGA has between 5 and 1,880 dual-port block RAMs, each storing 36 Kb. Each block RAM has two completely independent ports that share nothing but the stored data.

Synchronous Operation

Each memory access, read or write, is controlled by the clock. All inputs, data, address, clock enables, and write enables are registered. Nothing happens without a clock. The input address is always clocked, retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency.

During a write operation, the data output can reflect either the previously stored data, the newly written data, or can remain unchanged.

Programmable Data Width

Each port can be configured as 32K × 1, 16K × 2, 8K × 4, 4K × 9 (or 8), 2K × 18 (or 16), 1K × 36 (or 32), or 512 × 72 (or 64). The two ports can have different aspect ratios without any constraints.

Each block RAM can be divided into two completely independent 18 Kb block RAMs that can each be configured to any aspect ratio from 16K × 1 to 512 × 36. Everything described previously for the full 36 Kb block RAM also applies to each of the smaller 18 Kb block RAMs.

Only in simple dual-port (SDP) mode can data widths of greater than 18 bits (18 Kb RAM) or 36 bits (36 Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72.

Both sides of the dual-port 36 Kb RAM can be of variable width.

Two adjacent 36 Kb block RAMs can be configured as one cascaded 64K × 1 dual-port RAM without any additional logic.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, almost full, and almost empty. The almost full and almost empty flags are freely programmable. Similar to the block RAM, the FIFO width and depth are programmable, but the write and read ports always have identical width.

First word fall-through mode presents the first-written word on the data output even before the first read operation. After the first word has been read, there is no difference between this mode and the standard mode.

Digital Signal Processing — DSP Slice

Some highlights of the DSP functionality include:

- 25 x 18 two's complement multiplier/accumulator high-resolution (48 bit) signal processor
- Power saving pre-adder to optimize symmetrical filter applications
- Advanced features: optional pipelining, optional ALU, and dedicated buses for cascading

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All 7 series FPGAs have many dedicated, full custom, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 25 x 18 bit two's complement multiplier and a 48-bit accumulator, both capable of operating up to 741 MHz. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The DSP also includes a 48-bit-wide Pattern Detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

Input/Output

Some highlights of the input/output functionality include:

- High-performance SelectIO technology with support for 1,866 Mb/s DDR3
- High-frequency decoupling capacitors within the package for enhanced signal integrity
- Digitally Controlled Impedance that can be 3-stated for lowest power, high-speed I/O operation

The number of I/O pins varies depending on device and package size. Each I/O is configurable and can comply with a large number of I/O standards. With the exception of the supply pins and a few dedicated configuration pins, all other package pins have the same I/O capabilities, constrained only by certain banking rules. The I/O in 7 series FPGAs are classed as high range (HR) or high performance (HP). The HR I/Os offer the widest range of voltage support, from 1.2V to 3.3V. The HP I/Os are optimized for highest performance operation, from 1.2V to 1.8V.

HR and HP I/O pins in 7 series FPGAs are organized in banks, with 50 pins per bank. Each bank has one common V_{CCO} output supply, which also powers certain input buffers. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). There are two V_{REF} pins per bank (except configuration bank 0). A single bank can have only one V_{REF} voltage value.

Xilinx 7 series FPGAs use a variety of package types to suit the needs of the user, including small form factor wire-bond packages for lowest cost; conventional, high performance flip-chip packages; and bare-die flip-chip packages that balance smaller form factor with high performance. In the flip-chip packages, the silicon device is attached to the package substrate using a high-performance flip-chip process. Controlled ESR discrete decoupling capacitors are mounted on the package substrate to optimize signal integrity under simultaneous switching of outputs (SSO) conditions.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100Ω internal resistor. All 7 series devices support differential standards beyond LVDS: RSDS, BLVDS, differential SSTL, and differential HSTL.

Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended SSTL and differential SSTL. The SSTL I/O standard can support data rates of up to 1,866 Mb/s for DDR3 interfacing applications.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input and some outputs can be individually delayed by up to 32 increments of 78 ps, 52 ps, or 39 ps each. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O structure. Each I/O pin possesses an 8-bit IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 3, 4, 5, 6, 7, or 8 bits. By cascading two IOSERDES from two adjacent pins (default from differential I/O), wider width conversions of 10 and 14 bits can also be supported. The ISERDES has a special oversampling mode capable of asynchronous data recovery for applications like a 1.25 Gb/s LVDS I/O-based SGMII interface.

Low-Power Gigabit Transceivers

Some highlights of the Low-Power Gigabit Transceivers include:

- High-performance transceivers capable of up to 6.6 Gb/s (GTP), 12.5 Gb/s (GTX), 13.1 Gb/s (GTH), or 28.05 Gb/s (GTZ) line rates depending on the family, enabling the first single device for 400G implementations.
- Low-power mode optimized for chip-to-chip interfaces.
- Advanced Transmit pre and post emphasis, receiver linear equalization (CTLE), and decision feedback equalization (DFE) for long reach or backplane applications. Auto-adaption at receiver equalization and on-chip Eye Scan for easy serial link tuning.

Ultra-fast serial data transmission to optical modules, between ICs on the same PCB, over the backplane, or over longer distances is becoming increasingly popular and important to enable customer line cards to scale to 100 Gb/s and onwards to 400 Gb/s. It requires specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues at these high data rates.

The transceiver count in the 7 series FPGAs ranges from up to 16 transceiver circuits in the Artix-7 family, up to 32 transceiver circuits in the Kintex-7 family, and up to 96 transceiver circuits in the Virtex-7 family. Each serial transceiver is a combined transmitter and receiver. The various 7 series serial transceivers use either a combination of ring oscillators and

Encryption, Readback, and Partial Reconfiguration

In all 7 series FPGAs (except XC7S6 and XC7S15), the FPGA bitstream, which contains sensitive customer IP, can be protected with 256-bit AES encryption and HMAC/SHA-256 authentication to prevent unauthorized copying of the design. The FPGA performs decryption on the fly during configuration using an internally stored 256-bit key. This key can reside in battery-backed RAM or in nonvolatile eFUSE bits.

Most configuration data can be read back without affecting the system's operation. Typically, configuration is an all-or-nothing operation, but Xilinx 7 series FPGAs support partial reconfiguration. This is an extremely powerful and flexible feature that allows the user to change portions of the FPGA while other portions remain static. Users can time-slice these portions to fit more IP into smaller devices, saving cost and power. Where applicable in certain designs, partial reconfiguration can greatly improve the versatility of the FPGA.

XADC (Analog-to-Digital Converter)

Highlights of the XADC architecture include:

- Dual 12-bit 1 MSPS analog-to-digital converters (ADCs)
- Up to 17 flexible and user-configurable analog inputs
- On-chip or external reference option
- On-chip temperature (±4°C max error) and power supply (±1% max error) sensors
- Continuous JTAG access to ADC measurements

All Xilinx 7 series FPGAs (except XC7S6 and XC7S15) integrate a new flexible analog interface called XADC. When combined with the programmable logic capability of the 7 series FPGAs, the XADC can address a broad range of data acquisition and monitoring requirements. For more information, go to: http://www.xilinx.com/ams.

The XADC contains two 12-bit 1 MSPS ADCs with separate track and hold amplifiers, an on-chip analog multiplexer (up to 17 external analog input channels supported), and on-chip thermal and supply sensors. The two ADCs can be configured to simultaneously sample two external-input analog channels. The track and hold amplifiers support a range of analog input signal types, including unipolar, bipolar, and differential. The analog inputs can support signal bandwidths of at least 500 KHz at sample rates of 1MSPS. It is possible to support higher analog bandwidths using external analog multiplexer mode with the dedicated analog input (see UG480, 7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide).

The XADC optionally uses an on-chip reference circuit (±1%), thereby eliminating the need for any external active components for basic on-chip monitoring of temperature and power supply rails. To achieve the full 12-bit performance of the ADCs, an external 1.25V reference IC is recommended.

If the XADC is not instantiated in a design, then by default it digitizes the output of all on-chip sensors. The most recent measurement results (together with maximum and minimum readings) are stored in dedicated registers for access at any time via the JTAG interface. User-defined alarm thresholds can automatically indicate over-temperature events and unacceptable power supply variation. A user-specified limit (for example, 100°C) can be used to initiate an automatic powerdown.

The Spartan-7 FPGA ordering information is shown in Figure 1. Refer to the Package Marking section of UG475, *7 Series FPGAs Packaging and Pinout* for a more detailed explanation of the device markings.

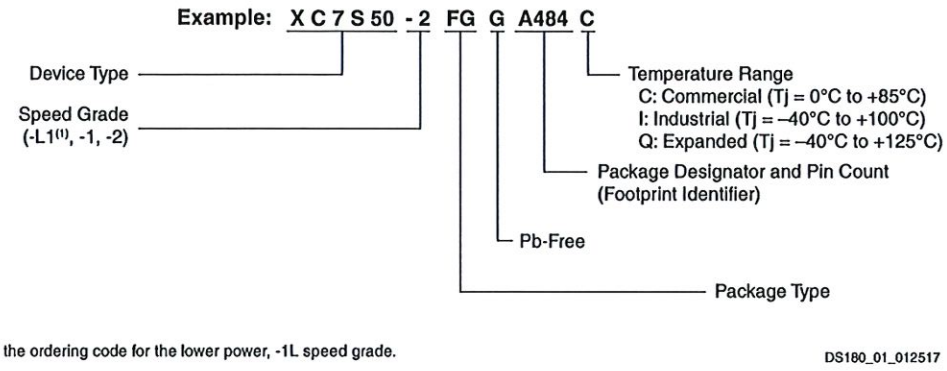


Figure 1: **Spartan-7 FPGA Ordering Information**

The Artix-7, Kintex-7, and Virtex-7 FPGA ordering information, shown in Figure 2, applies to all packages including Pb-Free. Refer to the Package Marking section of UG475, *7 Series FPGAs Packaging and Pinout* for a more detailed explanation of the device markings.

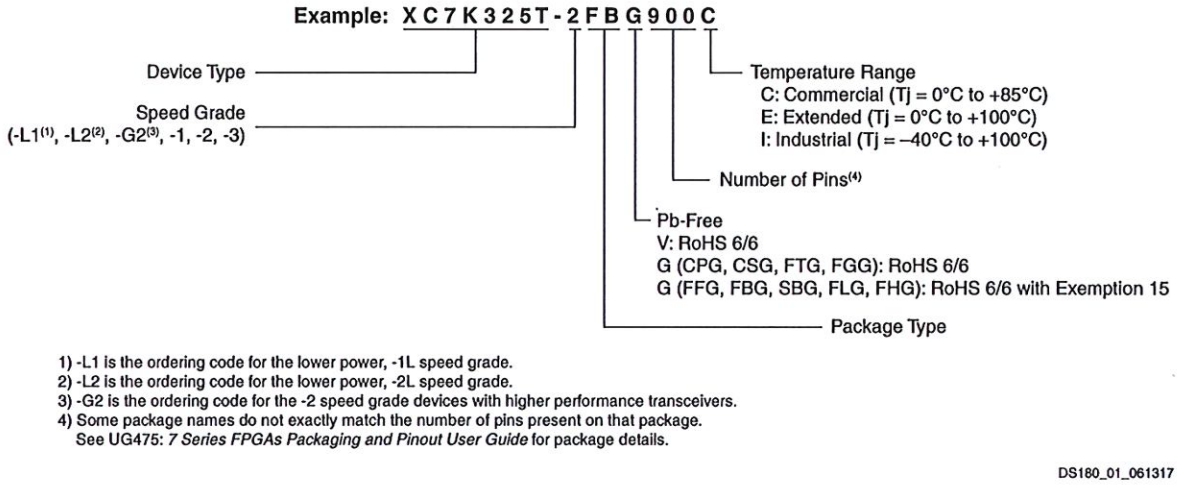
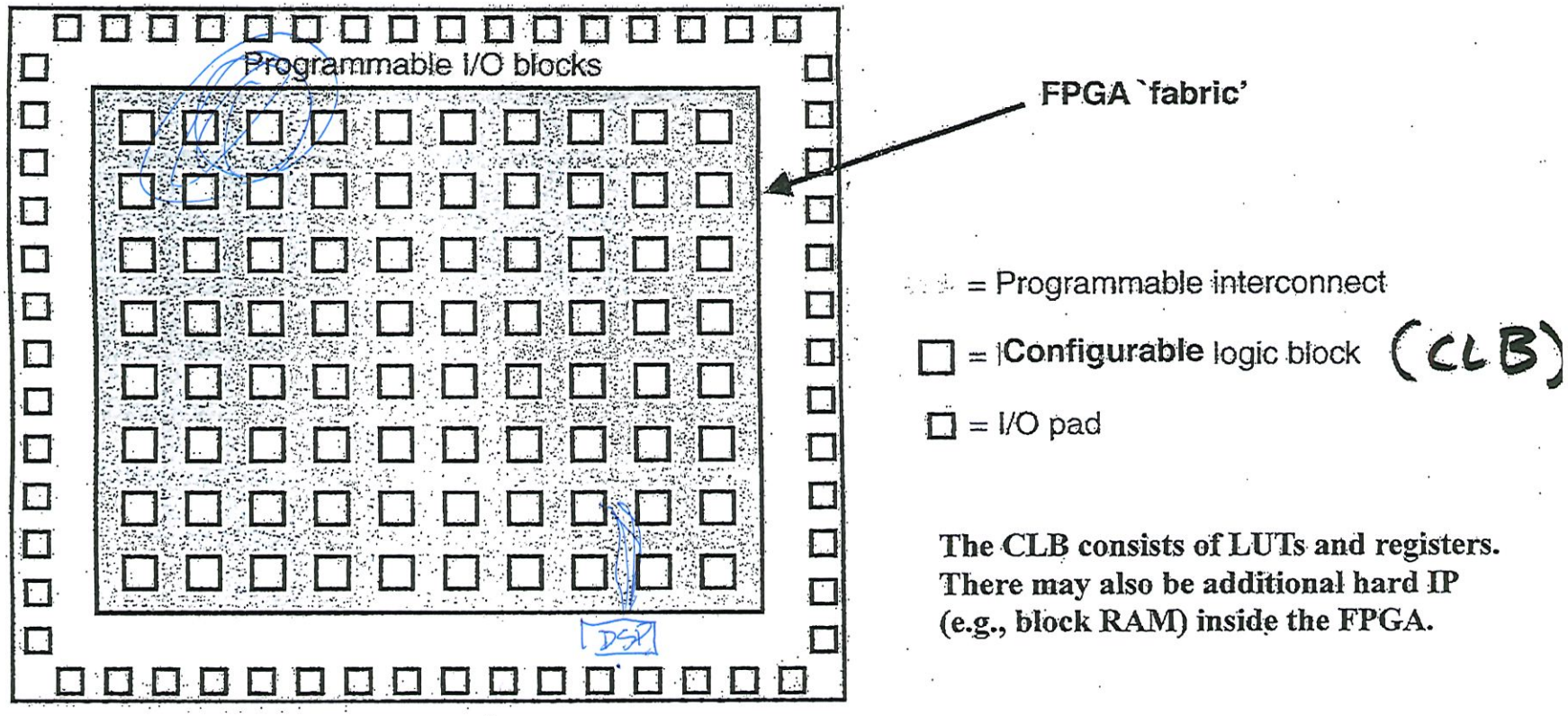


Figure 2: **Artix-7, Kintex-7, and Virtex-7 FPGA Ordering Information**

AMD

7 Series FPGAs Configurable Logic Block User Guide (UG474)



General FPGA chip architecture.

It is helpful to think of it this way: the **ASMBL architecture** is a 2D grid, but it is a **grid of columns** rather than a grid of individual, identical logic cells.

In a "traditional" FPGA (the way they were designed in the 90s), you might have one big repeating pattern where every logic block is surrounded by the same amount of routing and I/O. In the 7-series, AMD essentially "stacked" identical resources into vertical floor-to-ceiling strips.

How the "Grid" is Organized

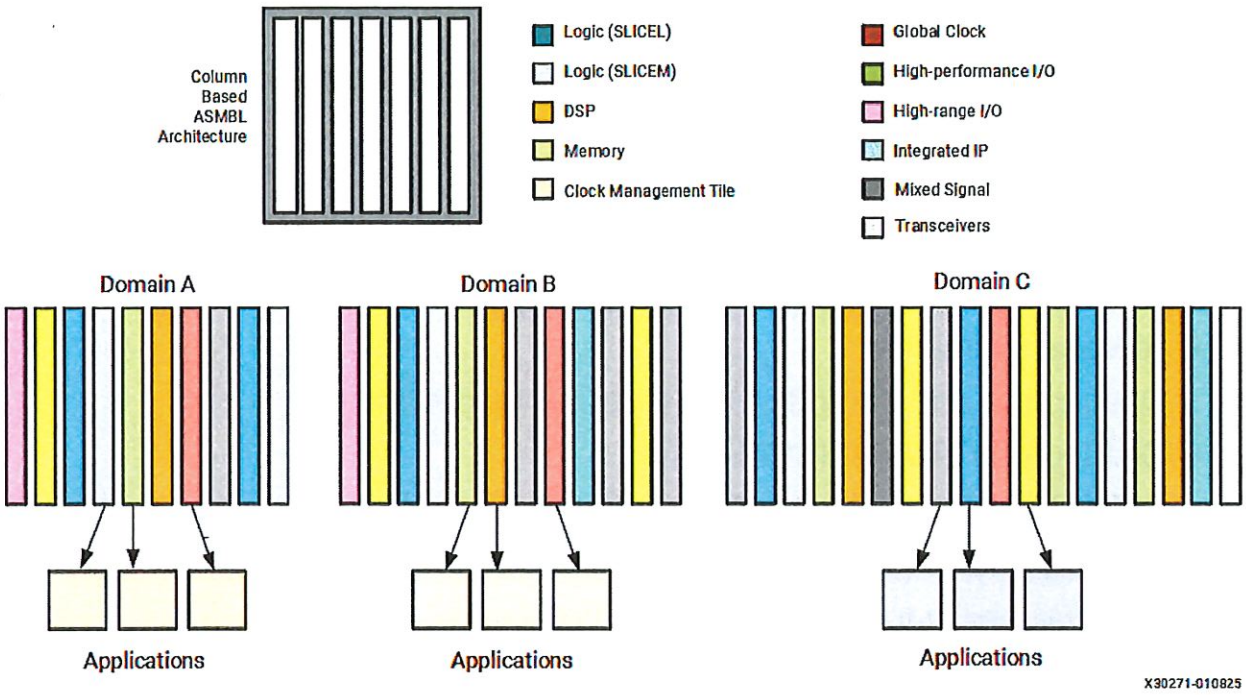
While you still have rows and columns, the **homogeneity** only exists vertically.

- **Vertically:** If you look at a single column of Configurable Logic Blocks (CLBs), it is uniform from top to bottom.
- **Horizontally:** As you move across the chip from left to right, the resources change. You might pass three columns of CLBs, then hit a column of Block RAM (BRAM), then a column of DSP slices, then more CLBs.

The Mix of Columns

Think of it as having a fixed set of "architectural LEGO strips." Every 7-series chip is built by picking from this same set of strips, but in different ratios:

- **Artix-7:** Primarily CLB columns with fewer DSP and BRAM columns. This is optimized for high-volume, low-power applications where you need general logic but aren't doing heavy number crunching.
- **Kintex-7:** A much higher density of DSP and BRAM columns relative to the logic. This is the "sweet spot" for signal processing, offering the best price-to-DSP ratio.
- **Virtex-7:** These are the largest chips, containing the most columns of every type. They often feature specialized columns for high-speed serial transceivers (GTX/GTH) and are frequently built using **Stacked Silicon Interconnect (SSI)**, which effectively tiles multiple die (Super Logic Regions) together to reach millions of logic cells.



The ASMBL architecture breaks through traditional design barriers by:

- Eliminating geometric layout constraints such as dependencies between I/O count and array size.
- Enhancing on-chip power and ground distribution by allowing power and ground to be placed anywhere on the chip.
- Allowing disparate integrated IP blocks to be scaled independent of each other and surrounding resources.

SSI Technology

The 7 series FPGAs extend integration even higher by using the unique stacked silicon interconnect (SSI) technology. SSI technology enables multiple super logic regions (SLRs) to be combined on a passive interposer layer, to create a single FPGA with more than ten thousand inter-SLR connections. See Advanced Topics for additional information.

CLB Slices

A CLB element contains a pair of slices, and each slice is composed of four 6-input LUTs and eight storage elements.