LatticeXP2 Family Data Sheet Introduction

May 2007 **Advance Data Sheet DS1009**

Features

- **flexiFLASH™ Architecture**
  - Instant-on
  - Infinitely reconfigurable
  - Single chip
  - FlashBAK™ technology
  - Serial TAG memory
  - Design security
- **Live Update Technology**
  - TransFR™ technology
  - Secure updates with 128 bit AES encryption
  - Dual-boot with external SPI
- **sysDSP™ Block**
  - Three to eight blocks for high performance Multiply and Accumulate
  - 12 to 32 18x18 multipliers
  - Each block supports one 36x36 multiplier or four 18x18 or eight 9x9 multipliers
- **Embedded and Distributed Memory**
  - Up to 885 Kbits sysMEM™ EBR
  - Up to 83 Kbits Distributed RAM
- **Flexible I/O Buffer**
  - sysIO™ buffer supports:
    - LVCMOS 33/25/18/15/12; LVTTL
    - SSTL 33/25/18 class I, II
    - HSTL15 class I; HSTL18 class I, II
    - PCI
    - LVDS, Bus-LVDS, MLVDS, LVPECL, RSDS
- **Pre-engineered Source Synchronous Interfaces**
  - DDR / DDR2 interfaces up to 200 MHz
  - 7:1 LVDS interfaces support display applications
  - XGMII
- **sysCLOCK™ PLLs**
  - Up to four analog PLLs per device
  - Clock multiply, divide and phase shifting
- **Density And Package Options**
  - 5k to 40k LUT4s, 86 to 540 I/Os
  - csBGA, TQFP, QFP, ftBGA and fpBGA packages
  - Density migration supported
- **Flexible Device Configuration**
  - SPI (master and slave) Boot Flash Interface
  - Dual Boot Image supported
  - Soft Error Detect (SED) macro embedded
- **System Level Support**
  - IEEE 1149.1 and IEEE 1532 Compliant
  - On-chip oscillator for initialization & general use
  - Devices operate with 1.2V power supply

Table 1-1. LatticeXP2 Family Selection Guide

Device	XP2-5	XP2-8	XP2-17	XP2-30	XP2-40
LUTs (K)	5	8	17	29	40
Distributed RAM (KBits)	10	18	35	56	83
EBR SRAM (KBits)	166	221	276	387	885
EBR SRAM Blocks	9	12	15	21	48
sysDSP Blocks	3	4	5	7	8
18 x 18 Multipliers	12	16	20	28	32
V_{CC} Voltage	1.2	1.2	1.2	1.2	1.2
GPLL	2	2	4	4	4
Max Available I/O	172	201	358	472	540
Packages and I/O Combinations					
132-Ball csBGA (8 x 8 mm)	86	86			
144-Pin TQFP (20 x 20 mm)	100	100			
208-Pin PQFP (28 x 28 mm)	146	146	146		
256-Ball ftBGA (17 x17 mm)	172	201	201	201	
484-Ball fpBGA (23 x 23 mm)			358	363	363
672-Ball fpBGA (27 x 27 mm)				472	540

Note: The information in this Advance Data Sheet is by definition not final and subject to change. Please consult the Lattice website and your local Lattice Sales Manager to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.

Introduction

LatticeXP2 devices combine a Look-up Table (LUT) based FPGA fabric with non-volatile Flash cells in an architecture referred to as flexiFLASH.

The flexiFLASH approach provides benefits including instant-on, infinite reconfigurability, on chip storage with FlashBAK embedded block memory and Serial TAG memory and design security. The parts also support Live Update technology with TransFR, 128-bit AES Encryption and Dual-boot technologies.

The LatticeXP2 FPGA fabric was optimized for the new technology from the outset with high performance and low cost in mind. LatticeXP2 devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support and enhanced sysDSP blocks.

The ispLEVER® design tool from Lattice allows large and complex designs to be efficiently implemented using the LatticeXP2 family of FPGA devices. Synthesis library support for LatticeXP2 is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeXP2 device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed Intellectual Property (IP) ispLeverCORE™ modules for the LatticeXP2 family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

LatticeXP2 Family Data Sheet Architecture

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Architecture Overview

Each LatticeXP2 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and a row of sysDSP™ Digital Signal Processing blocks as shown in Figure 2-1.

On the left and right sides of the Programmable Functional Unit (PFU) array, there are Non-volatile Memory Blocks. In configuration mode the nonvolatile memory is programmed via the IEEE 1149.1 TAP port or the sysCONFIG™ peripheral port. On power up, the configuration data is transferred from the Non-volatile Memory Blocks to the configuration SRAM. With this technology, expensive external configuration memory is not required, and designs are secured from unauthorized read-back. This transfer of data from non-volatile memory to configuration SRAM via wide busses happens in microseconds, providing an “instant-on” capability that allows easy interfacing in many applications. LatticeXP2 devices can also transfer data from the sysMEM EBR blocks to the Non-volatile Memory Blocks at user request.

There are two kinds of logic blocks, the PFU and the PFU without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

LatticeXP2 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large dedicated 18Kbit memory blocks. Each sysMEM block can be configured in a variety of depths and widths of RAM or ROM. In addition, LatticeXP2 devices contain up to two rows of DSP Blocks. Each DSP block has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

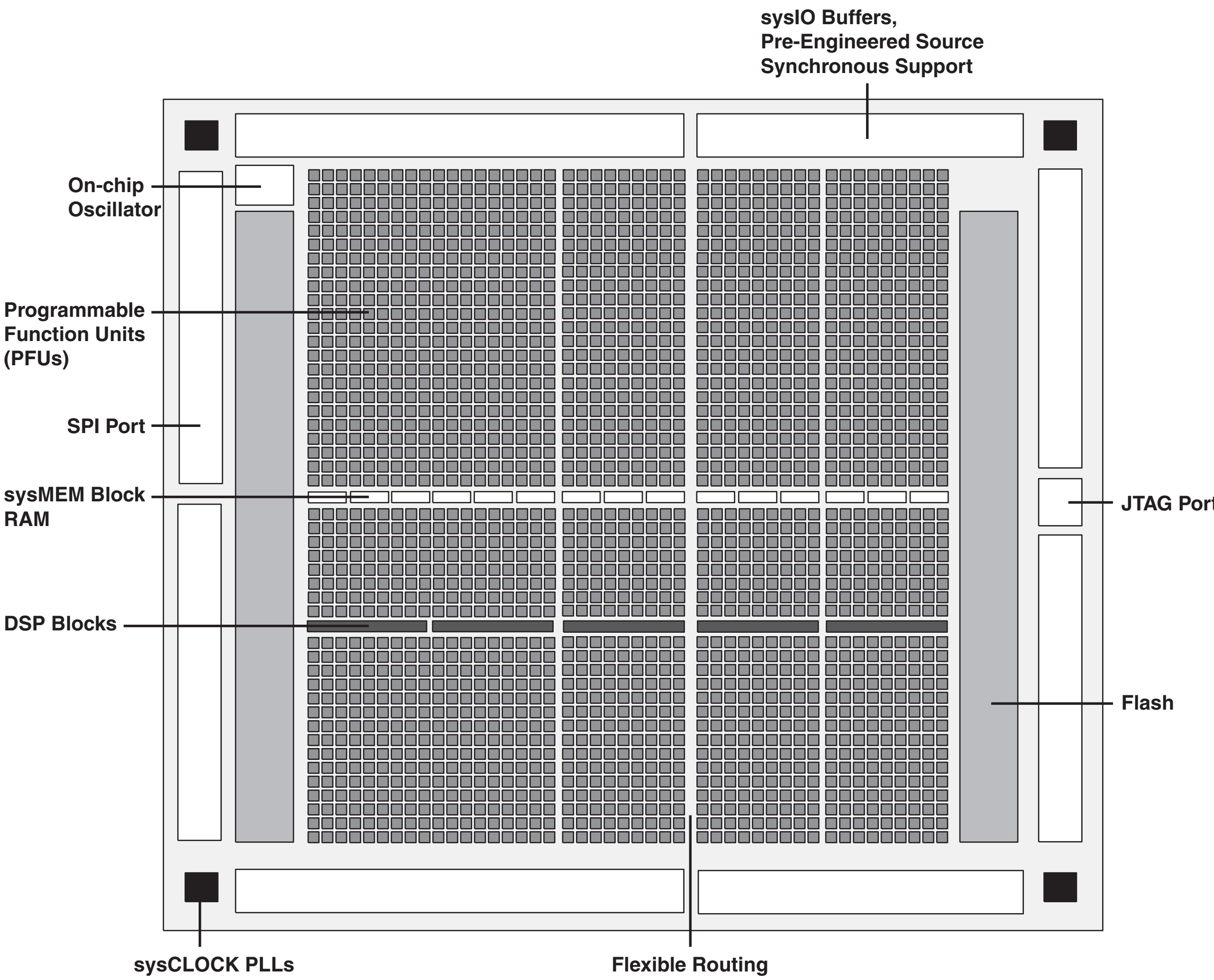
Each PIC block encompasses two PIOs (PIO pairs) with their respective sysIO buffers. The sysIO buffers of the LatticeXP2 devices are arranged into eight banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for programming interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as 7:1 LVDS interfaces, found in many display applications, and memory interfaces including DDR and DDR2.

Other blocks provided include PLLs and configuration functions. The LatticeXP2 architecture provides up to four General Purpose PLLs (GPLL) per device. The GPLL blocks are located in the corners of the device.

The configuration block that supports features such as configuration bit-stream de-encryption, transparent updates and dual boot support is located between banks two and three. Every device in the LatticeXP2 family supports a sysCONFIG port, muxed with bank seven I/Os, which supports serial device configuration. A JTAG port is provided between banks two and three.

This family also provides an on-chip oscillator and Soft Error Detect (SED) capability. LatticeXP2 devices use 1.2V as their core voltage.

Figure 2-1. Simplified Block Diagram, LatticeXP2-17 Device (Top Level)

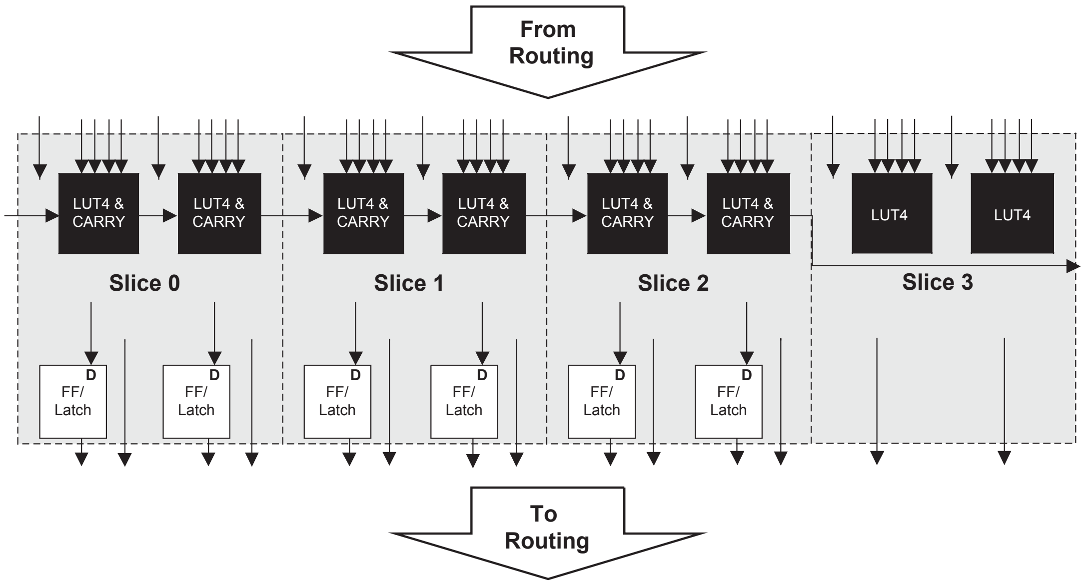


PFU Blocks

The core of the LatticeXP2 device is made up of logic blocks in two forms, PFUs and PFFs. PFUs can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. PFF blocks can be programmed to perform logic, arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered Slice 0 through Slice 3, as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

Figure 2-2. PFU Diagram



Slice

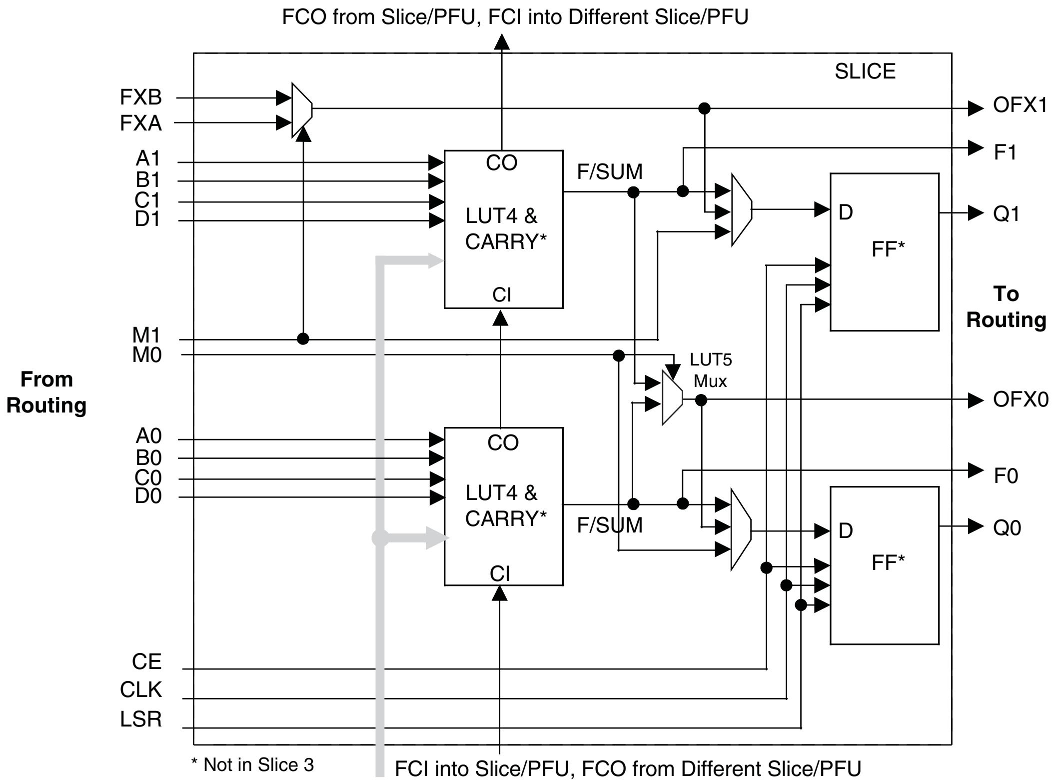
Slice 0 through Slice 2 contain two 4-input combinatorial Look-Up Tables (LUT4), which feed two registers. Slice 3 contains two LUT4s and no registers. For PFUs, Slice 0 and Slice 2 can also be configured as distributed memory, a capability not available in PFF blocks. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU BLock		PFF Block	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

Slice 0 through Slice 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 13 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

Figure 2-3. Slice Diagram



For Slices 0 and 2, memory control signals are generated from Slice 1 as follows:
- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data
- WAD [A:D] is a 4bit address from slice 1 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-In[1]
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output[1]

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as LUT4s. A LUT4 has 16 possible input combinations. Four-input logic functions are generated by programming the LUT4. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger LUTs such as LUT6, LUT7 and LUT8, can be constructed by concatenating two or more slices. Note that a LUT8 requires more than four slices.

Ripple Mode

Ripple mode allows efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two carry signals, FCI and FCO, are generated per slice in this mode, allowing fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed Single Port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit Pseudo Dual Port RAM (PDPR) memory is created by using one slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information on using RAM in LatticeXP2 devices, please see TN1137, *LatticeXP2 Memory Usage Guide.*

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16X4	PDPR 16X4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in the ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

Routing

There are many resources provided in the LatticeXP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) or x6 (spans seven PFU) connections. The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered to allow both short and long connections routing between PFUs.

The LatticeXP2 family has an enhanced routing architecture to produce a compact design. The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Phase Locked Loops (PLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The LatticeXP2 family supports between two and four full featured General Purpose PLLs (GPLL). The architecture of the GPLL is shown in Figure 2-4.

CLKI, the PLL reference frequency, is provided either from the pin or from routing; it feeds into the Input Clock Divider block. CLKFB, the feedback signal, is generated from CLKOP (the primary clock output) or from a user clock pin/logic. CLKFB feeds into the Feedback Divider and is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. The phase and frequency of the VCO are determined from the input path and feedback signals. A LOCK signal is generated by the VCO to indicate that the VCO is locked with the input clock signal.

The output of the VCO feeds into the CLKOP Divider, a post-scalar divider. The duty cycle of the CLKOP Divider output can be fine tuned using the Duty Trim block, which creates the CLKOP signal. By allowing the VCO to operate at higher frequencies than CLKOP, the frequency range of the GPLL is expanded. The output of the CLKOP Divider is passed through the CLKOK Divider, a secondary clock divider, to generate lower frequencies for the CLKOK output. For applications that require even lower frequencies, the CLKOP signal is passed through a divide-by-three divider to produce the CLKOK2 output. The CLKOK2 output is provided for applications that use source synchronous logic. The Phase/Duty Cycle/Duty Trim block is used to adjust the phase and duty cycle of the CLKOP Divider output to generate the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The clock outputs from the GPLL; CLKOP, CLKOK, CLKOK2 and CLKOS, are fed to the clock distribution network.

For further information on the GPLL please see TN1126, *LatticeXP2 sysCLOCK PLL Design and Usage Guide.*

Figure 2-4. General Purpose PLL (GPLL) Diagram

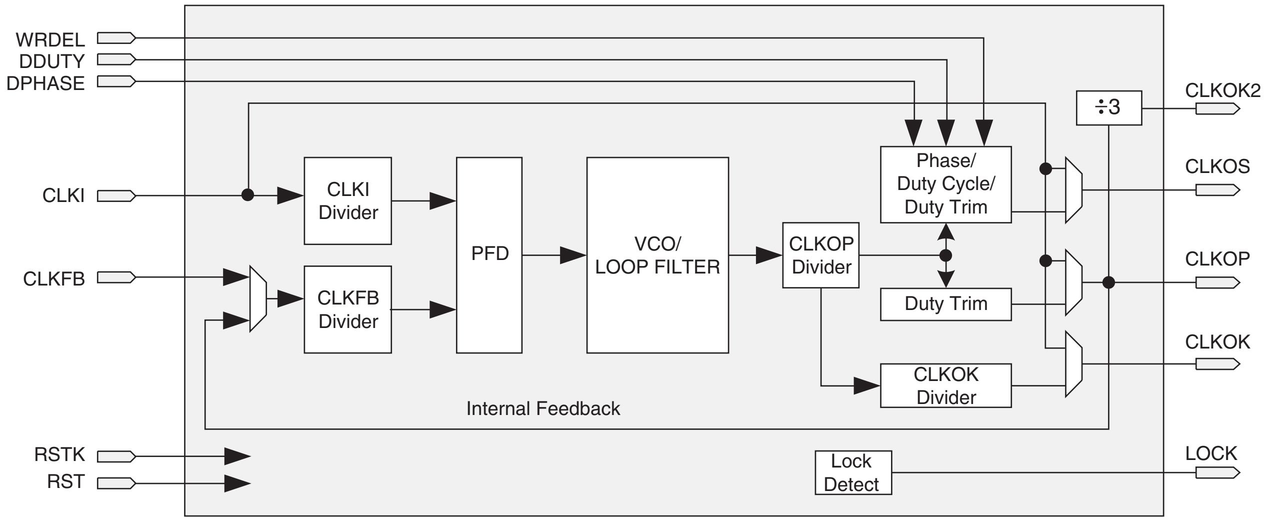


Table 2-4 provides a description of the signals in the GPLL blocks.

Table 2-4. GPLL Block Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	“1” to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	“1” to reset K-divider
DPHASE [3:0]	I	DPA Phase Adjust input
DDDUTY [3:0]	I	DPA Duty Cycle Select input
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
CLKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	“1” indicates PLL LOCK to CLKI

Clock Dividers

LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, please see TN1126, *sysCLOCK PLL Design and Usage Guide.* Figure 2-5 shows the clock divider connections.

IPexpress™

The user can access the sysDSP block via the ispLEVER IPexpress tool, which provides the option to configure each DSP module (or group of modules), or by direct HDL instantiation. In addition, Lattice has partnered with The MathWorks® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with ispLEVER to dramatically shorten the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeXP2 DSP include the Bit Correlator, FFT functions, FIR Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

Resources Available in the LatticeXP2 Family

Table 2-8 shows the maximum number of multipliers for each member of the LatticeXP2 family. Table 2-9 shows the maximum available EBR RAM Blocks and Serial TAG Memory bits in each LatticeXP2 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-8. Maximum Number of DSP Blocks in the LatticeXP2 Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
XP2-5	3	24	12	3
XP2-8	4	32	16	4
XP2-17	5	40	20	5
XP2-30	7	56	28	7
XP2-40	8	64	32	8

Table 2-9. Embedded SRAM/TAG Memory in the LatticeXP2 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)	TAG Memory (Bits)
XP2-5	9	166	632
XP2-8	12	221	768
XP2-17	15	276	2184
XP2-30	21	387	2640
XP2-40	48	885	3384

LatticeXP2 DSP Performance

Table 2-10 lists the maximum performance in Millions of MAC (MMAC) operations per second for each member of the LatticeXP2 family.

Table 2-10. DSP Performance

Device	DSP Block	DSP Performance MMAC
XP2-5	3	3,900
XP2-8	4	5,200
XP2-17	5	6,500
XP2-30	7	9,100
XP2-40	8	10,400

For further information on the sysDSP block, please see TN1140, *LatticeXP2 sysDSP Usage Guide.*

Table 2-13. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVCMOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVCMOS18	4mA, 8mA, 12mA, 16mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II	N/A	1.8
HSTL15 Class I	N/A	1.5
SSTL33 Class I, II	N/A	3.3
SSTL25 Class I, II	N/A	2.5
SSTL18 Class I, II	N/A	1.8
Differential Interfaces		
Differential SSTL33, Class I, II	N/A	3.3
Differential SSTL25, Class I, II	N/A	2.5
Differential SSTL18, Class I, II	N/A	1.8
Differential HSTL18, Class I, II	N/A	1.8
Differential HSTL15, Class I	N/A	1.5
LVDS[1, 2]	N/A	2.5
MLVDS[1]	N/A	2.5
BLVDS[1]	N/A	2.5
LVPECL[1]	N/A	3.3
RSDS[1]	N/A	2.5

1. Emulated with external resistors. For more detail, please see TN1138, *LatticeXP2 High Speed I/O Interface.*
2. On the left and right edges, LVDS outputs are supported with a dedicated differential output driver on 50% of the I/Os. This solution does not require external resistors at the driver.

Hot Socketing

LatticeXP2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeXP2 ideal for many multiple power supply and hot-swap applications.

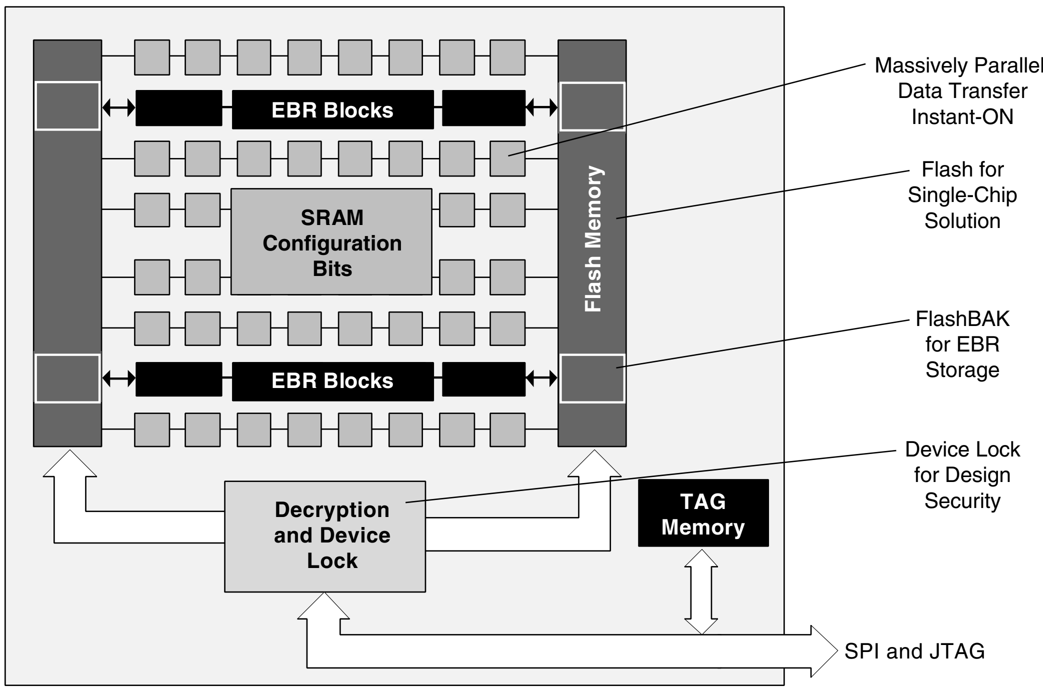
IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeXP2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards. For more information, please see TN1141, *LatticeXP2 sysCONFIG Usage Guide.*

flexiFLASH Device Configuration

The LatticeXP2 devices combine Flash and SRAM on a single chip to provide users with flexibility in device programming and configuration. Figure 2-33 provides an overview of the arrangement of Flash and SRAM configuration cells within the device. The remainder of this section provides an overview of these capabilities. See TN1141, *LatticeXP2 sysCONFIG Usage Guide,* for a more detailed description.

Figure 2-33. Overview of Flash and SRAM Configuration Cells Within LatticeXP2 Devices



At power-up, or on user command, data is transferred from the on-chip Flash memory to the SRAM configuration cells that control the operation of the device. This is done with massively parallel buses enabling the parts to operate within microseconds of the power supplies reaching valid levels; this capability is referred to as Instant-On.

The on-chip Flash enables a single-chip solution eliminating the need for external boot memory. This Flash can be programmed through either the JTAG or SPI ports of the device. The SRAM configuration space can also be infinitely reconfigured through the JTAG and SPI ports. The JTAG port is IEEE 1149.1 and IEEE 1532 compliant.

As described in the EBR section of the data sheet, the FlashBAK capability of the parts enables the contents of the EBR blocks to be written back into the Flash storage area without erasing or reprogramming other aspects of the device configuration. Serial TAG memory is also available to allow the storage of small amounts of data such as calibration coefficients and error codes.

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM only FPGAs. This is further enhanced by device locking. The device can be in one of three modes:

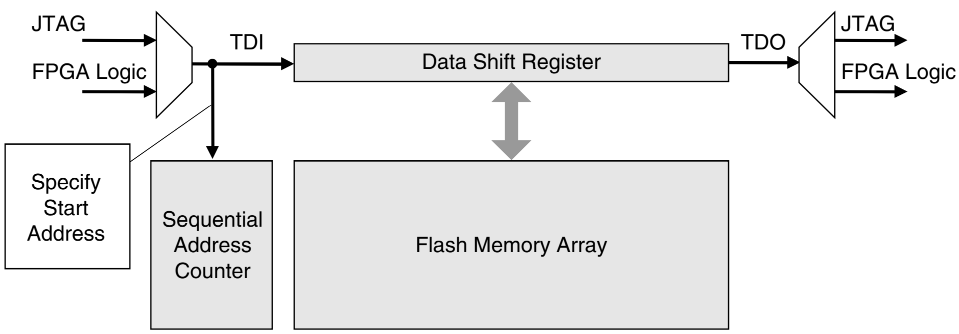
1. Unlocked
2. Key Locked – Presenting the key through the programming interface allows the device to be unlocked.
3. Permanently Locked – The device is permanently locked.

To further complement the security of the device a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash portion of the device.

Serial TAG Memory

LatticeXP2 devices offer 0.6 to 3.3kbits of Flash memory in the form of Serial TAG memory. The TAG memory is an area of the on-chip Flash that can be used for non-volatile storage including electronic ID codes, version codes, date stamps, asset IDs and calibration settings. A block diagram of the TAG memory is shown in Figure 2-34. The TAG memory is accessed in the same way as external SPI Flash and it can be read or programmed either through JTAG or directly from FPGA logic. To read the TAG memory, a start address is specified and the entire TAG memory contents are read sequentially in a first-in-first-out manner. The TAG memory is independent of the Flash used for device configuration and given its use for general-purpose storage functions is always accessible regardless of the device security settings. For more information, see TN1137, *LatticeXP2 Memory Usage Guide*, and TN1141, *LatticeXP2 sysCONFIG Usage Guide*.

Figure 2-34. Serial TAG Memory Diagram



Live Update Technology

Many applications require field updates of the FPGA. LatticeXP2 devices provide three features that enable this configuration to be done in a secure and failsafe manner while minimizing impact on system operation.

1. **Decryption Support**
   LatticeXP2 devices provide on-chip, non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and deterring design piracy.

2. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. For more information please see TN1143, *LatticeXP2 TransFR I/O.*

3. **Dual Boot Image Support**
   Dual boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeXP2 can be re-booted from this new configuration file. If there is a problem such as corrupt data during download or incorrect version number with this new boot image, the LatticeXP2 device can revert back to the original backup configuration and try again. This all can be done without power cycling the system. For more information please see TN1144, *LatticeXP2 Dual Boot Usage Guide.*

For more information on device configuration, please see TN1141, *LatticeXP2 sysCONFIG Usage Guide*.

Soft Error Detect (SED) Support

LatticeXP2 devices have dedicated logic to perform Cyclic Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, LatticeXP2 devices can be programmed for checking soft errors in SRAM. The SED operation can run in the background during user mode (normal operation). In the event a soft error occurs, the device can be programmed to either reload from a known good boot image (from internal Flash or external SPI memory) or generate an error signal.

For further information on SED support, please see TN1130, *LatticeXP2 Soft Error Detection (SED) Usage Guide*.

On-Chip Oscillator

Every LatticeXP2 device has an internal CMOS oscillator that is used to derive a Master Clock (CCLK) for configuration. The oscillator and CCLK run continuously and are available to user logic after configuration is complete. The available CCLK frequencies are listed in Table 2-14. When a different CCLK frequency is selected during the design process, the following sequence takes place:

1. Device powers up with the default CCLK frequency.
2. During configuration, users select a different CCLK frequency.
3. CCLK frequency changes to the selected frequency after clock configuration bits are received.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1141, *LatticeXP2 sysCONFIG Usage Guide.*

Table 2-14. Selectable CCLKs and Oscillator Frequencies During Configuration and User Mode

CCLK/Oscillator (MHz)
2.5[1]
3.1[2]
4.3
5.4
6.9
8.1
9.2
10
13
15
20
26
32
40
54
80[3]
163[3]

1. Software default oscillator frequency.
2. Software default CCLK frequency.
3. Frequency not valid for CCLK.

LatticeXP2 Family Data Sheet DC and Switching Characteristics

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Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . -0.5 to 1.32V

Supply Voltage V_{CCAUX} . . . . -0.5 to 3.75V

Supply Voltage V_{CCJ} . . . . -0.5 to 3.75V

Supply Voltage V_{CCPLL}[4] . . . . -0.5 to 3.75V

Output Supply Voltage V_{CCIO} . . . . -0.5 to 3.75V

Input or I/O Tristate Voltage Applied[5] . . . . . . -0.5 to 3.75V

Storage Temperature (Ambient) . . . . -65 to 150°C

Junction Temperature Under Bias (Tj) . . . . +125°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. V_{CCPLL} only available on PQFP and TQFP packages.
5. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCPLL}[1]	PLL Supply Voltage	3.135	3.465	V
V_{CCIO}[2, 3]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[2]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C

1. V_{CCPLL} only available on PQFP and TQFP packages.
2. If V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC}. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX}.
3. See recommended voltages by I/O standard in subsequent table.

On-Chip Flash Memory Specifications

Symbol	Parameter	Max.	Units
$N_{PROGCYC}$	Flash Programming Cycles		Cycles
$t_{RETENTION}$	Data Retention (10,000 Cycles)	20	Years

Hot Socketing Specifications[1, 2, 3, 4, 5]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX.)	—	—	+/-1	mA

1. Insensitive to sequence of V_{CC}, V_{CCAUX} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX} and V_{CCIO}.
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) or $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
4. LVCMOS and LVTTL only.
5. Note this table represents DC conditions. For the first 20ns after hot insertion, current specification is 8mA.

sysIO Recommended Operating Conditions

Over Recommended Operating Conditions

Standard	V_{CCIO} Min.	V_{CCIO} Typ.	V_{CCIO} Max.	V_{REF} (V) Min.	V_{REF} (V) Typ.	V_{REF} (V) Max.
LVCMOS33[2]	3.135	3.3	3.465	—	—	—
LVCMOS25[2]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[2]	1.14	1.2	1.26	—	—	—
LVTTL33[2]	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL18_I[2], SSTL18_II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I[2], SSTL25_II[2]	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I[2], SSTL33_II[2]	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I[2]	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I[2], HSTL18_II[2]	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25[2]	2.375	2.5	2.625	—	—	—
MLVDS25[1]	2.375	2.5	2.625	—	—	—
LVPECL33[1, 2]	3.135	3.3	3.465	—	—	—
BLVDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS[1, 2]	2.375	2.5	2.625	—	—	—
SSTL18D_I[2], SSTL18D_II[2]	1.71	1.8	1.89	—	—	—
SSTL25D_ I[2], SSTL25D_II[2]	2.375	2.5	2.625	—	—	—
SSTL33D_ I[2], SSTL33D_ II[2]	3.135	3.3	3.465	—	—	—
HSTL15D_ I[2]	1.425	1.5	1.575	—	—	—
HSTL18D_ I[2], HSTL18D_ II[2]	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. Input on this standard does not depend on the value of V_{CCIO}.

LatticeXP2 Internal Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.218	—	0.239	—	0.260	ns
t_{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.420	—	0.457	—	0.494	ns
t_{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.690	—	0.754	—	0.818	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.147	—	0.147	—	0.148	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.059	—	-0.056	—	-0.053	—	ns
t_{SUD_PFU}	Clock to D input setup time	0.070	—	0.082	—	0.093	—	ns
t_{HD_PFU}	Clock to D input hold time	0.002	—	0.003	—	0.003	—	ns
t_{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.328	—	0.356	—	0.383	ns
t_{RSTREC_PFU}	Asynchronous reset recovery time for PFU Logic	—	0.498	—	0.623	—	0.748	ns
t_{RST_PFU}	Asynchronous reset time for PFU Logic	—	0.690	—	0.754	—	0.818	ns
PFU Dual Port Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output (F Port)	—	1.037	—	1.244	—	1.452	ns
t_{SUDATA_PFU}	Data Setup Time	-0.198	—	-0.236	—	-0.274	—	ns
t_{HDATA_PFU}	Data Hold Time	0.229	—	0.271	—	0.312	—	ns
t_{SUADDR_PFU}	Address Setup Time	-0.282	—	-0.327	—	-0.371	—	ns
t_{HADDR_PFU}	Address Hold Time	0.282	—	0.327	—	0.371	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	-0.140	—	-0.167	—	-0.193	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.152	—	0.179	—	0.207	—	ns
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.609	—	0.641	—	0.674	ns
t_{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.029	—	1.029	—	1.246	ns
IOLOGIC Input/Output Timing								
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.596	—	0.645	—	0.694	—	ns
t_{HI_PIO}	Input Register Hold Time (Data after Clock)	-0.570	—	-0.614	—	-0.658	—	ns
t_{COO_PIO}	Output Register Clock to Output Delay	—	0.61	—	0.66	—	0.72	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	0.032	—	0.037	—	0.041	—	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	-0.022	—	-0.025	—	-0.028	—	ns
t_{SULSR_PIO}	Set/Reset Setup Time	0.184	—	0.201	—	0.217	—	ns
t_{HLSR_PIO}	Set/Reset Hold Time	-0.080	—	-0.086	—	-0.093	—	ns
t_{RSTREC_PIO}	Asynchronous reset recovery time for IO Logic	—	0.228	—	0.247	—	0.266	ns

Flash Download Time (from On-Chip Flash to SRAM)

Over Recommended Operating Conditions

Symbol	Parameter		Min.	Typ.	Max.	Units
$t_{REFRESH}$	PROGRAMN Low-to-High. Transition to Done High.	XP2-5	—			ms
		XP2-8	—			ms
		XP2-17	—	1.65		ms
		XP2-30	—			ms
		XP2-40	—			ms
	PROGRAMN $V_{CC} = V_{CC}$ Min.	XP2-5	—			ms
		XP2-8	—			ms
		XP2-17	—	1.65		ms
		XP2-30	—			ms
		XP2-40	—			ms

Flash Program Time

Over Recommended Operating Conditions

Device	Flash Density		Program Time		Units
			Typ.	Max.	
XP2-5	1.2M	TAG			Seconds
		Main Array			Seconds
XP2-8	2.0M	TAG			Seconds
		Main Array			Seconds
XP2-17	3.6M	TAG	0.02		Seconds
		Main Array	5.97		Seconds
XP2-30	6.0M	TAG			Seconds
		Main Array			Seconds
XP2-40	8.0M	TAG			Seconds
		Main Array			Seconds

Flash Erase Time

Over Recommended Operating Conditions

Device	Flash Density		Erase Time		Units
			Typ.	Max.	
XP2-5	1.2M	TAG			Seconds
		Main Array			Seconds
XP2-8	2.0M	TAG			Seconds
		Main Array			Seconds
XP2-17	3.6M	TAG	0.33		Seconds
		Main Array	4.20		Seconds
XP2-30	6.0M	TAG			Seconds
		Main Array			Seconds
XP2-40	8.0M	TAG			Seconds
		Main Array			Seconds

FlashBAK Program Time (from EBR to Flash)

Over Recommended Operating Conditions

Device	Flash Density	Program Time		Units
		Typ.	Max.	
XP2-5	1.2M			Seconds
XP2-8	2.0M			Seconds
XP2-17	3.6M	1.3		Seconds
XP2-30	6.0M			Seconds
XP2-40	8.0M			Seconds

JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK Clock Frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Timing v. A 0.06

LatticeXP2 Family Data Sheet
Ordering Information

Part Number Description

LFXP2 – XX E – X XXXXX X

Device Family
XP2

Logic Capacity
5 = 5K LUTs
8 = 8K LUTs
17 = 17K LUTs
30 = 30K LUTs
40 = 40K LUTs

Supply Voltage
E = 1.2V

Speed
5 = Slowest
6
7 = Fastest

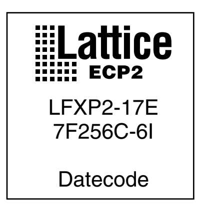
Grade
C = Commercial
I = Industrial

Package
M132 = 132-ball csBGA
T144 = 144-pin TQFP
Q208 = 208-pin PQFP
FT256 = 256-ball ftBGA
F484 = 484-ball fpBGA
F672 = 672-ball fpBGA

MN132 = 132-ball Lead-Free csBGA
TN144 = 144-pin Lead-Free TQFP
QN208 = 208-pin Lead-Free PQFP
FTN256 = 256-ball Lead-Free ftBGA
FN484 = 484-ball Lead-Free fpBGA
FN672 = 672-ball Lead-Free fpBGA

Ordering Information

Note: LatticeXP2 devices are dual marked. For example, the commercial speed grade LFXP2-17E-7256C is also marked with industrial grade -6I (LFXP2-17E-6256I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:



Conventional Packaging

Commercial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5Q208C	1.2V	-5	PQFP	208	COM	17
LFXP2-17E-6Q208C	1.2V	-6	PQFP	208	COM	17
LFXP2-17E-7Q208C	1.2V	-7	PQFP	208	COM	17
LFXP2-17E-5FT256C	1.2V	-5	ftBGA	256	COM	17
LFXP2-17E-6FT256C	1.2V	-6	ftBGA	256	COM	17
LFXP2-17E-7FT256C	1.2V	-7	ftBGA	256	COM	17
LFXP2-17E-5F484C	1.2V	-5	fpBGA	484	COM	17
LFXP2-17E-6F484C	1.2V	-6	fpBGA	484	COM	17
LFXP2-17E-7F484C	1.2V	-7	fpBGA	484	COM	17

Industrial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5Q208I	1.2V	-5	PQFP	208	COM	17
LFXP2-17E-6Q208I	1.2V	-6	PQFP	208	COM	17
LFXP2-17E-5FT256I	1.2V	-5	ftBGA	256	COM	17
LFXP2-17E-6FT256I	1.2V	-6	ftBGA	256	COM	17
LFXP2-17E-5F484I	1.2V	-5	fpBGA	484	COM	17
LFXP2-17E-6F484I	1.2V	-6	fpBGA	484	COM	17

Lead-Free Packaging

Commercial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208C	1.2V	-5	Lead-Free PQFP	208	IND	17
LFXP2-17E-6QN208C	1.2V	-6	Lead-Free PQFP	208	IND	17
LFXP2-17E-7QN208C	1.2V	-7	Lead-Free PQFP	208	IND	17
LFXP2-17E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	IND	17
LFXP2-17E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	IND	17
LFXP2-17E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	IND	17
LFXP2-17E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	IND	17
LFXP2-17E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	IND	17
LFXP2-17E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	IND	17

Industrial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	17
LFXP2-17E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	17
LFXP2-17E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	17
LFXP2-17E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	17
LFXP2-17E-5FN484I	1.2V	-5	Lead-Free fpBGA	484	IND	17
LFXP2-17E-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	17

LatticeXP2 Family Handbook
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Section II. LatticeXP2 Family Technical Notes

LatticeXP2 sysIO Usage Guide

LatticeXP2 sysCLOCK PLL Design and Usage Guide

LatticeXP2 Memory Usage Guide

LatticeXP2 FPGA Application Notes

Access individual documents by clicking on the document title, or select multiple documents by using the checkboxes and clicking the "Download Selected Files as ZIP Archive" button.

- TN1033 - High-Speed PCB Design Considerations (v6) (431K .pdf)
- TN1040 - LatticeXP2 sysDSP Usage Guide Technical Note (1187K .pdf)
- TN1074 - PCB Layout Recommendations for BGA Packages (104K .pdf)
- TN1076 - Solder Reflow Guide for Surface Mount Devices (42K .pdf)
- TN1087 - Minimizing System Interruption During Configuration Using TransFR Technology Technical Note (721K .pdf)
- TN1126 - LatticeXP2 sysCLOCK PLL Design and Usage Guide (672K .pdf)
- TN1130 - LatticeXP2 Soft Error Detection (SED) Usage Guide Technical Note (187K .pdf)
- TN1136 - LatticeXP2 sysIO Usage Guide (295K .pdf)
- TN1137 - LatticeXP2 Memory Usage Guide Technical Note (1234K .pdf)
- TN1138 - LatticeXP2 High-Speed I/O Interface Technical Note (1582K .pdf)
- TN1139 - Power Estimation and Management for LatticeXP2 Devices Technical Note (1180K .pdf)
- TN1141 - LatticeXP2 sysCONFIG Usage Guide Technical Note (156K .pdf)
- TN1142 - LatticeXP2 Configuration Encryption and Security Usage Guide Technical Note (460K .pdf)
- TN1144 - LatticeXP2 Dual Boot Usage Guide Technical Note (383K .pdf)
- Thermal Management (66K .pdf)

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LatticeXP2 FPGA BSDL Models

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Icon Key:

R Restricted access (account Sign-in required)

- R [BSDL] LFXP217E 208 PQFP Ver 1.0 (50K .bsm)
- R [BSDL] LFXP217E 256 FPBGA Ver 1.0 (54K .bsm)
- R [BSDL] LFXP217E 484 FPBGA Ver 1.0 (70K .bsm)

Contact Details
Customer Service Area
JTAG Partnerships
Device Support
- PLDs
- Flash
- Special Programmable Devices
- Mixed Signal Devices
- System Level
- Embedded Test
- BSDL Models
EDA Support

BSDL Models

BSDL Models - Company Links

BSDL (Boundary-Scan Description Language) files are necessary for the application of boundary-scan for board and system level testing and in-system programming. BSDL files are the electronic data sheets that describe the IEEE 1149.1 or JTAG design within an IC, and are provided by the IC vendors as a part of their device specification.

Actel	Music
Altera	National Semiconductor
AMD	PMC Sierra
Analog Devices	QuickLogic
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Freescale Semiconductor	Texas Instruments
IDT	Tundra
Intel	Xilinx
Lattice	Zarlink

It is impossible to list all the BSDL files we have worked with. For customers with a valid maintenance contract we would be pleased to share our experience. We have experience with several other companies, such as: Conexant, Broadbus, AMCC, Hitachi, IBM, Mitel, SEMTech, Sony, TI DSPs, and so on. Please contact our support group to help you find a solution, or if you have remarks on companies not listed or not correctly listed here.