ECE 271 Lab #1

Winter 2005

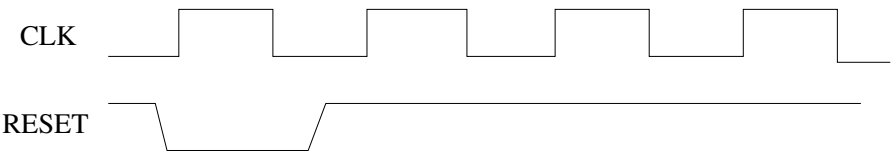
You are to build a 2-bit counter circuit using D-FFs. The implementation equations are

$$D_0 = \overline{Q}_0$$

$$D_1 = Q_0 \oplus Q_1$$

where Q_0 is the LSB. Design the circuit so that an (active low) signal $RESET$ will clear the counter when it is asserted.

1. Give a schematic of your design
2. Based on your design, complete the following timing diagram:



3. Build your circuit and connect a 100 Hz clock to the counter. Record the counter's output for at least 6 clock pulses using a logic analyzer.

NOTE: You will receive NO credit for this lab unless you include a hardcopy of the logic analyzer's display.