

Table 9-1. Interrupt Vector Map

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
\$FFFE, \$FFFF	Reset	None	None	—
\$FFFC, \$FFFD	Clock monitor fail reset	None	COPCTL (CME, FCME)	—
\$FFFA, \$FFFB	COP failure reset	None	COP rate selected	—
\$FFF8, \$FFF9	Unimplemented instruction trap	None	None	—
\$FFF6, \$FFF7	SWI	None	None	—
\$FFF4, \$FFF5	XIRQ	X bit	None	—
\$FFF2, \$FFF3	IRQ	I bit	INTCR (IRQEN)	\$F2
\$FFF0, \$FFF1	Real time interrupt	I bit	RTICTL (RTIE)	\$F0
\$FFEE, \$FFEF	Timer channel 0	I bit	TMSK1 (C0I)	\$EE
\$FFEC, \$FFED	Timer channel 1	I bit	TMSK1 (C1I)	\$EC
\$FFEA, \$FFEB	Timer channel 2	I bit	TMSK1 (C2I)	\$EA
\$FFE8, \$FFE9	Timer channel 3	I bit	TMSK1 (C3I)	\$E8
\$FFE6, \$FFE7	Timer channel 4	I bit	TMSK1 (C4I)	\$E6
\$FFE4, \$FFE5	Timer channel 5	I bit	TMSK1 (C5I)	\$E4
\$FFE2, \$FFE3	Timer channel 6	I bit	TMSK1 (C6I)	\$E2
\$FFE0, \$FFE1	Timer channel 7	I bit	TMSK1 (C7I)	\$E0
\$FFDE, \$FFDF	Timer overflow	I bit	TMSK2 (TOI)	\$DE
\$FFDC, \$FFDD	Pulse accumulator overflow	I bit	PACTL (PAOVI)	\$DC
\$FFDA, \$FFDB	Pulse accumulator input edge	I bit	PACTL (PAI)	\$DA
\$FFD8, \$FFD9	SPI serial transfer complete	I bit	SP0CR1 (SPIE)	\$D8
\$FFD6, \$FFD7	SCI 0	I bit	SC0CR2 (TIE, TCIE, RIE, ILIE)	\$D6
\$FFD4, \$FFD5	SCI 1	I bit	SC1CR2 (TIE, TCIE, RIE, ILIE)	\$D4
\$FFD2, \$FFD3	ATD0 or ATD1	I bit	ATDxCTL2 (ASCIE)	\$D2
\$FFD0, \$FFD1	MSCAN wake-up	I bit	CRIER (WUPIE)	\$D0
\$FFCE, \$FFCF	Key wake-up G or H	I bit	KWIEG[6:0] and KWIEH[7:0]	\$CE
\$FFCC, \$FFCD	Modulus down counter underflow	I bit	MCCTL (MCZI)	\$CC
\$FFCA, \$FFCB	Pulse Accumulator B Overflow	I bit	PBCTL (PBOVI)	\$CA
\$FFC8, \$FFC9	MSCAN errors	I bit	CRIER (RWRNIE, TWRNIE, RERRIE, TERRIE, BOFFIE, OVRIE)	\$C8
\$FFC6, \$FFC7	MSCAN receive	I bit	CRIER (RXFIE)	\$C6
\$FFC4, \$FFC5	MSCAN transmit	I bit	CTCR (TXEIE[2:0])	\$C4
\$FFC2, \$FFC3	CGM lock and limp home	I bit	PLLCL (LOCKIE, LHIE)	\$C2
\$FF80–\$FFC1	Reserved	I bit		\$80–\$C0