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– VHDL implementation of a D-FF
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entity FindSeq is port(
    clk: in bit;
    clear: in bit;
    serdata: in bit;
    Q: buffer bit;
    QBAR: out bit);
end FindSeq;

architecture ArchFindSeq of FindSeq is
type states is (A, B);
signal state: states;

    begin
    fsm: process (clk, clear)
    begin
        if(clk'event and clk='1') then
            if clear='0' then                          – initialize flip-flop
                state <= A;
            else
                case state is
                    when A =>                          – in state 'A'
                        if  serdata = '0' then
                            state <= A;
                        else
                            state <= B;
                        end if;

                    when B =>                          – in state 'B'
                        if  serdata = '1' then
                            state <= B;
                        else
                            state <= A;
                        end if;

                end case;
            end if;
        end if;
    end process fsm;
    Q <= '0' when (state = A) else
        '1';
    QBAR <= not(Q);

end ArchFindSeq;
```