ECE 271 Final Win '03

SOLUTIONS

1. Exhaustive testing can always provide 100% fault coverage.

   b. FALSE

2. The state assignments of a FSM are described in Verilog using

   a. a parameter statement

3. A DRAM refresh operation consists of keeping $\overline{\text{CAS}}$ high while pulsing $\overline{\text{RAS}}$ many times. This is an example of

   c. $\overline{\text{RAS}}$ -only refresh

4. You can use either D FFs or D latches to build a 3-bit binary counter.

   b. FALSE

5. All state machines need a clock.

   b. FALSE (remember asynchronous state machines???)

NOTE: Questions 6 and 7 concern a Mealy FSM described by the following state table:

Present State	Next State		Next Output (Z)	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
A	B	B	1	1
B	A	B	1	0

The FSM is implemented with a D-type FF. There are no equivalent states. The state assignments are A=0 and B=1.

6. If x is the input and y is the present state FF output, then the FF input boolean equation is

   d. none of the above

7. The FF output boolean equation is

   c. Z= $\overline{x \cdot y}$

8. Can you buy a Cypress CY7C185 SRAM in a ball grid array package?

   (b) NO

9. The generating polynomial for an n-bit LFSR is non-primitive. The total number of unique test patterns this circuit can produce is

   d. $< 2^n - 1$

10. A core is sold as a gate-level netlist. This core is

    b. firm

11. A VLSI chip has scan insertion. How does a test engineer determine the response of internal circuitry to a particular test pattern?

    b. The scan chain contains the response. It is clocked out at the same time the next test pattern is clocked in.

12. A core has a sequential depth of 8 and a combinational width of 9. How many test patterns are needed for exhaustive testing?

    c. 128K

13. You need to order a 27C64 EPROM with a 170 ns access time in a commercial temperature range and in a small outline package. Which of the following is contained in the correct part number?

    e. none of the above

14. Does the FSM described below contain any equivalent states?

	$x_1x_2 = 00$	$x_1x_2 = 01$	$x_1x_2 = 11$	$x_1x_2 = 10$	output
R	U	R	U	V	1
S	U	V	U	R	0
T	S	T	T	T	0
U	R	R	S	V	1
V	V	U	T	S	1

(b) NO

15. What is the cause of a metastable state?

a. failure to meet a setup time requirement

16. A digital circuit has a MTBF of 20 years. What is the probability $\mathcal{P}$ this circuit will fail in the next 30 days?

c. $0.1\% < \mathcal{P} \leq 1\%$

17. Consider the timing diagram at the top of page 563 in your textbook. This timing diagram represents

b. a ring counter

18. The three outputs of a modulo-5 counter have a 50% duty cycle.

    b. FALSE

19. How long after $\overline{OE}$ is asserted does it take before a CY7C185-20 SRAM can provide valid data?

    b. 9 ns

20. Which of the following devices is non-volatile?

    c. EPROM

21. Which of the following memory devices are erased with a voltage level?

    d. none of the above (EPROMs are done with UV light; FLASH EPROMs are done with a voltage. FLASH EPROM was not one of the available choices.)

22. DFT often requires adding devices to a design in support of test. These additional devices should be removed before the design goes into production.

    b. FALSE

23. Consider the timing diagram on page 546 of your textbook. Assuming Y2 is the most significant bit, the count sequence is

    e. none of the above

24. The 54HC160 counter is a FSM.

    a. TRUE

25. In some FPGAs the logic circuit is implemented using lookup tables (LUTs). These LUTs are often implemented with

    d. memory devices