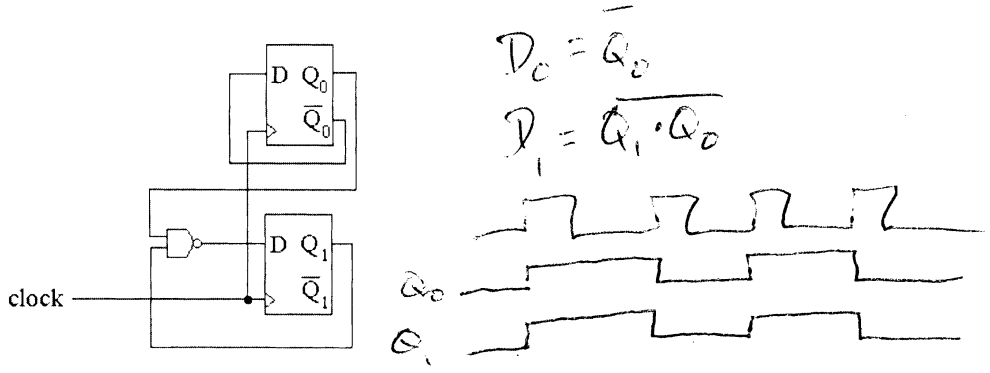
ECE 271 Midterm #2 Solu

All questions are equally weighted in this open book/open note exam. You are to choose the best answer and mark it on your SCANTRON sheet.

1. All modulo-*n* counter circuits meet the definition of a FSM.

a. TRUE
b. FALSE

2. Consider the following schematic:



The circuit implements which of the following count sequences?

a. $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 0 \rightarrow \ldots$
b. $3 \rightarrow 1 \rightarrow 2 \rightarrow 0 \rightarrow 3 \rightarrow \ldots$
c. $0 \rightarrow 2 \rightarrow 1 \rightarrow 3 \rightarrow 0 \rightarrow \ldots$
d. none of the above

3. Which type of counter would you expect to operate at a higher frequency?

a. asynchronous counter
b. synchronous counter

4. Which of the following generates a 50% duty cycle output:
   a. ring counter
   b. modulo-n counter
   c. twisted ring counter
   d. decade counter

5. Which of the following is NOT true concerning the 54LV163 counter
   a. it has a synchronous load function
   b. it is a binary counter
   c. RCO is asserted when the count is maximum
   d. The two enables are active low.

6. One of your classmates says "*CLR is the highest priority input on the 54LV163 counter.*" Do you agree?
   a. yes
   b. no

7. A shift register is made with 74LVC2G74 flip-flops operating at VCC = 3.3V. Which of the following is closest to the maximum clock speed of that circuit?
   a. 100 MHz
   b. 122 MHz
   c. 139 MHz
   d. 175 MHz

$5.9 + 1.3 = 7.2\,ns$

$\frac{1}{7.2} \times 10^9 =$

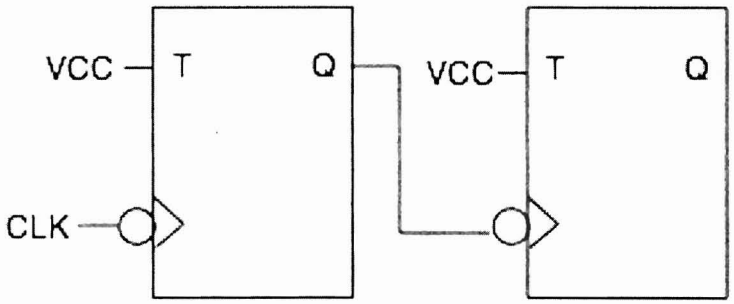
8. How can you initialize a counter?
   a. by providing two clock pulses within 2 ns of each other
   b. with a power-on reset circuit
   c. with a manually applied reset pulse
   d. all of the above
   e. (b) or (c) only

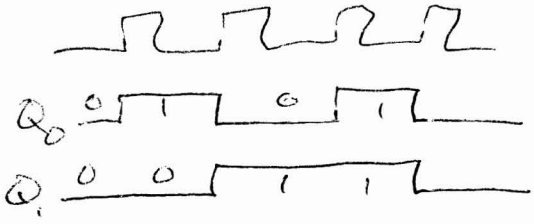
9. You are building a modulo-832 counter using only 54LV163 counters. How many 54LV163 counters are needed?
   a. 2
   b. 3
   c. 8
   d. 16
   e. none of the above

10. What is the output value of the counter in problem 9 when CLR on the 54LV163 counters is asserted?
    a. 831
    b. 832
    c. 0
    d. none of the above

11. The macrocells in a GAL22V10 have a synchronous preset.
    a. TRUE
    b. FALSE

12. A ring counter is implemented in a PAL16R4-15C. What is the maximum clock speed?
    a. 22 MHz
    b. 27 MHz
    c. 37 MHz
    d. 41 MHz





13. The count sequence of the above counter is
    a. $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 0 \rightarrow \ldots$
    b. $3 \rightarrow 1 \rightarrow 2 \rightarrow 0 \rightarrow 3 \rightarrow \ldots$
    c. $0 \rightarrow 2 \rightarrow 1 \rightarrow 3 \rightarrow 0 \rightarrow \ldots$
    d. none of the above

14. The counter of problem 13 is an example of an asynchronous counter.
    a. TRUE
    b. FALSE

15. A 68-pin PGA is physically larger than a 68-pin flat pack package. (Do not include the area of the pins that extend beyond the flat pack page; only consider the body of the package.)
    a. TRUE
    b. FALSE

16. An EPROM is erased with
    a. a voltage
    b. UV light
    c. infared light
    d. an eraser at the end of a pencil
    e. (b) or (c)

17. Which of the following devices erases memory in small blocks of memory locations?
    a. EPROM
    b. EEPROM
    c. E^2PROM
    d. flash memory
    e. none of the above

18. On the AT27BV010 EPROM, OE must be asserted at the same time (or before) CE is asserted or the minimum memory access time cannot be achieved.
    a. TRUE
    b. FALSE

19. Suppose you want to order a GAL22V10 with a propagation delay of 10 ns in a lead free plastic leadless chip carrier package. You want the low power version in the industrial temperature range. What is the part number?
    a. GAL22V10D-7LJN
    b. GAL22V10D-10QJI
    c. GAL22V10D-10LJNI
    d. none of the above

20. Which package has pins that extend from the sides of the package?
    a. PGA
    b. BGA
    c. PLCC
    d. (a) or (b)
    e. none of the above