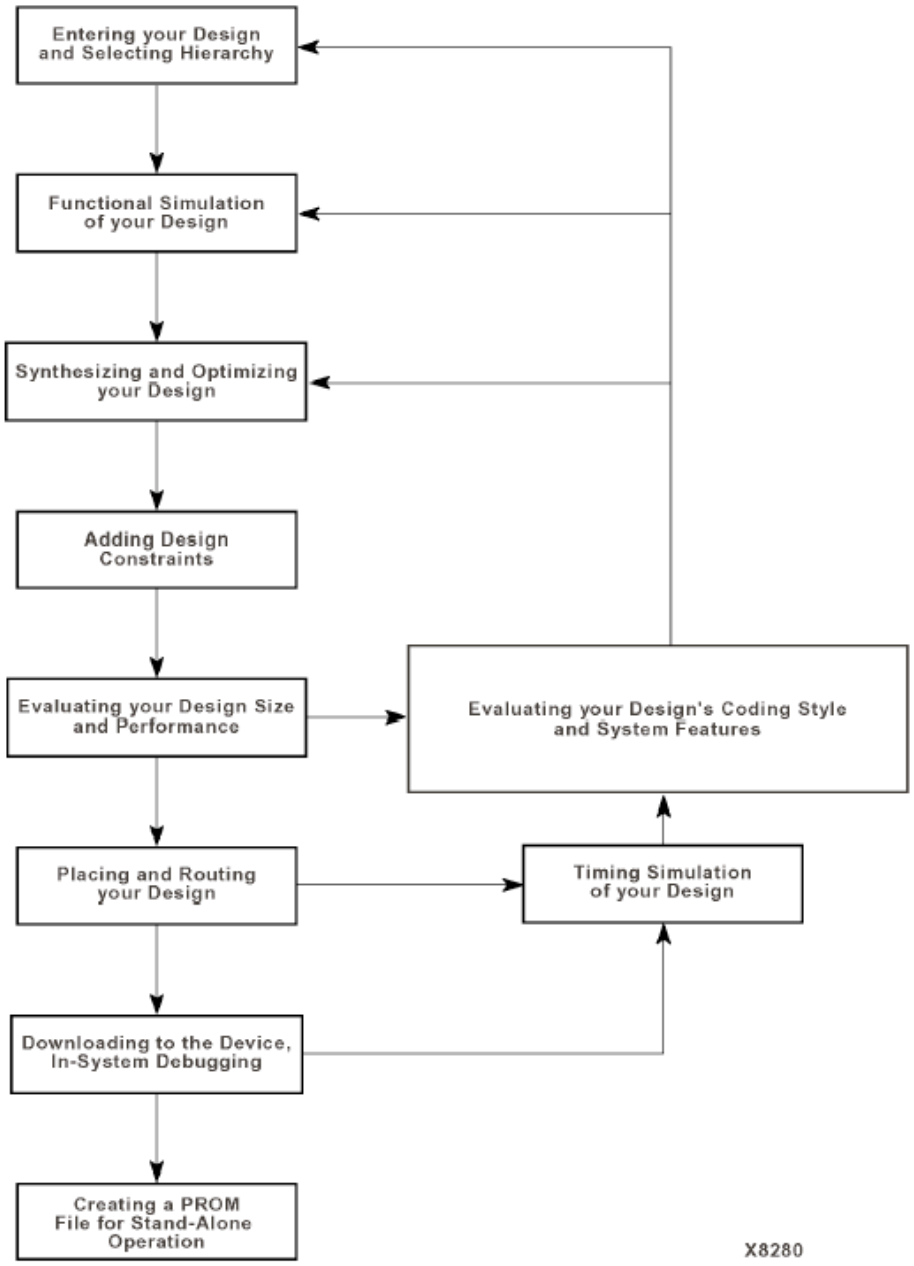
Entering your Design and Selecting Hierarchy
Functional Simulation of your Design
Synthesizing and Optimizing your Design
Adding Design Constraints
Evaluating your Design Size and Performance
Evaluating your Design's Coding Style and System Features
Placing and Routing your Design
Timing Simulation of your Design
Downloading to the Device, In-System Debugging
Creating a PROM File for Stand-Alone Operation
X8280

1. Entering your design and selecting hierarchy

   This is the step where you perform partitioning and write your RTL code.

2. Simulation

   This is a functional checkout using a testbench

3. Synthesis

   First, you create a *setup file* that defines compiler defaults and identifies your technology libraries. Second, you create a *script file* that runs the compiler. (You can also do this with a graphical interface, but that is tedious if you are making lots of incremental changes.) The output is a synthesized netlist in EDIF or XNF format, which Xilinx software can use.

4. Add constraints

   You create a *user constraint file* to identify timing and other constraints.

5. Evaluate the design size and performance

   These are design automation tools that estimate timing and whether or not design will fit into target device i.e., the FPGA you specified. The synthesis tool provides estimates that are contained in report files. Other design automation tools are available to get actual results prior to implementation.

6. Evaluate your coding style

   If the design evaluation in step 5 is unacceptable, you may have to modify the design. For example, you may have to reassess the design hierarchy if the size is too big. (Remember, smaller modules are easier to optimize.)

7. Place & routing

   This is the implementation phase where the design is mapped to specific FPGA LUTs and the routing between logic blocks is determined. The I/O is also determined and the pinout is defined.

8. Timing simulation

   After the worst-case timing delays are determined from the layout, the timing can be verified. Often this is evaluated using the same testbench used for functional checkout.

9. Download

   A datafile (.bit) is created for downloading into the device.

10. Stand-alone PROM

    RAM based FPGAs must be programmed when powered up. This is usually done from a PROM when the FPGA is installed in a circuit.

NOTES:

◇ Synthesis tool venders provide interface instructions for each major FPGA vendor and vice versa.

◇ The amount of vendor's literature one frequently must wade through (application notes, manuals, etc.) can be quite large!

◇ The design flow diagram is extracted from the Xilinx Synthesis & Simulation Design Guide (2.1i). This is a 312 page application note. If interested, you can download a copy by going to the Xilinx web site (www.xilinx.com).