The interrupt force and clear register, IFC, is a write-only register that contains a force bit and a clear bit for each interrupt (except for level-sensitive interrupts and the ADSP-2111 HIP interrupts—these cannot be forced or cleared in software).

When responding to an interrupt, the ASTAT, MSTAT, and IMASK status registers are pushed onto the status stack and the PC counter is loaded with the appropriate vector address. The status stack is seven levels deep (nine levels deep on the ADSP-2111) to allow interrupt nesting. The stack is automatically popped when a return from the interrupt instruction is executed.

Pin Definitions

Table IV (on next page) shows pin definitions for the ADSP-21xx processors. Any inputs not used must be tied to V_{DD}.

Table III. Interrupt Vector Addresses & Priority

ADSP-2105 Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0010
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0014
Timer	0x0018 *(Low Priority)*

ADSP-2101/2103/2115/216x Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
SPORT0 Transmit	0x0008
SPORT0 Receive	0x000C
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0010
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0014
Timer	0x0018 *(Low Priority)*

ADSP-2111 Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
HIP Write from Host	0x0008
HIP Read to Host	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0018
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x001C
Timer	0x0020 *(Low Priority)*

SYSTEM INTERFACE

Figure 3 shows a typical system for the ADSP-2101, ADSP-2115, or ADSP-2103, with two serial I/O devices, a boot EPROM, and optional external program and data memory. A total of 15K words of data memory and 16K words of program memory is addressable for the ADSP-2101 and ADSP-2103. A total of 14.5K words of data memory and 15K words of program memory is addressable for the ADSP-2115.

Figure 4 shows a system diagram for the ADSP-2105, with one serial I/O device, a boot EPROM, and optional external program and data memory. A total of 14.5K words of data memory and 15K words of program memory is addressable for the ADSP-2105.

Figure 5 shows a system diagram for the ADSP-2111, with two serial I/O devices, a host processor, a boot EPROM, and optional external program and data memory. A total of 15K words of data memory and 16K words of program memory is addressable.

Programmable wait-state generation allows the processors to easily interface to slow external memories.

The ADSP-2101, ADSP-2103, ADSP-2115, and ADSP-2111 processors also provide either: one external interrupt ($\overline{\text{IRQ2}}$) and two serial ports (SPORT0, SPORT1), *or* three external interrupts ($\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$) and one serial port (SPORT0).

The ADSP-2105 provides either: one external interrupt ($\overline{\text{IRQ2}}$) and one serial port (SPORT1), *or* three external interrupts ($\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$) with no serial port.

Clock Signals

The ADSP-21xx processors' CLKIN input may be driven by a crystal or by a TTL-compatible external clock signal. The CLKIN input may not be halted or changed in frequency during operation, nor operated below the specified low frequency limit.

If an external clock is used, it should be a TTL-compatible signal running at the instruction rate. The signal should be connected to the processor's CLKIN input; in this case, the XTAL input must be left unconnected.

Because the ADSP-21xx processors include an on-chip oscillator circuit, an external crystal may also be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 2. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

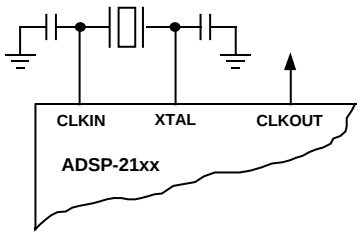

Figure 2. External Crystal Connections