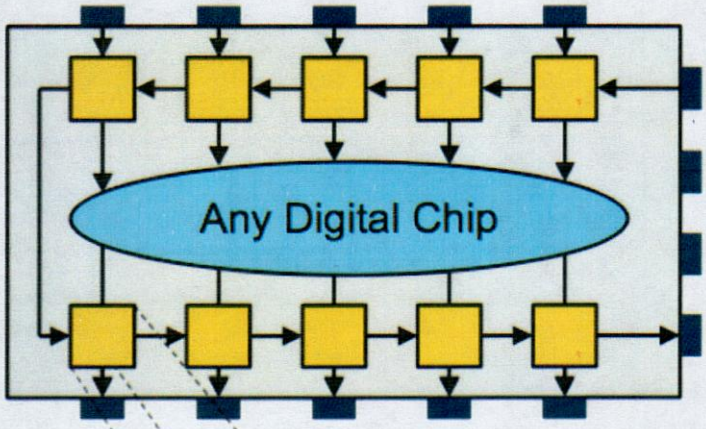
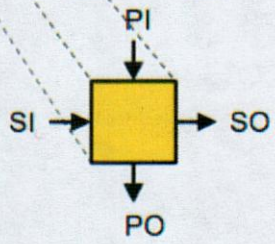
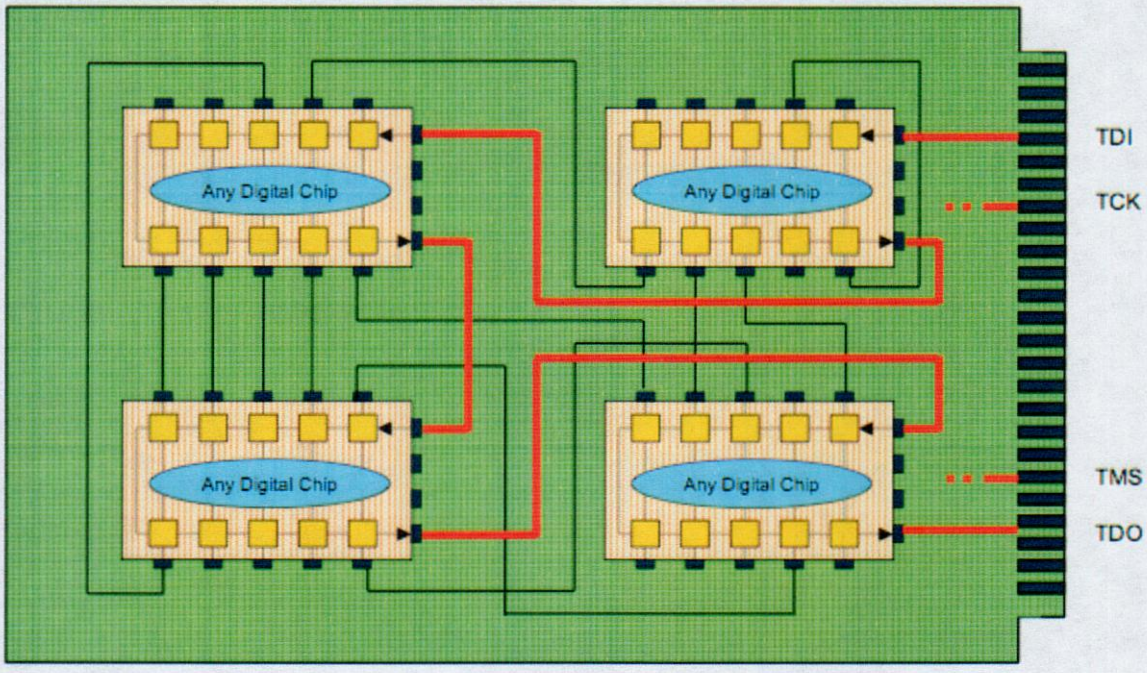




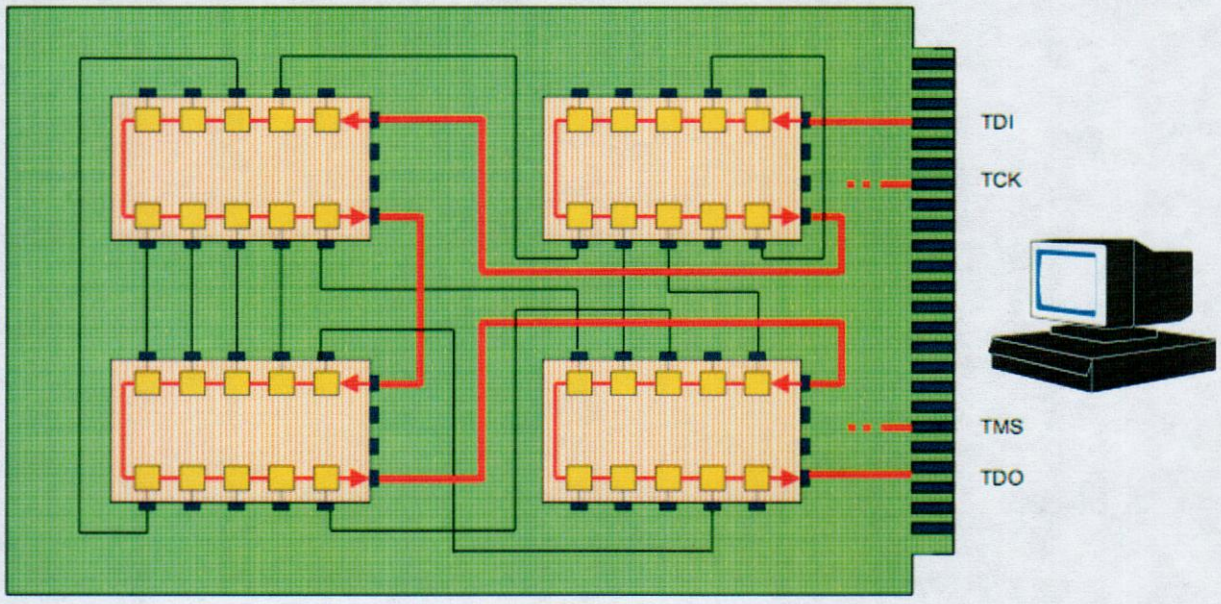
Each boundary-scan cell can:

- ☐ Capture data on its parallel input PI
- ☐ Update data onto its parallel output PO
- ☐ Serially scan data from SO to its neighbour's SI
- ☐ Behave transparently: PI passes to PO
- ☐ Note: all digital logic is contained inside the boundary-scan register

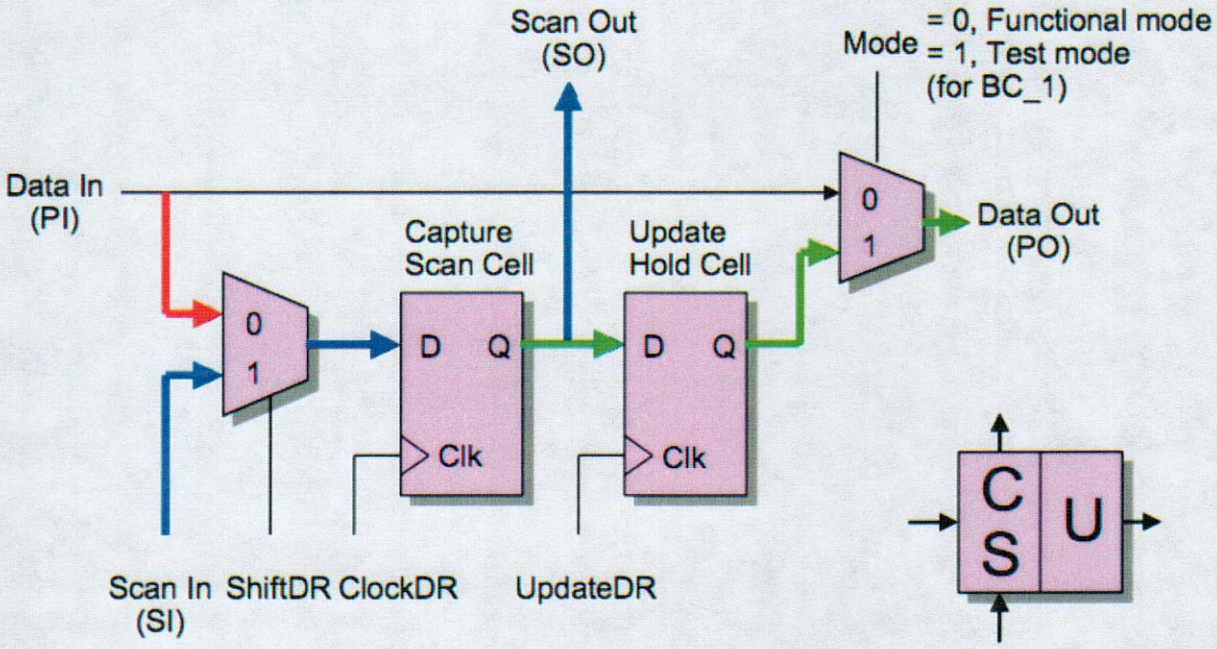
Using The Boundary-Scan Path



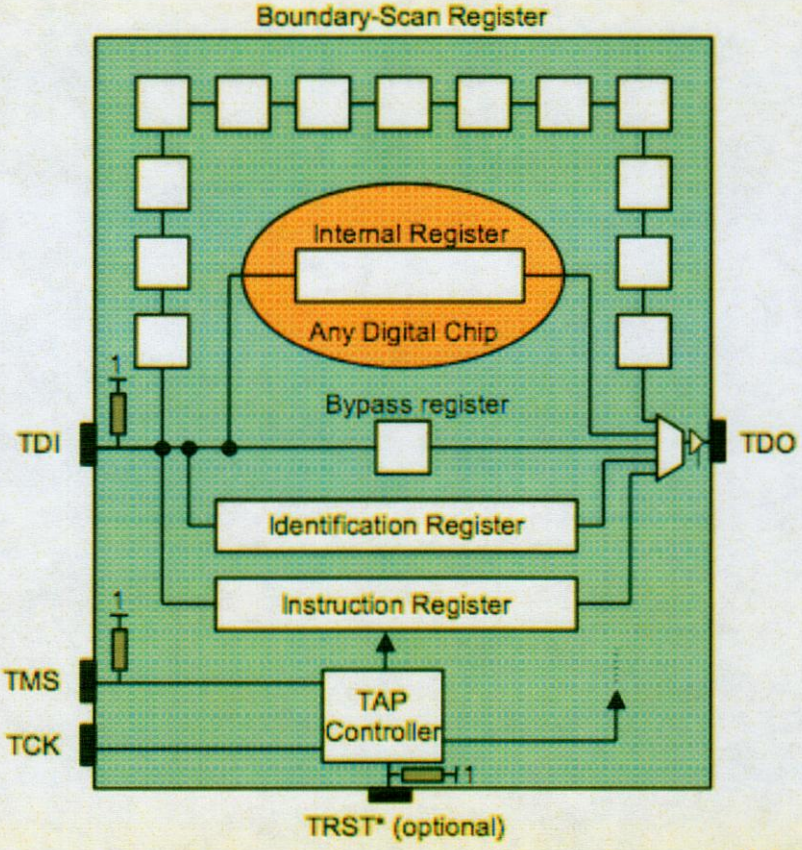
What The Tester Sees



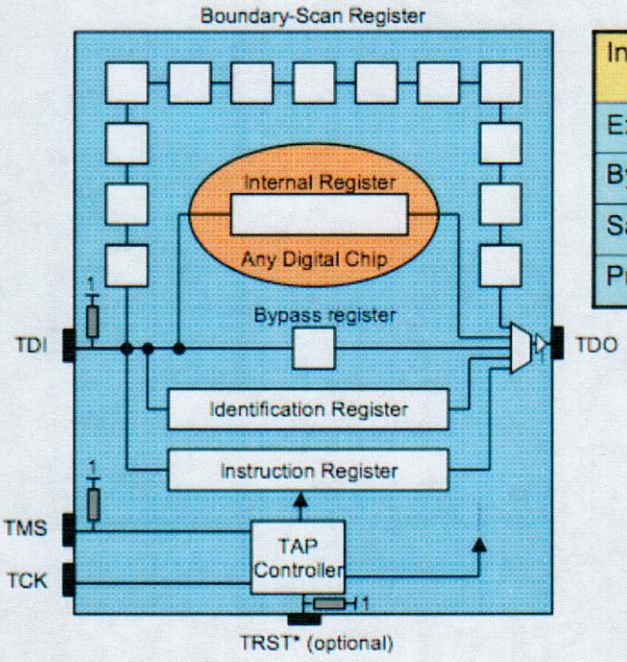
Basic Boundary-Scan Cell (BC_1)



1149.1 Chip Architecture



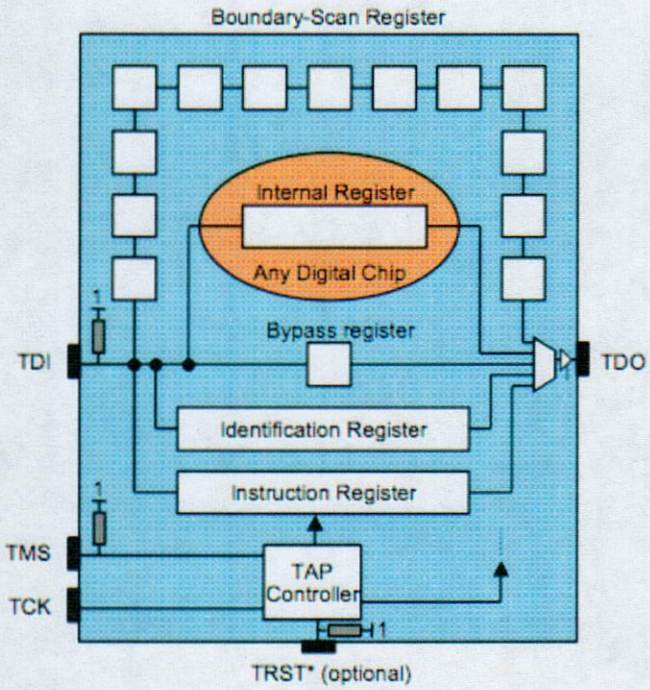
Mandatory Instructions and Reset Modes

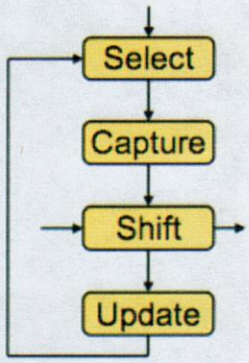


Instruction	Target (Active) Register	Code
Extest	Boundary Scan	Formerly All-0s
Bypass	Bypass	All-1s
Sample	Boundary Scan	Undefined
Preload	Boundary Scan	Undefined

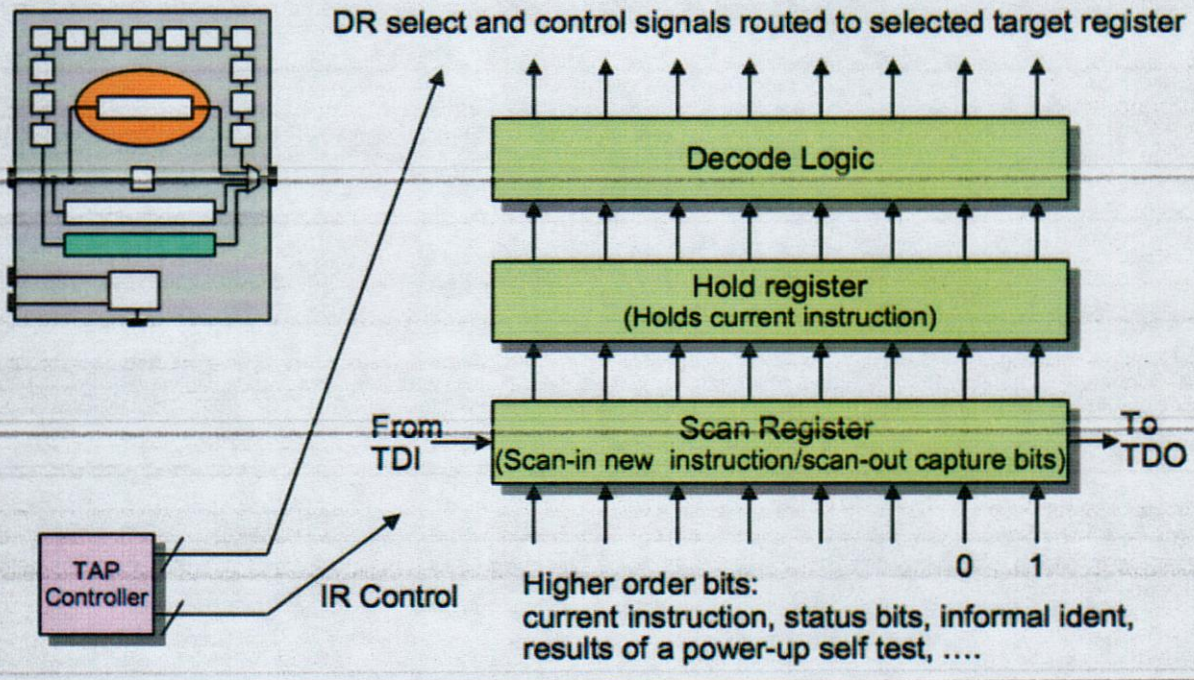
IR ≥ 2
Reset:
TMS = 1, 5 x TCK

Target Register Modes

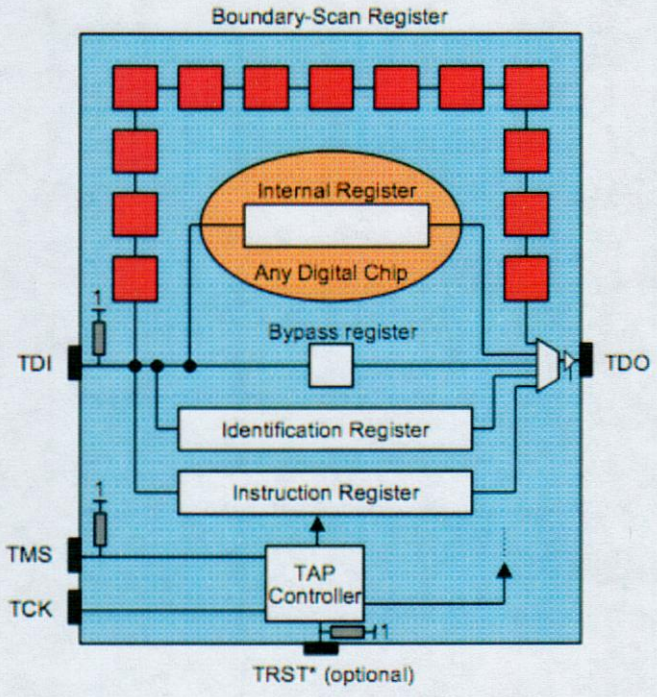




Instruction Register

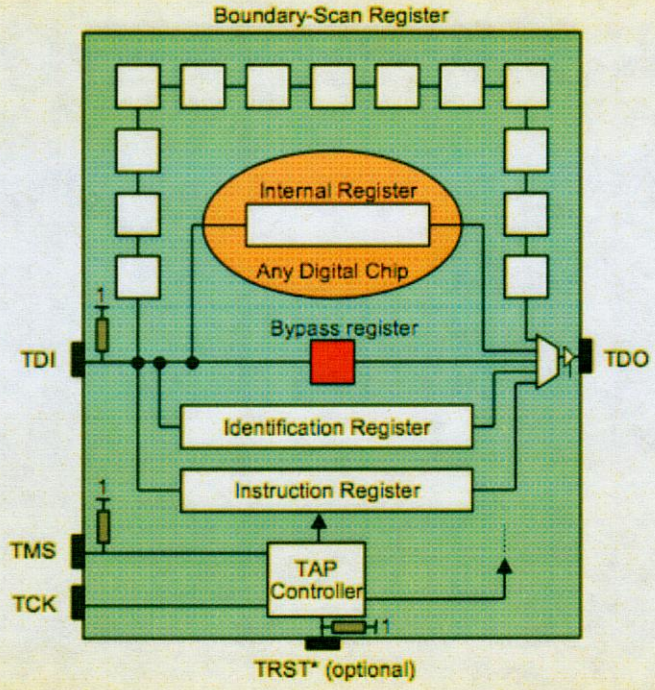


Extest Instruction



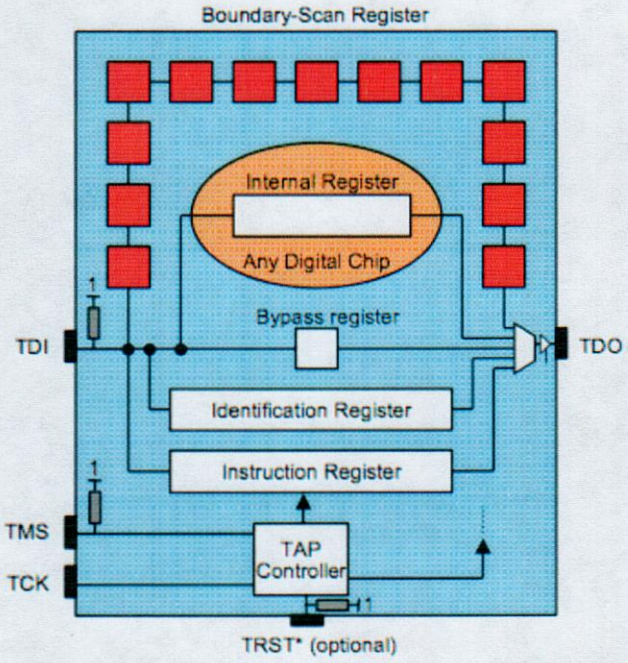
- Boundary-scan register selected
- Used to apply patterns to the interconnect structures on the board
- Boundary-scan cells have permission to write to their outputs (device in test mode)

Bypass Instruction



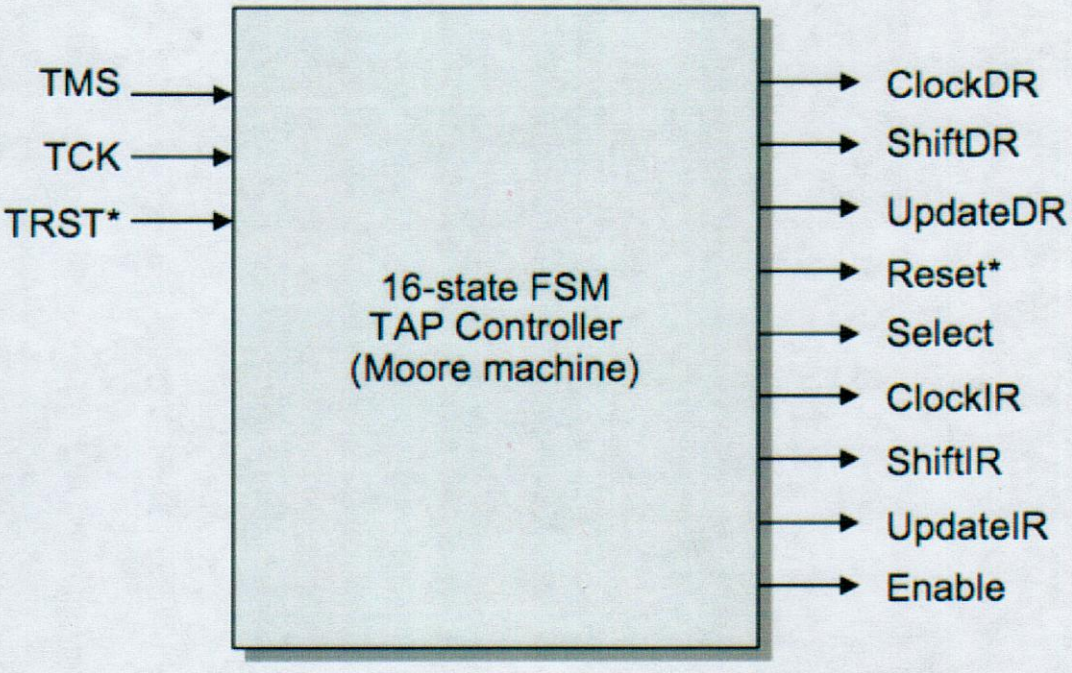
- Bypass register selected
- Used to allow quick passage through this device to another device connected in the chain

Sample and Preload Instruction

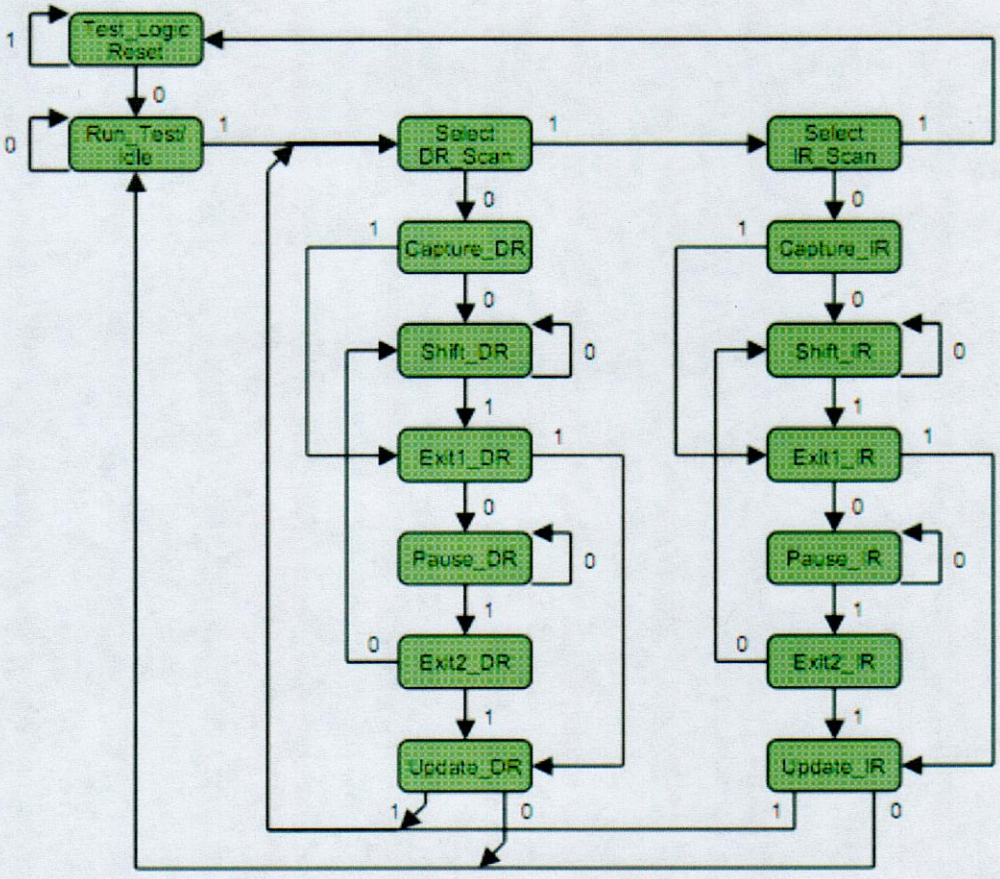


- Boundary scan register selected
- Used to Preload known values in the boundary scan cells.
- Also used to Sample (Capture) mission-mode signals into the boundary-scan cells
- Device in functional mode, not test mode

TAP Controller



TAP Controller State Diagram



Faults on a 4-Net Interconnect