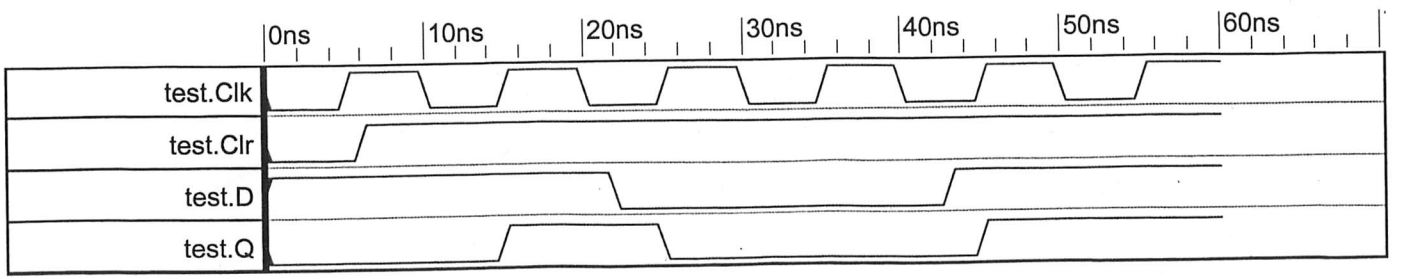
```
$date
      Sat May 10 16:02:30 2003

$end
$version
      VeriLogger 9.0g
$end
$timescale
      1 ps
$end


$scope module test $end
$var reg      1 !    Clk  $end
$var reg      1 "    Clr  $end
$var reg      1 #    D  $end
$var wire     1 $    Q  $end

$scope module gg $end
$var wire     1 %    d  $end
$var wire     1 &    clr  $end
$var wire     1 '    clk  $end
$var reg      1 (    q  $end
$upscope $end

$upscope $end

$enddefinitions      $end
$dumpvars
0(
0'
0&
1%
0$
1#
0"
0!
$end
#5000
1!
1'
#6000
1"
1&
#10000
0!
0'
#15000
1!
1'
1(
1$
#20000
0!
0'
#22000
0#
0%
#25000
1!
1'
0(
0$
#30000
0!
0'
#35000
1!
1'
#40000
0!
0'
#43000
1#
1%
#45000
1!
1'
1(
1$
#50000
0!
0'
#55000
1!
1'
```

testbench instantiated D-FF

= 5 ns
CLK = 1 (module test)
clk = 1 (module gg)

$dumpvars(0, test);



```
$date
      Sat May 10 16:06:36 2003

$end
$version
      VeriLogger 9.0g
$end
$timescale
      1 ps
$end


$scope module test $end
$var reg       1 !    Clk  $end
$var reg       1 "    Clr  $end
$var reg       1 #    D  $end
$var wire      1 $    Q  $end
$upscope $end

$enddefinitions      $end
$dumpvars
0$
1#
0"
0!
$end
#5000
1!
#6000
1"
#10000
0!
#15000
1!
1$
#20000
0!
#22000
0#
#25000
1!
0$
#30000
0!
#35000
1!
#40000
0!
#43000
1#
#45000
1!
1$
#50000
0!
#55000
1!
```

$dumpvars(1, test);