Tutorial of ALTERA Cyclone II FPGA Starter Board

This is a simple project which makes the LED and seven-segment display count from 0 to 9.

You will get familiar with Quartus II design software—You will understand basic design steps about Quartus II projects, such as designing projects using *schematic editor* and *HDL*, compiling your design, pin assignment, and downloading it into the FPGA board.

Procedures:

Create a Project:

1. Launch the Quartus II software, select **File → New Project Wizard → Next**;
2. Choose the Directory and name of the project:
    a. **Working directory**: Choose the E: where your flash disk will be.
    b. **Name of this project**: Type `counter`.
    c. **Name of the top-level design entity**: Type `counter_top`.
3. Click **Finish,** when prompted, choose **Yes;**

Assign the Device

4. Choose **Assignments → Device;**
5. Under **Family**, choose ***Cyclone II*;**
6. Under **Available devices**, choose **EP2C20F484C7;**
7. Click **OK;**

Design Entry

8. Choose **File → New → Block Diagram/Schematic File** to create a new file, Block1.bdf;
9. Click **OK**;
10. Choose **File → Save As** and enter the File name: `counter_top`;
11. Click **Save**;
12. Choose **File → New → Verilog HDL File** to create a new Verilog File.
13. Click **OK** to create a new file Verilog1.v;
14. Select **File → Save As** and enter the File name: `counter`;
15. Copy the Verilog HDL code from **decade.v** (Verilog source file along with this tutorial) into the blank counter.v file;
16. Save the file by choosing **File → Save**;
17. Choose **File → Create/Update → Create Symbol Files for Current File** to convert the counter.v file to a Symbol File (.sym). You use this Symbol File to add the HDL code to your BDF schematic;
18. Click **Ok**;
19. To add the counter.v symbol to the top-level design, click the **counter_top.bdf** tab;
20. Choose **Edit → Insert Symbol**;
21. Double-click the **Project** directory to expand it;
22. Select **Decade**, which is module name of created symbol;
23. Click **Ok**;
24. Move the cursor to the BDF grid Click to place the counter symbol onto the BDF.
25. Add an input pin and an output bus with the following steps:

a. Choose **Edit → Insert Symbol**;
b. Under **Libraries**, select **quartus/libraries > primitives > pin > input**;
c. Click **OK**;
d. Place the input symbol to the BDF grid, move the symbol so that it is touching the **CLK** input to the **Decade** symbol;
e. Use the mouse to click and drag the new input pin to the left; notice that the ports remain connected;
f. Change the pin name by double-clicking `pin_name`;

26. Do the same procedures as 25.a to 25.f to add input and output pins to other ports. Select **quartus/libraries > primitives > pin > output** for output pins;
27. When rename the output port 'digit', remember to enter `digit[6..0],` which means they have 7 pins.
28. When rename the output port 'Q, remember to enter `Q[3..0],` which means they have 4 pins.
29. Save the file by choosing **File → Save**;

Pin Assign

30. Choose **Processing → Start → Start Analysis & Elaboration** in preparation for assigning pin locations;
31. Click **OK** in the message window that appears after analysis and elaboration completes;
32. Choose **Assignments → Pins**, which opens the Pin Planner, a spreadsheet-like table of specific pin assignments. The Pin Planner shows the design's pins.
33. In the **Location** column next to each of the node names, add the coordinates (pin numbers) for the actual values to use with the board. For the pin layout of components on the Board, please refer to Appendix A;

Compile Your Project

34. In the **Processing** menu, choose **Start Compilation**, If you are asked to save changes to your BDF, click **Yes**;
35. When compilation is complete, the Quartus II software displays a message. Click **OK** to close the message box.

Program the Device

36. Choose **Tools → Programmer**. The Programmer window opens.
37. Connect the USB Cable from the Computer to the FPGA Board;
38. Set the **RUN/PROG** switch (SW12) to the **RUN** position;
39. Turn the board on using the on/off switch (SW11)Power;
40. Click **Start**. The file downloads to the development board.

Congratulations, you have created, compiled, and programmed your design!
If everything is Ok, you will see the LEDs and 7-Segment show the count sequence from 0 to 9.

For further development, please refer to the following documents:
UserGuide: http://www.altera.com/literature/ug/ug_cii_starter_board.pdf
Pin Assignment: http://www.altera.com/literature/manual/mnl_cii_starter_board_rm.pdf
Schematic: http://www.altera.com/products/devkits/altera/documents/cy2_fpga_starter_board_schematic.pdf

Appendix A: Pin Connections on FPGA Board

Table 2–9. Clock Circuit FPGA Pin Connections

Signal Name	FPGA Pin	Description
CLOCK_27	PIN_D12	27 MHz clock input
CLOCK_50	PIN_L1	50 MHz clock input
CLOCK_24	PIN_B12	24 MHz clock input from USB Blaster
EXT_CLOCK	PIN_M21	External (SMA) clock input

Table 2–10. Push Button Switch FPGA Pin Connections

Switch	FPGA Pin	Description
KEY[0]	PIN_R22	Pushbutton[0]
KEY[1]	PIN_R21	Pushbutton[1]
KEY[2]	PIN_T22	Pushbutton[2]
KEY[3]	PIN_T21	Pushbutton[3]

Table 2–11. Toggle Switch FPGA Pin Connections

Switch	FPGA Pin	Description
SW[0]	PIN_L22	Toggle Switch[0]
SW[1]	PIN_L21	Toggle Switch[1]
SW[2]	PIN_M22	Toggle Switch[2]
SW[3]	PIN_V12	Toggle Switch[3]
SW[4]	PIN_W12	Toggle Switch[4]
SW[5]	PIN_U12	Toggle Switch[5]
SW[6]	PIN_U11	Toggle Switch[6]
SW[7]	PIN_M2	Toggle Switch[7]
SW[8]	PIN_M1	Toggle Switch[8]
SW[9]	PIN_L2	Toggle Switch[9]

Table 2–12. LED FPGA Pin Connections

Signal Name	FPGA Pin	Description
LEDR[0]	PIN_R20	LED Red[0]
LEDR[1]	PIN_R19	LED Red[1]
LEDR[2]	PIN_U19	LED Red[2]
LEDR[3]	PIN_Y19	LED Red[3]
LEDR[4]	PIN_T18	LED Red[4]
LEDR[5]	PIN_V19	LED Red[5]
LEDR[6]	PIN_Y18	LED Red[6]
LEDR[7]	PIN_U18	LED Red[7]
LEDR[8]	PIN_R18	LED Red[8]
LEDR[9]	PIN_R17	LED Red[9]
LEDG[0]	PIN_U22	LED Green[0]
LEDG[1]	PIN_U21	LED Green[1]
LEDG[2]	PIN_V22	LED Green[2]
LEDG[3]	PIN_V21	LED Green[3]
LEDG[4]	PIN_W22	LED Green[4]
LEDG[5]	PIN_W21	LED Green[5]
LEDG[6]	PIN_Y22	LED Green[6]
LEDG[7]	PIN_Y21	LED Green[7]

Table 2–13. Seven-Segment Display FPGA Pin Connections (Part 1 of 2)

Signal Name	FPGA Pin	Description
HEX0[0]	PIN_J2	Seven-Segment segment 0[0]
HEX0[1]	PIN_J1	Seven-Segment segment 0[1]
HEX0[2]	PIN_H2	Seven-Segment segment 0[2]
HEX0[3]	PIN_H1	Seven-Segment segment 0[3]
HEX0[4]	PIN_F2	Seven-Segment segment 0[4]
HEX0[5]	PIN_F1	Seven-Segment segment 0[5]
HEX0[6]	PIN_E2	Seven-Segment segment 0[6]
HEX1[0]	PIN_E1	Seven-Segment segment 1[0]
HEX1[1]	PIN_H6	Seven-Segment segment 1[1]

Table 2–13. Seven-Segment Display FPGA Pin Connections (Part 2 of 2)

Signal Name	FPGA Pin	Description
HEX1[2]	PIN_H5	Seven-Segment segment 1[2]
HEX1[3]	PIN_H4	Seven-Segment segment 1[3]
HEX1[4]	PIN_G3	Seven-Segment segment 1[4]
HEX1[5]	PIN_D2	Seven-Segment segment 1[5]
HEX1[6]	PIN_D1	Seven-Segment segment 1[6]
HEX2[0]	PIN_G5	Seven-Segment segment 2[0]
HEX2[1]	PIN_G6	Seven-Segment segment 2[1]
HEX2[2]	PIN_C2	Seven-Segment segment 2[2]
HEX2[3]	PIN_C1	Seven-Segment segment 2[3]
HEX2[4]	PIN_E3	Seven-Segment segment 2[4]
HEX2[5]	PIN_E4	Seven-Segment segment 2[5]
HEX2[6]	PIN_D3	Seven-Segment segment 2[6]
HEX3[0]	PIN_F4	Seven-Segment segment 3[0]
HEX3[1]	PIN_D5	Seven-Segment segment 3[1]
HEX3[2]	PIN_D6	Seven-Segment segment 3[2]
HEX3[3]	PIN_J4	Seven-Segment segment 3[3]
HEX3[4]	PIN_L8	Seven-Segment segment 3[4]
HEX3[5]	PIN_F3	Seven-Segment segment 3[5]
HEX3[6]	PIN_D4	Seven-Segment segment 3[6]