Product Bulletin

Boundary-Scan Logic

Fully compliant with IEEE Std 1149.1 (JTAG)

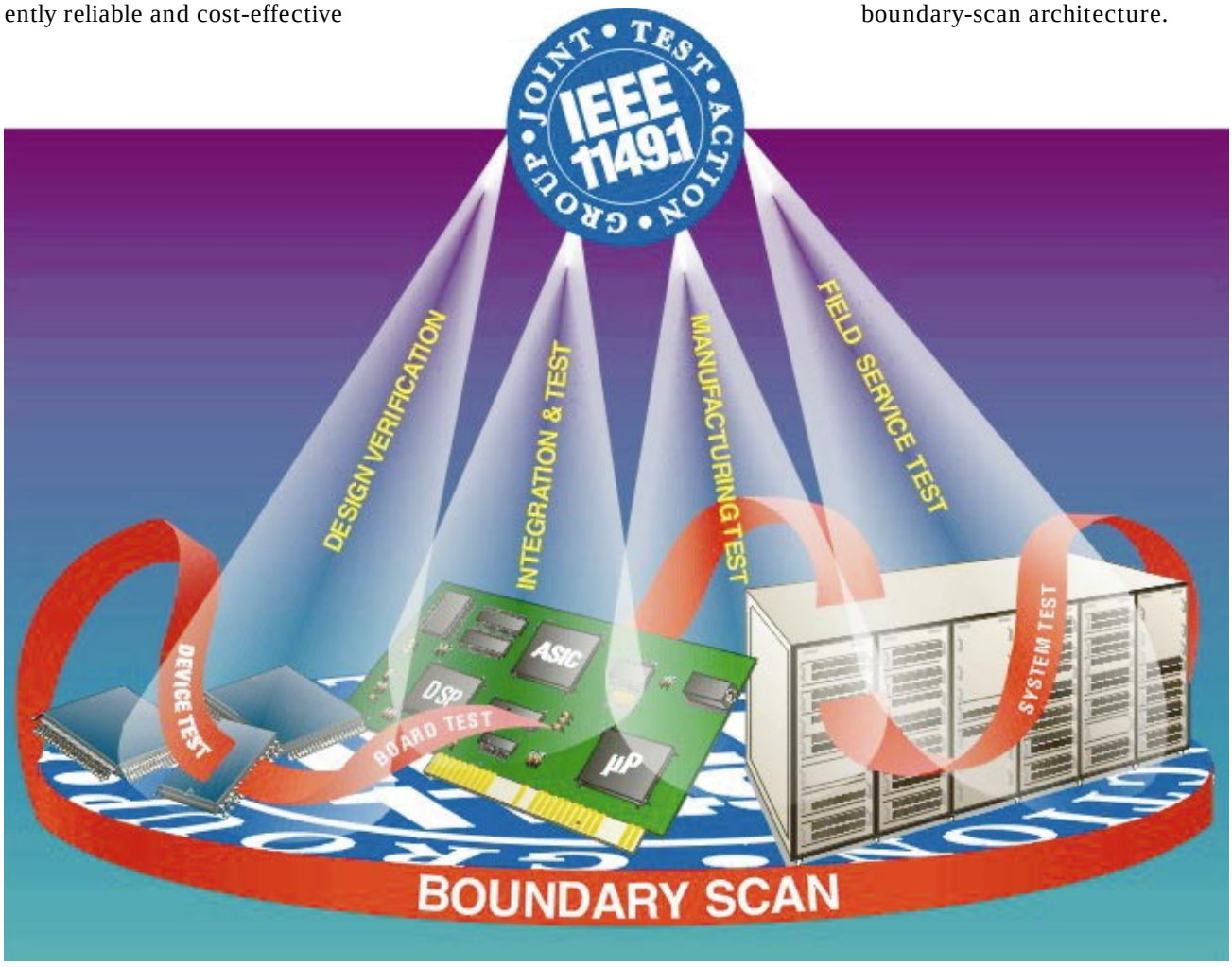
Key Benefits

- Provides controllability and observability without physical access
- Reduces number of test points needed on PCB
- Reduces number of pins needed for "Bed-of-Nails" testers
- Eliminates need for In-Circuit Test (ICT) models for JTAG parts
- Allows for quick identification and isolation of defects
- Industry standard ensures inter-operability between vendors

Introduction

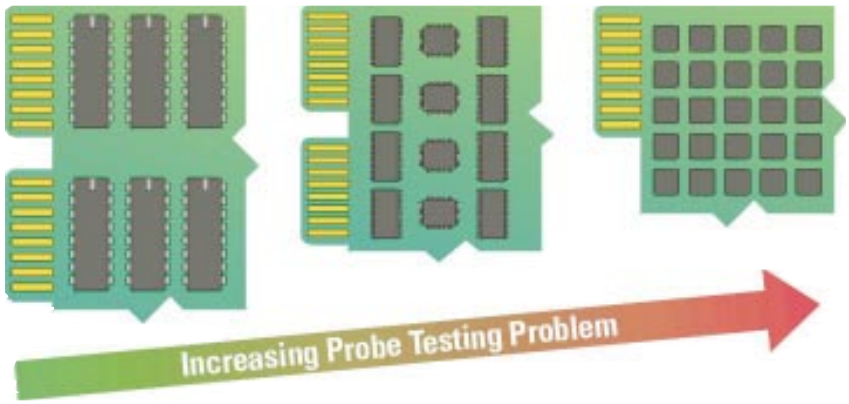
In today's complex systems, testability is an increasing concern in almost every application and in every area of application development. Manufacturers that thoroughly address the issue of testability at the device, board, and system levels deliver more consistently reliable and cost-effective products to the marketplace. This means building in test capabilities in every phase of development and deployment, including design verification, hardware and software integration, manufacturing, and in the field. OEMs that do not design systems with full testability in mind open themselves to increased possibility of product failures, reduced time-to-market and missed market opportunities.

Texas Instruments leads the industry with the widest array of catalog logic products that implement IEEE Std 1149.1 (JTAG) boundary-scan architecture.



TI offers off-the-shelf JTAG-compliant devices that can virtually eliminate traditional probe testing at the device, board and system levels.

TI Boundary-Scan Logic (BSL) devices serve as off-the-shelf building blocks for designers to add boundary-scan test capability at the board and system levels. With more than 40 released JTAG-enabled devices, including more than 20 Widebus™ devices, octal bus interface devices, scan-support devices, and a line of Universal Bus Transceivers (UBT™) that can replace more than 50 bus interface functions, TI BSL products address most any design need. In addition, they also come in innovative and space-saving package configurations.

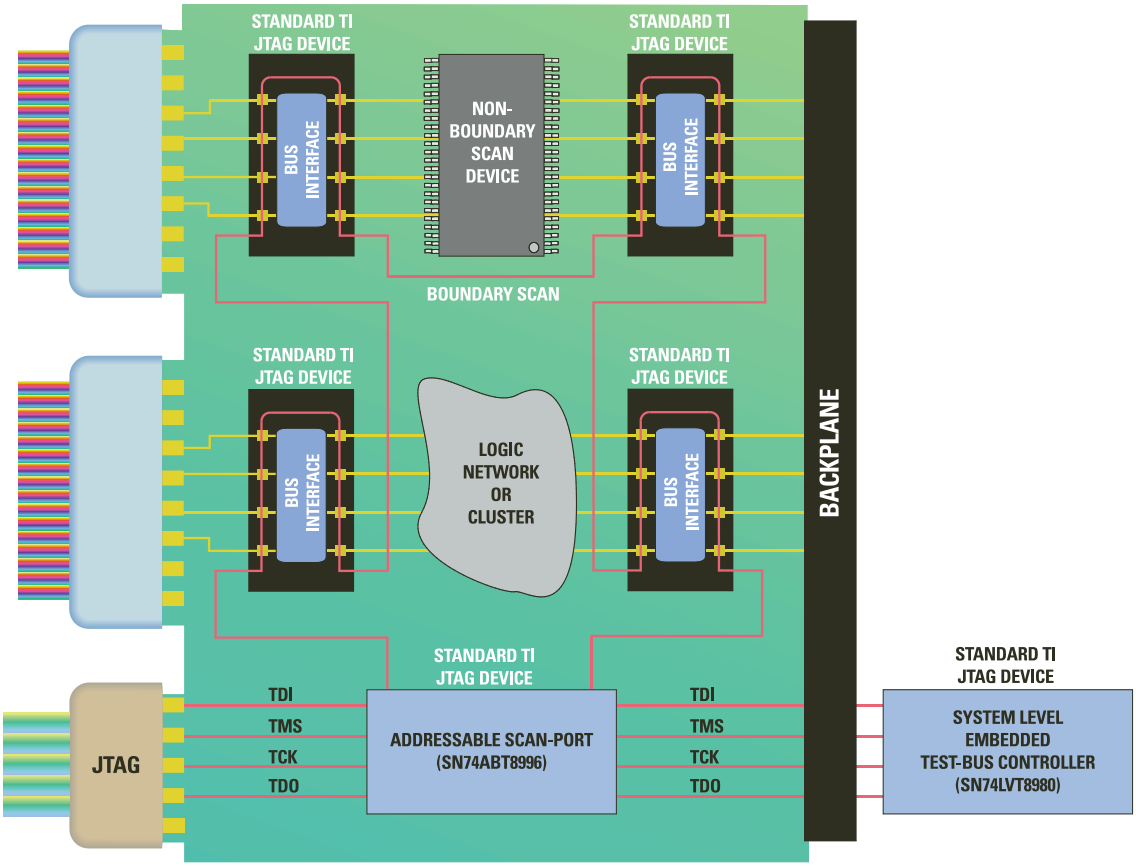


Today's highly integrated multilayer boards with fine-pitch ICs are virtually impossible to access physically for test.

Adding Boundary-Scan Logic from TI

Today's highly integrated multilayer boards with fine-pitch ICs are virtually impossible to access physically for test. Traditional board test methods include functional test, which only accesses the board's primary I/Os, providing limited coverage and poor diagnostics for board-network faults. In-circuit test, another traditional test method, works by physically accessing each wire on the board via costly "bed of nails" probes and testers.

JTAG-enabled BSL devices from TI eliminate the need for these ineffective test methods with built-in boundary-scan circuitry. Designers can use catalog JTAG functions where bus interfaces are normally required to augment boundary-scan test coverage and partition the board/system function at critical interfaces (such as CPU/DSP/memory). Alternatively, these devices may be added expressly to build test capability around a specific non-boundary-scan device



Standard JTAG bus-interface and scan-support logic from TI enable boundary-scan testing techniques to be applied to any functional level even when the primary logic cluster or device is not JTAG-compliant.

or logic cluster. Furthermore, TI's catalog scan-support devices enable system-level interconnection and control of board-level JTAG test ports. Using these devices, designers can take boundary-scan test functionality from device, to board, to system level. The net result is freedom from constraints of physical test access at all phases of product deployment.

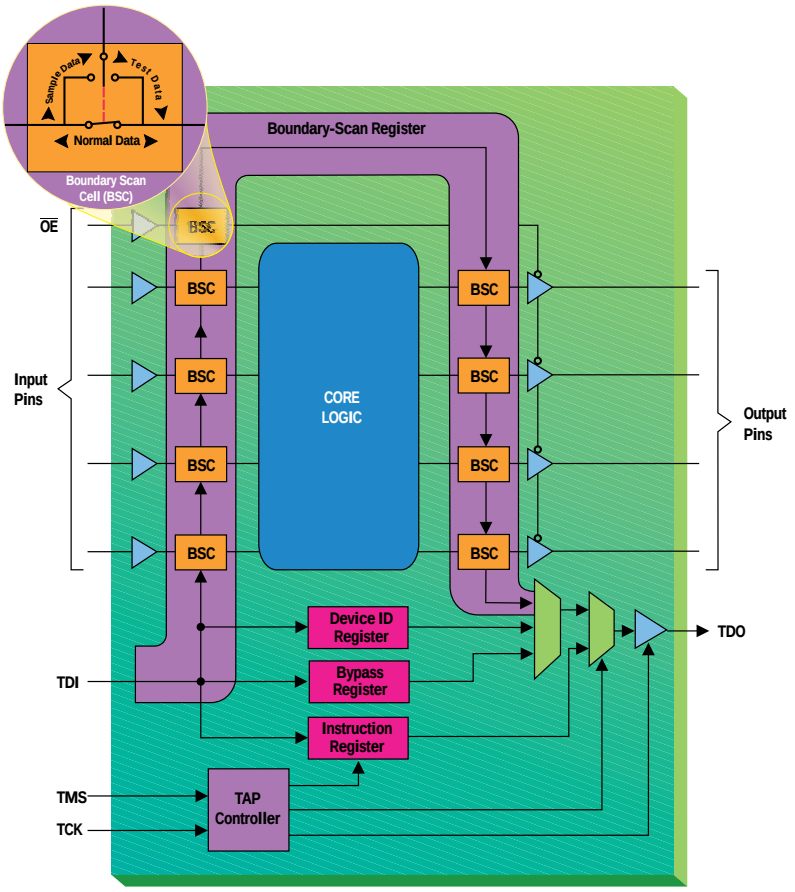
How Boundary Scan Works

Boundary scan is a special type of scan path that consists of a series of test cells added at every I/O pin on a device. The resulting boundary-scan register and other test features of the device are accessed through a standard interface—the JTAG Test Access Port (TAP).

At the device level, the JTAG TAP allows for access to standard chip internal test facilities such as internal scan path, Built-in Self Test (BIST), and built-in emulation and debug. The chip internal scan path involves the substitution of normal storage elements (latches and flip-flops) with scannable counterparts that can be serially interconnected for test purposes. BIST uses on-chip stimulus generators and response monitors to eliminate the need for test pattern generation.

JTAG is ideally suited for board-level testing since the boundary-scan registers of compliant devices provide access to control and observe board-level nodes/networks. Naturally, with more devices on a board that include JTAG, test coverage and diagnostic facility are consequently improved. However, even where some devices on a board do not include JTAG, JTAG access to many nodes still can be used effectively in place of physical probes.

Using JTAG at the system level allows for higher integration of the whole system. The standard TAP enables system hardware debug and hardware/software integration while chips and boards are still in their normal



Boundary-scan architecture uses a boundary-scan cell (BSC) at every I/O pin which can interrupt normal data, sample data and inject test data according to the IEEE 1149.1 instruction set.

system configuration and operating environment. Furthermore, this built-in access can be reused in fielded systems for in-service test and maintenance.

The obvious benefit offered by the boundary-scan technique is fault isolation at the printed circuit node/network level. This level of isolation is a common requirement in telecommunications switching or similar environments where prompt field repair is critical.

Boundary-Scan Architecture

The boundary-scan register cells (BSCs) are interconnected to form a scan path between a test data input (TDI) pin and a test data output (TDO) pin. During normal IC operations, input and output signals pass freely through each BSC, from the normal data input (NDI), to the normal data output (NDO). However, when the boundary-test mode is entered, the IC's boundary is controlled in such a way that test stimulus can be shifted in (at TDI) and applied from each BSC output, and test response can be captured at each BSC input and shifted out (at TDO) for inspection. External testing of wiring interconnects and neighboring ICs on a board assembly is accomplished by applying test stimulus from the output BSCs and capturing test response at the input BSCs. As an option, internal testing of the IC core logic can be accomplished by applying test stimulus from the input BSCs and capturing test response at the output BSCs.

The complete test architecture consists of the boundary-scan register (highlighted), a one-bit bypass register, an optional device identification register, other optional user data register(s), a single instruction register, and the JTAG TAP controller.

Three Required Instructions (IEEE Std 1149.1)

IEEE Std 1149.1 defines nine test instructions. Of the nine instructions, three are required and six are optional.

BYPASS

The required BYPASS instruction allows the IC to remain in a normal functional mode and selects the one-bit bypass register to be connected between TDI and TDO. The BYPASS instruction allows serial data to be transferred through the IC from TDI to TDO without affecting the operation of the IC.

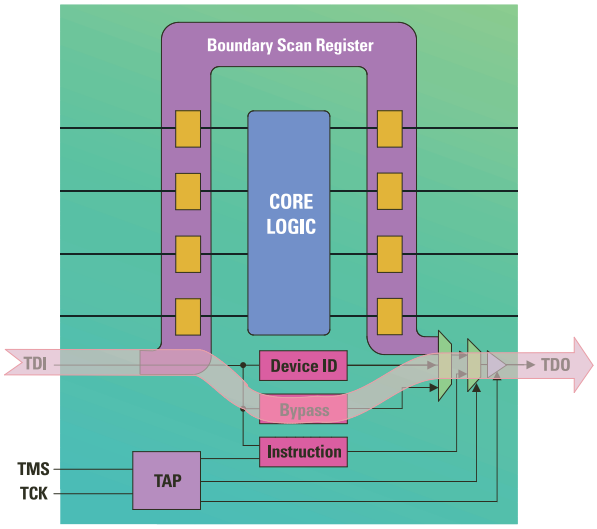
SAMPLE/PRELOAD

The required SAMPLE/PRELOAD instruction allows the IC to remain in a normal functional mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register can be accessed via a data scan operation, to take a sample of the functional data entering and leaving the IC. This instruction is also used to preload test data into the boundary-scan register before loading an EXTEST instruction.

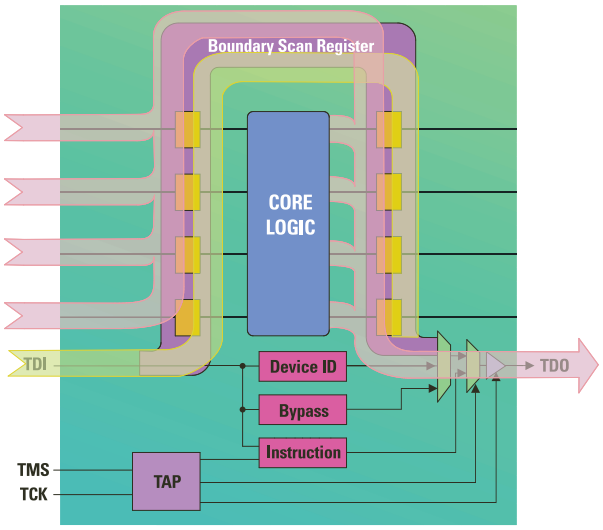
EXTEST

The required EXTEST instruction places the IC into an external boundary-test mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register is accessed to drive test data off-chip via the boundary outputs and receive test data off-chip via the boundary inputs. As such, the EXTEST instruction is the workhorse of IEEE Std 1149.1, providing for probe-less testing of solder-joint opens/shorts and of logic cluster function.

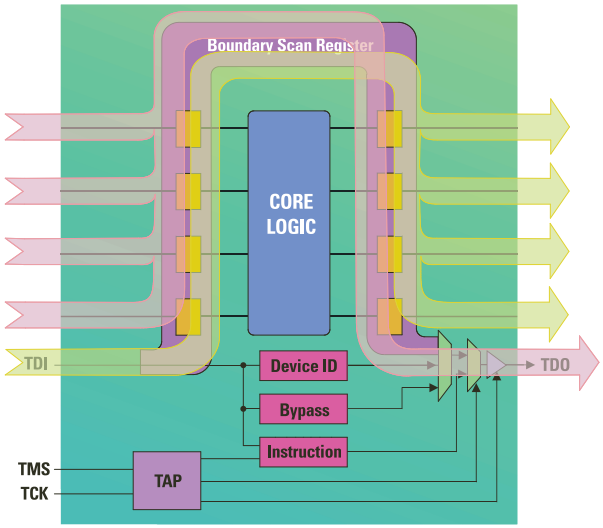
BYPASS Instruction



SAMPLE/PRELOAD Instruction



EXTEST Instruction



Six Optional Instructions (IEEE Std 1149.1)

INTEST

The optional INTEST instruction places the IC in an internal boundary-test mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register is accessed to drive test data on-chip via the boundary inputs and receive test data on chip via the boundary outputs.

RUNBIST

The optional RUNBIST instruction places the IC in a self-test mode, enables a comprehensive self-test of the IC's core logic, and selects a user-specified data register to be connected between TDI and TDO. During this instruction, the boundary outputs are controlled so that external signals cannot interfere with neighboring ICs during the RUNBIST operation.

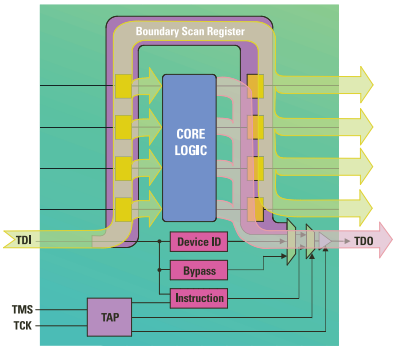
CLAMP

The optional CLAMP instruction sets the outputs of an IC to logic levels determined by the contents of the boundary-scan register and selects the one-bit bypass register to be connected between TDI and TDO. Before loading this instruction, the contents of the boundary-scan register can be preset with the SAMPLE/PRELOAD instruction. During this instruction, data can be shifted through the bypass register from TDI to TDO without affecting the condition of the outputs.

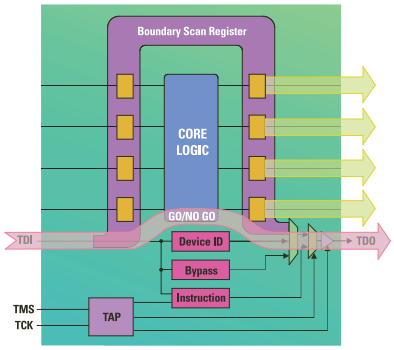
HIGHZ

The optional HIGHZ instruction sets all outputs (including two-state as well as three-state types) of an IC to a disabled (high-impedance) state and selects the one-bit bypass register to be connected between TDI and TDO. During this instruction, data can be shifted through the bypass register from TDI to TDO without affecting the condition of the IC outputs.

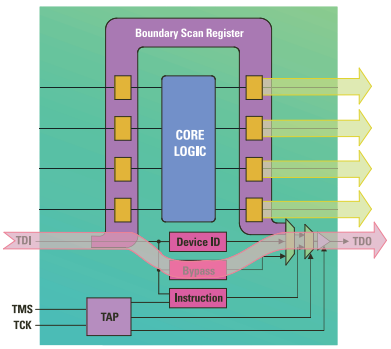
INTEST Instruction



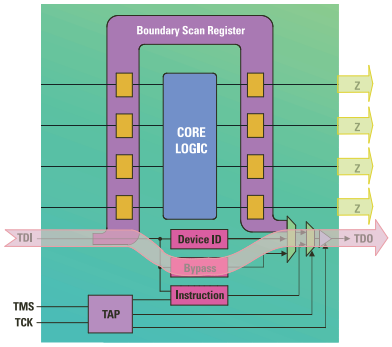
RUNBIST Instruction



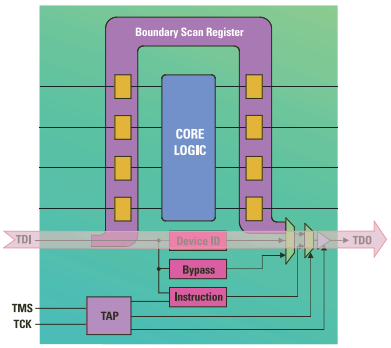
CLAMP Instruction



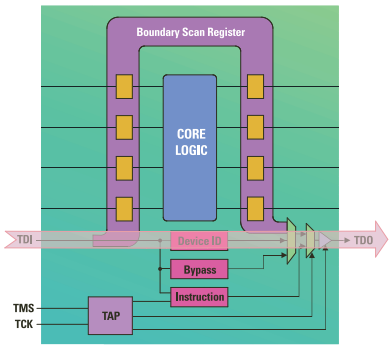
HIGHZ Instruction



IDCODE Instruction



USERCODE Instruction



IDCODE

The optional IDCODE instruction allows the IC to remain in its functional mode and selects the optional device identification register to be connected between TDI and TDO. The device identification register is a 32-bit shift register containing information regarding the IC manufacturer, device type, and version code. Accessing the device identification register does not interfere with the operation of the IC. Also, access to the device identification register should be immediately available, via a TAP data-scan operation, after power-up of the IC or after the TAP has been reset using the optional TRST pin or by otherwise moving to the Test-Logic-Reset state.

USERCODE

The optional USERCODE instruction allows the IC to remain in its functional mode and selects the device identification register to be connected between TDI and TDO. During the USERCODE instruction, the optional 32-bit device identification register captures user-defined information about the IC. Accessing the device identification register does not interfere with the operation of the IC.

With the industry's widest selection of JTAG-enabled devices, TI is the industry's choice for boundary-scan logic. The chart below lists all of TI's BSL devices and their functional description.

Widebus™ Interface Devices

Part Number	Function	Bits	Max t_{pd} (ns)	Packages
Advanced BiCMOS (ABT) Family—5V V_{CC}, High-Drive Outputs (64 mA I_{OL}/–32 mA I_{OH}), Low Noise				
SN74ABT18245A	Transceiver	18	5.4	56-pin SSOP (DL), TSSOP (DGG)
SN74ABT18640	Inverting Transceiver	18	5.4	56-pin SSOP (DL), TSSOP (DGG)
SN74ABTH18502A	Universal Bus Transceiver (UBT™)	18	5.5	64-pin TQFP (PM)
SN74ABTH182502A	Universal Bus Transceiver (UBT)	18	6.2	64-pin TQFP (PM)
SN74ABTH18504A	Universal Bus Transceiver (UBT)	20	5.5	64-pin TQFP (PM)
SN74ABTH182504A	Universal Bus Transceiver (UBT)	20	6.2	64-pin TQFP (PM)
SN74ABTH18646A	Registered Transceiver	18	5.4	64-pin TQFP (PM)
SN74ABTH182646A	Registered Transceiver	18	6.1	64-pin TQFP (PM)
SN74ABTH18652A	Registered Transceiver	18	5.4	64-pin TQFP (PM)
SN74ABTH182652A	Registered Transceiver	18	6.1	64-pin TQFP (PM)
Low-Voltage BiCMOS Technology (LVT) Family—3.3V V_{CC}, High-Drive Outputs (64 mA I_{OL}/–32 mA I_{OH})				
SN74LVTH18502A	Universal Bus Transceiver (UBT)	18	4.9	64-pin TQFP (PM)
SN74LVTH182502A	Universal Bus Transceiver (UBT)	18	5.7	64-pin TQFP (PM)
SN74LVTH18504A	Universal Bus Transceiver (UBT)	20	5.1	64-pin TQFP (PM)
SN74LVTH182504A	Universal Bus Transceiver (UBT)	20	5.9	64-pin TQFP (PM)
SN74LVT18512	Universal Bus Transceiver (UBT)	18	4.9	64-pin TSSOP (DGG)
SN74LVTH18512	Universal Bus Transceiver (UBT)	18	4.9	64-pin TSSOP (DGG)
SN74LVTH182512	Universal Bus Transceiver (UBT)	18	5.7	64-pin TSSOP (DGG)
SN74LVTH18514	Universal Bus Transceiver (UBT)	20	5.1	64-pin TSSOP (DGG)
SN74LVTH18646A	Registered Transceiver	18	4.7	64-pin TQFP (PM)
SN74LVTH182646A	Registered Transceiver	18	5.6	64-pin TQFP (PM)
SN74LVTH18652A	Registered Transceiver	18	4.7	64-pin TQFP (PM)
SN74LVTH182652A	Registered Transceiver	18	5.6	64-pin TQFP (PM)
Low-Voltage BiCMOS Technology (LVT) Proposed Devices				
SN74LVTH182514	Universal Bus Transceiver (UBT)	20	5.9	64-pin TSSOP (DGG)
SN74LVTH18516	Universal Bus Transceiver (UBT)	18	5.1	64-pin TSSOP (DGG)
SN74LVTH182516	Universal Bus Transceiver (UBT)	18	5.9	64-pin TSSOP (DGG)

Octal Bus Interface Devices

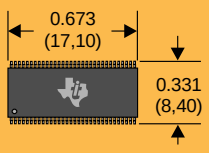
Part Number	Function	Bits	Max t_{pd} (ns)	Packages
Advanced BiCMOS (ABT) Family—5V V_{CC}, High-Drive Outputs (64 mA I_{OL}/–32 mA I_{OH}), Low Noise				
SN74ABT8245	Transceiver	8	5.1	24-pin SOIC (DW)
SN74ABT8543	Latched Transceiver	8	5.5	28-pin SOIC (DW), SSOP (DL)
SN74ABT8646	Registered Transceiver	8	5.5	28-pin SOIC (DW), SSOP (DL)
SN74ABT8652	Registered Transceiver	8	5.5	28-pin SOIC (DW), SSOP (DL)
SN74ABT8952	Registered Transceiver with CLKEN	8	6.3	28-pin SOIC (DW), SSOP (DL)
BiCMOS Technology Family—5V V_{CC}, High-Drive Outputs (64 mA I_{OL}/–15 mA I_{OH})				
SN74BCT8240A	Inverting Buffer/Driver	8	9	24-pin SOIC (DW)
SN74BCT8244A	Buffer/Driver	8	8.5	24-pin SOIC (DW)
SN74BCT8245A	Transceiver	8	10	24-pin SOIC (DW)
SN74BCT8373A	Bus Latch	8	9.5	24-pin SOIC (DW)
SN74BCT8374A	Bus Flip-Flop	8	10	24-pin SOIC (DW)

Scan-Support Devices

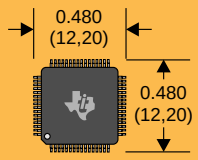
Part Number	Function	Packages
SN74LVT8980	Embedded Test Bus Controller	24-pin SOIC (DW)
SN74ACT8990	Test Bus Controller	44-pin PLCC (FN)
SN74ACT8994	Digital Bus Monitor	28-pin PLCC (FN)
SN74ABT8996	Addressable Scan Port	24-pin SOIC (DW), TSSOP (PW)
SN74ACT8997	Scan Path Linker	28-pin SOIC (DW)
SN74ACT8999	Scan Path Selector	28-pin SOIC (DW)
Proposed Devices		
SN74LVT8996	Addressable Scan Port	24-pin SOIC (DW), TSSOP (PW)
SN74LVT8980A	Embedded Test Bus Controller	24-pin SOIC (DW)

Space-saving Package Options for Boundary-Scan Logic Devices

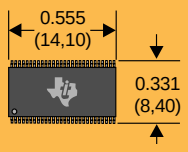
64-pin
Shrink Widebus™
TSSOP (DGG)
Lead pitch = 0.020 (0,50)
Height = 0.047 (1,20)
Area = 0.223 (144)



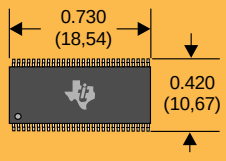
64-pin
TQFP (PM)
Lead pitch = 0.020 (0,50)
Height = 0.063 (1,60)
Area = 0.230 (149)



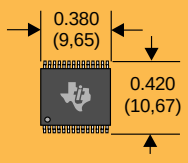
56-pin
Shrink Widebus
TSSOP (DGG)
Lead pitch = 0.020 (0,50)
Height = 0.047 (1,20)
Area = 0.184 (118)



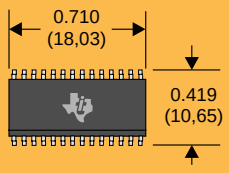
56-pin Widebus
SSOP (DL)
Lead pitch = 0.025 (0,635)
Height = 0.110 (2,79)
Area = 0.307 (198)



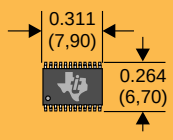
28-pin
SSOP (DL)
Lead pitch = 0.025 (0,635)
Height = 0.110 (2,79)
Area = 0.160 (103)



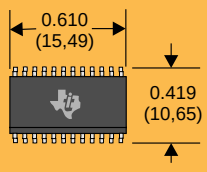
28-pin
SOIC (DW)
Lead pitch = 0.050 (1,27)
Height = 0.104 (2,65)
Area = 0.297 (192)



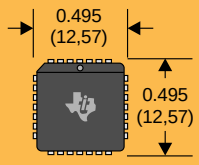
24-pin
TSSOP (PW)
Lead pitch = 0.026 (0,65)
Height = 0.047 (1,20)
Area = 0.080 (53)



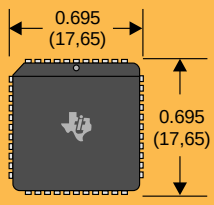
24-pin
SOIC (DW)
Lead pitch = 0.050 (1,27)
Height = 0.104 (2,65)
Area = 0.256 (165)



28-pin
PLCC (FN)
Lead pitch = 0.050 (1,27)
Height = 0.180 (4,57)
Area = 0.245 (158)



44-pin
PLCC (FN)
Lead pitch = 0.050 (1,27)
Height = 0.180 (4,57)
Area = 0.483 (312)



Package Styles

To complement the industry's broadest product spectrum, TI provides many packaging options designed to maximize board-space for a number of applications. In addition, TI is the industry's first IC supplier with a highly integrated JTAG Universal Bus Transceiver (UBT)—the SN74LVTH18512—packaged in an ultra-small Thin-Shrink-Small-Outline-Package (TSSOP).

For More Information

TI's extensive JTAG product line is enabling more designers than ever to incorporate boundary-scan testability into every area of their systems. If you would like more information on how Boundary-Scan Logic from Texas Instruments can help you build more successful systems, please call your local TI field sales office or authorized distributor. Or, visit the TI Boundary-Scan Logic (JTAG) Home Page at:

http://www.ti.com/sc/jtag

TI Worldwide Technical Support

Internet

TI Semiconductor Home Page
http://www.ti.com/sc

TI Distributors
http://www.ti.com/sc/docs/distmenu.htm

Product Information Centers

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