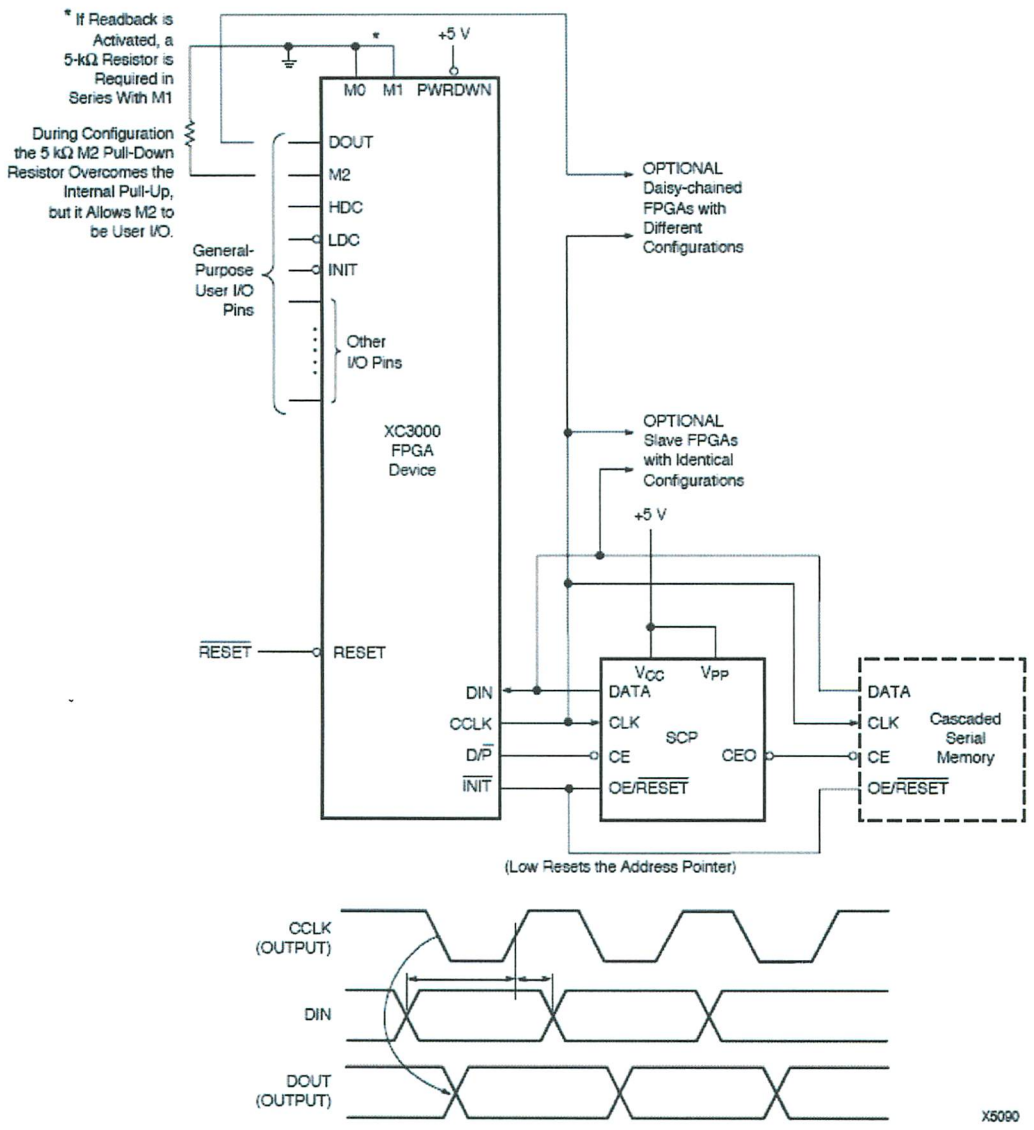

Figure 2: Master Serial Mode. The one-time-programmable Serial Configuration PROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional FPGA. An early D/$\overline{P}$ inhibits the PROM data output one CCLK cycle before the FPGA I/Os become active.

Upon power-up or reconfiguration, an FPGA enters the Master Serial Mode whenever all three of the FPGA modeselect pins are Low (M0=0, M1=0, M2=0). Data is read from the Serial Configuration PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration. Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an FPGA. Data from the Serial Configuration PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.