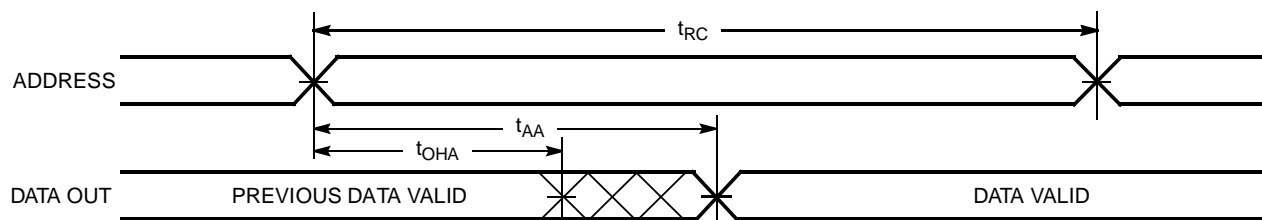


Switching Characteristics Over the Operating Range^[3,7] (continued)

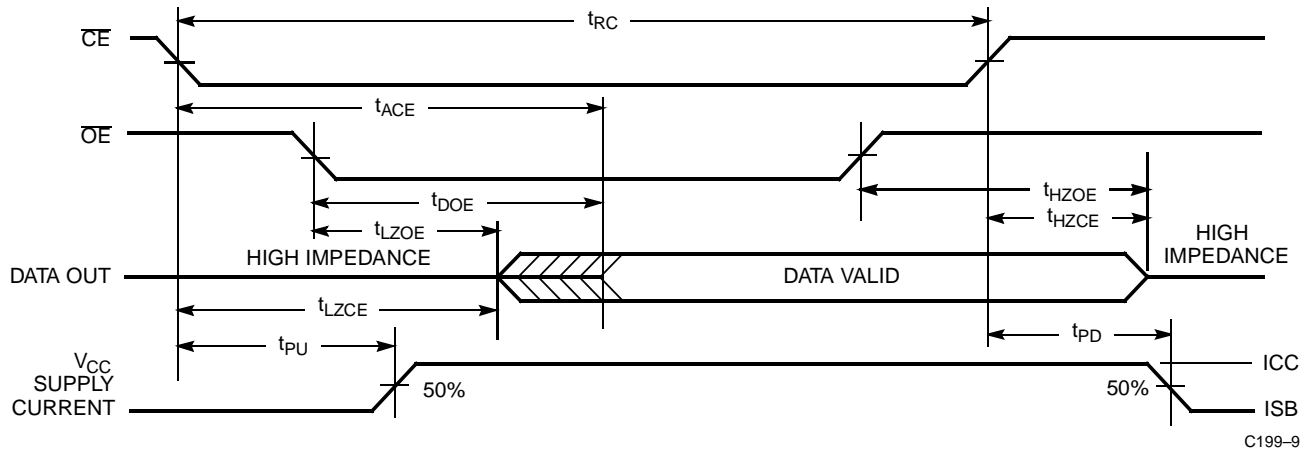
Parameter	Description	7C199-20		7C199-25		7C199-35		7C199-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	20		25		35		45		ns
t _{AA}	Address to Data Valid		20		25		35		45	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		20		25		35		45	ns
t _{DOE}	\overline{OE} LOW to Data Valid		9		10		16		16	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[8]	0		0		0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[8,9]		9		11		15		15	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[8]	3		3		3		3		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[8,9]		9		11		15		15	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		20		20		20		25	ns
WRITE CYCLE ^[10,11]										
t _{WC}	Write Cycle Time	20		25		35		45		ns
t _{SCE}	\overline{CE} LOW to Write End	15		18		22		22		ns
t _{AW}	Address Set-Up to Write End	15		20		30		40		ns
t _{HA}	Address Hold from Write End	0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	15		18		22		22		ns
t _{SD}	Data Set-Up to Write End	10		10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[9]		10		11		15		15	ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[8]	3		3		3		3		ns

Switching Waveforms
Read Cycle No. 1^[12, 13]


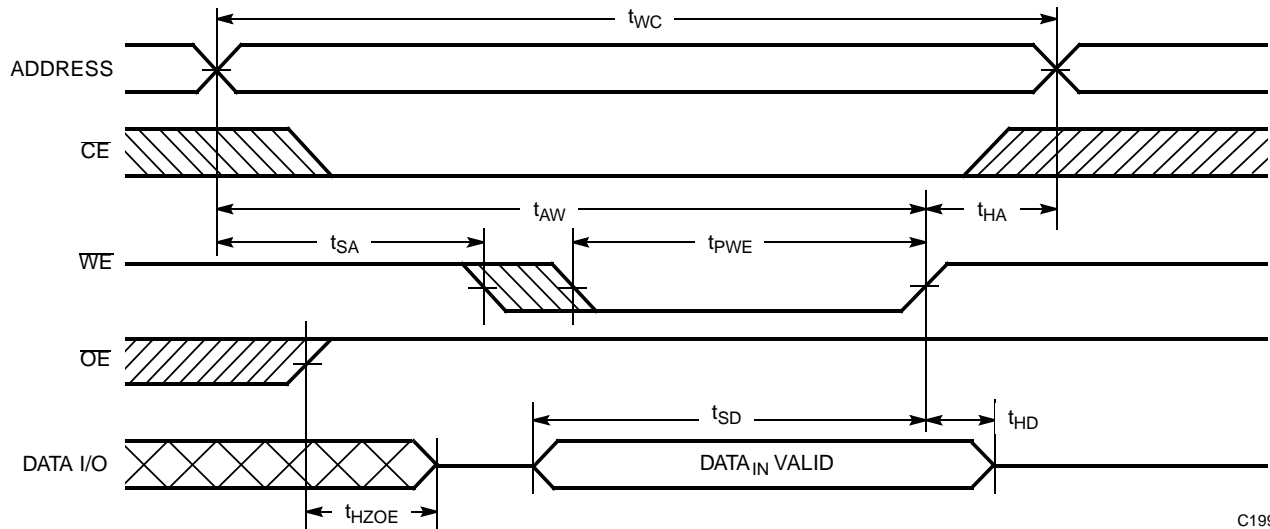
C199-8

Notes:

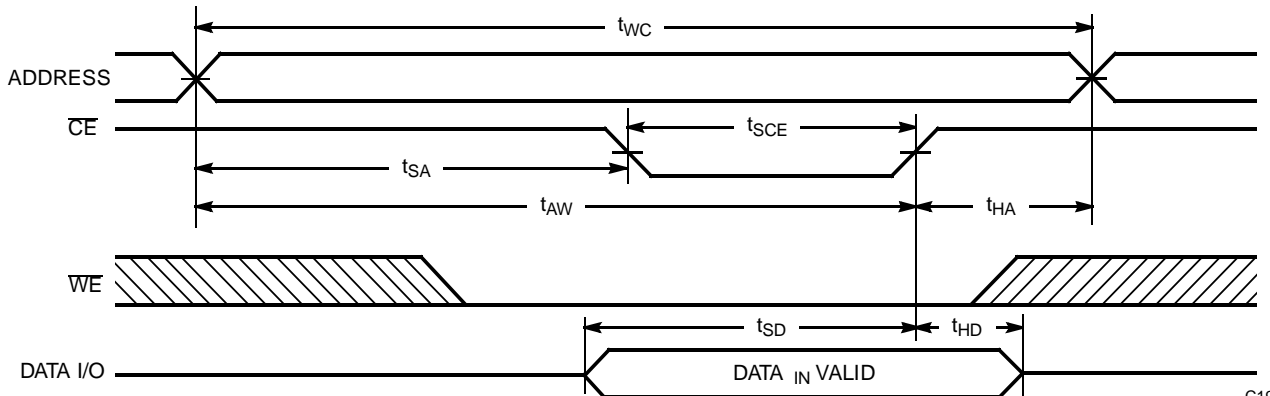
12. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
13. \overline{WE} is HIGH for read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 [13, 14]


C199-9

Write Cycle No. 1 (WE Controlled) [10, 15, 16]


C199-10

Write Cycle No. 2 (CE Controlled) [10, 15, 16]


C199-11

Notes:

14. Address valid prior to or coincident with \overline{CE} transition LOW.
15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
16. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.