

Design For Testability Guidelines

Version 3.1

www.xjtag.com

enquiries@xjtag.com | +44 (0) 1954 213888
XJTAG | The Irwin Centre | Scotland Road
Dry Drayton | Cambridge | CB23 8AR | UK

Introduction

The following DFT guidelines are suggestions for improving the testability of circuits using XJTAG. These guidelines should not be taken as a set of rules. The potential advantages in term of testability should be considered together with all other implications which they may have (e.g. functionality, device cost and board area).

It is assumed that readers of this document have some familiarity with IEEE standard 1149.1-1990 and the 1993 and 1994 revisions. Throughout this document the term 1149.1 refers to the IEEE 1149.1 (JTAG) Boundary Scan standard.

➤ Specify and use 1149.1 compliant devices

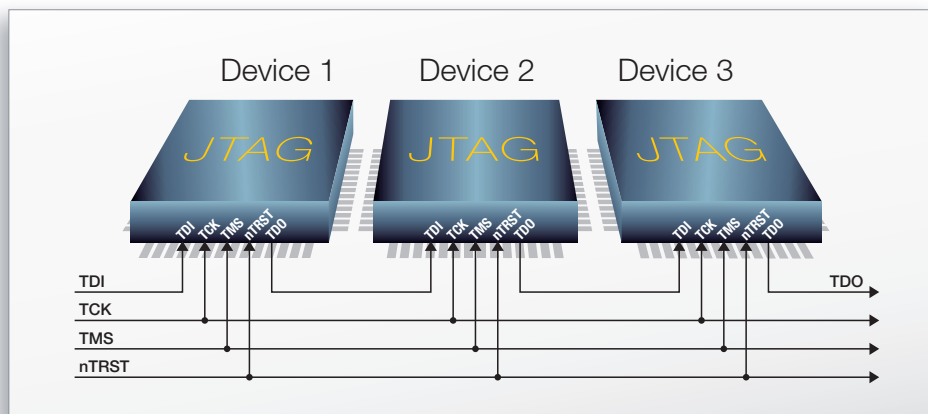
Although XJTAG is capable of testing non-compliant devices, greater coverage can be obtained by specifying 1149.1 compliant devices wherever possible. The more 1149.1 compliant devices that are incorporated into a circuit design the greater the number of nodes that can be fully exercised and tested.

➤ Check the BSDL files for 1149.1 compliant devices

1149.1 compliance requires that a BSDL file (Boundary Scan Description Language) is made available for any 1149.1 compliant device which describes its interfaces. Ensure that this file is available (usually directly from the device manufacturer's web-site) and that it has been fully validated. (BSDL syntax checking is included as an integral part of the XJTAG development system).

➤ Ensure the 1149.1 chain is correctly designed and laid out

Ensure that the design includes all the required 1149.1 TAP signals and that they are correctly wired. It is preferable to route TAP signals away from other active signals and separated by power or GND signals so that short circuits on the TAP signals are easier to detect. Add a suitable TAP connector to give access to the required signals. It is important to ensure that the default power-up mode of the system will have the 1149.1 device chain powered and in a compliant mode.

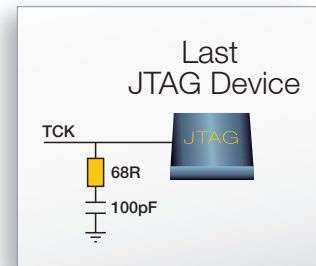


➤ Ensure low skew between TAP signals

It is important for correct operation that there is low skew between the TAP signals (especially TCK and TMS). Therefore track lengths and buffer delays should be kept equal wherever possible.

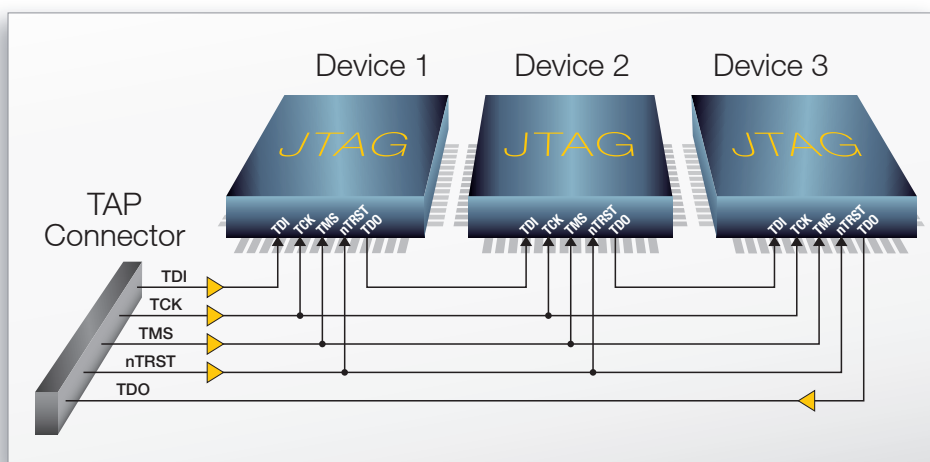
➤ Use correct termination for all TAP signals

TCK should be terminated at the last device in the JTAG chain with a 68R resistor and a 100pF capacitor in series to ground. TDI and TMS should be pulled to the power rail with 10K resistors. TDO should be pulled to the power rail with a 10K resistor and have a 22R series resistor fitted near to the final device in the chain. It is also recommended that a pull-down resistor be added to the nTRST line to avoid floating inputs (this value may require careful selection taking into account the driver strength and the strength of any nTRST pull-ups provided in the 1149.1 compliant devices).



➤ Buffer the TAP signals

If possible buffer the primary TAP signals to minimise noise and impedance mismatches and to improve fan-out. Buffer TCK, TDI, TMS, nTRST at board entry and TDO at board exit. It is advisable to buffer the signals after every 4-6 1149.1 devices in order to improve signal integrity, but remember to maintain a low skew between the signals.



➤ Use spare pins on 1149.1 compliant devices

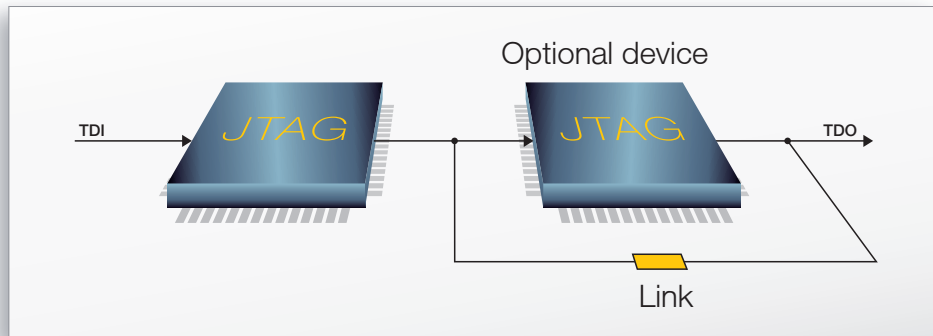
Where spare I/O pins are available on 1149.1 compliant devices use these to monitor otherwise inaccessible circuit nodes if this will not interfere with normal circuit operation. This will allow test coverage to be considerably enhanced if a careful choice of monitored nodes is made.

➤ Make full use of I/O pins on 1149.1 devices

Where a 1149.1 device is driving the input of a non-1149.1 compliant device use an I/O pin on the 1149.1 device if possible. This will allow "stuck at 0 or 1" testing to be performed on the output node by reading back the signal.

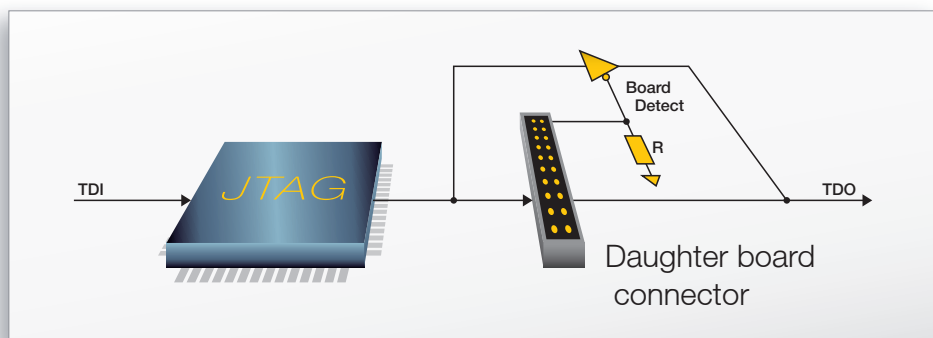
>> Bypass optionally fitted 1149.1 compliant devices

Where 1149.1 compliant devices are 'optional fit' devices on a board ensure that a link is provided to reconnect the TAP data chain whenever the device is not fitted as shown below.



>> Include add-on and option boards in the 1149.1 chain

Where daughter boards are used, route the 1149.1 chain through devices on the daughter boards via the board connector. If the daughter board is an option then use some board detect logic to bypass the TAP data path on the daughter board when it is not fitted as shown below.



>> If designing or specifying ASICs include 1149.1 compliance

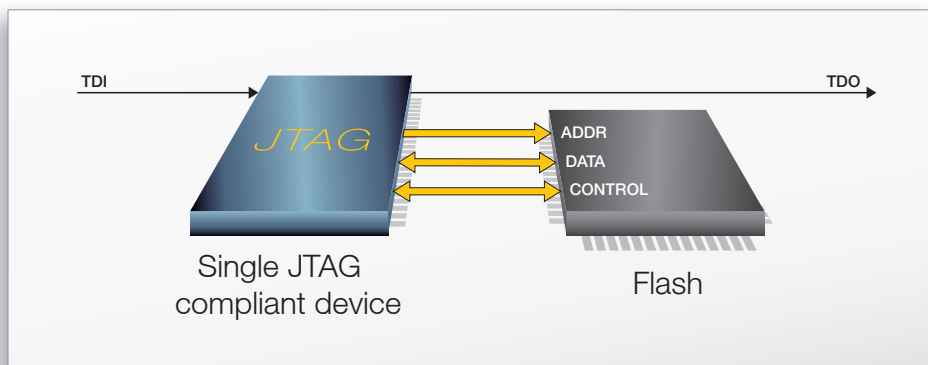
If your design requires or uses ASICs or any other custom designed silicon you should consider incorporating 1149.1 compliance.

>> Ensure that important board control signals are accessible

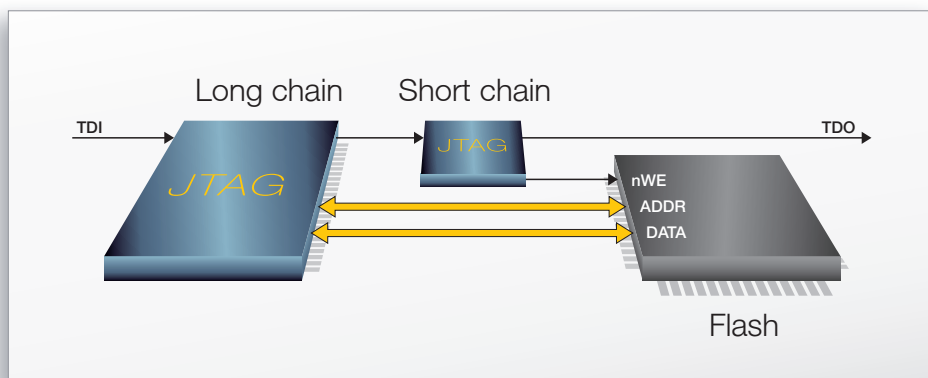
Where important board or device control signals exist, e.g. reset, power enables, watchdogs, and shutdown signals, ensure that these are controllable from an 1149.1 compliant device. If any 1149.1 compliant devices have modes which are not compatible with 1149.1 (e.g. the program pin for some FPGAs) ensure that the devices default to an 1149.1 compliant mode or the operation of the whole chain may be effected.

➤ Make programmable parts accessible from the 1149.1 chain

If in-system programming of programmable devices (EEPROM/flash/FPGA/CPLD) is required, and these devices do not include 1149.1 programming interfaces, make all the necessary pins of the programmable devices accessible from 1149.1 compliant devices. It is preferable to make all of the required nodes accessible from a single 1149.1 compliant device, in this instance the XJTAG development system will automatically put all other devices in the 1149.1 chain into CLAMP mode (when not being used) to improve performance.



It can sometimes be advantageous to use short-chain 1149.1 compliant devices (e.g. 1149.1 enabled buffers) to control circuit nodes which will be toggled frequently (e.g. the nWE pin on flash parts) as shown in the following diagram. This allows the XJTAG development system to reduce the active chain length and improve performance when addressing only these nodes. (Future versions of the XJTAG development system will allow direct I/O access to these nodes which will further improve performance – to utilise this facility when it becomes available it is recommended that these circuit nodes are made accessible at the test connector, or at some suitable point in the circuit).

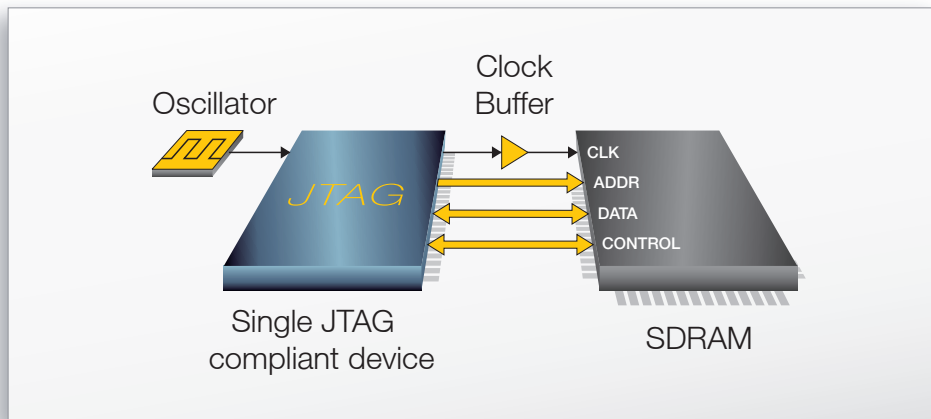


➤ Connect driver direction control and output enable pins

Wherever multiple sources can drive a signal ensure that sufficient control over the drivers is available from the 1149.1 devices to enable/disable the outputs of all the signal drivers as required. Where non-1149.1 compliant bidirectional bus drivers are included ensure that the direction can also be controlled.

>> Allow control of the clock to synchronous devices

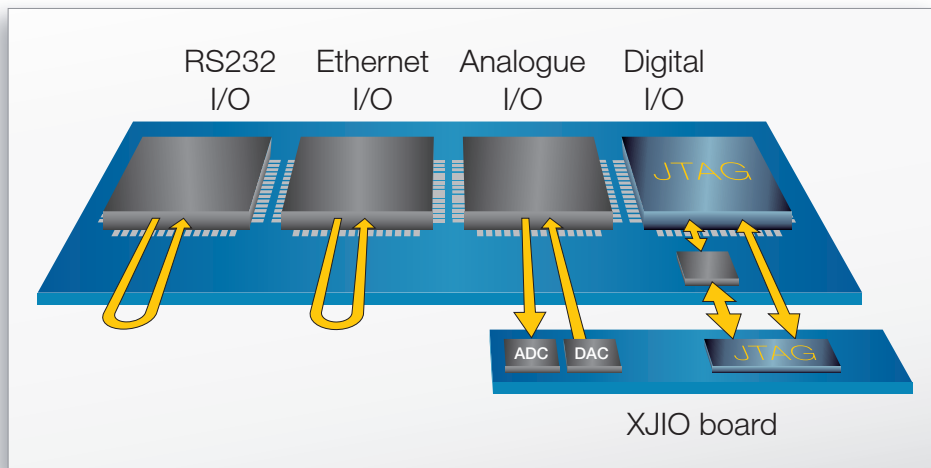
Many synchronous devices can be tested by XJTAG if control over the clock is possible. For example an SDRAM connected to an FPGA can be tested only if the SDRAM clock is controlled by an 1149.1 compliant device. If a free-running clock were to be connected directly to the SDRAM then XJTAG test vectors cannot be synchronised to the clock in real time. If an 1149.1 compliant device is available (e.g. CPLD or FPGA) then route the clock through the device between the clock source and the SDRAM or clock buffers to maximise test coverage as shown below.



>> Design I/O interfaces for 1149.1 test

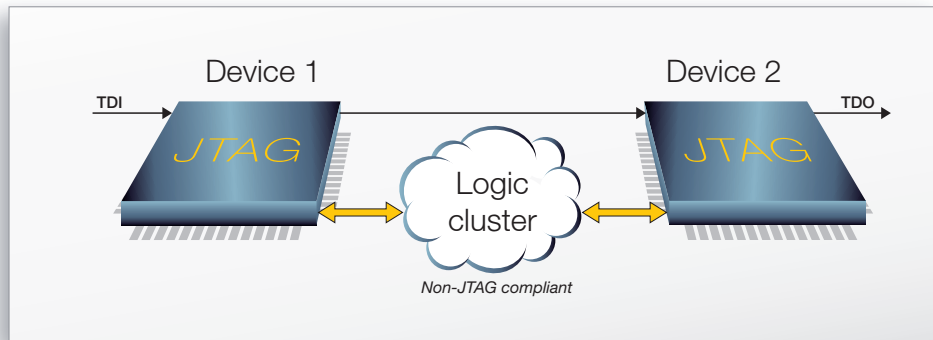
Test coverage is greatly increased if external connectors can be attached to 1149.1 accessible nets. Many connector pins are attached to nets with a single 1149.1 pin, testing of these connector pins can be extended to include open circuit testing if connected to external 1149.1 controllable I/O, such as the XJIO board.

Where such testing is not possible design I/O ports so that loopback is possible. This extends testing through off-board connections and greatly increase test coverage. Simple loopback connectors will suffice for most interfaces (e.g. Ethernet, RS232, RS485 etc.) but external test circuitry can aid this if necessary and this can even be controlled by the TAP chain if this is extended through the I/O connector.



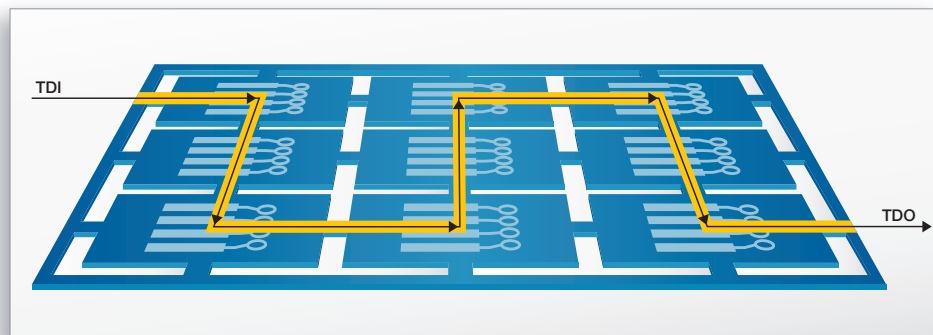
➤ Surround logic clusters with 1149.1 compliant devices

Arrange non-1149.1 compliant logic into clusters surrounded by 1149.1 compliant devices which can control all the inputs and monitor all the outputs to and from the cluster. Try to ensure that sufficient access to nodes within the cluster is available in order to test the operation of the cluster as fully as possible. If necessary add additional 1149.1 compliant devices to gain access to the required cluster nodes.



➤ Consider testing multi-board panels as one unit

Where multiple boards are constructed on a single panel consider routing power and TAP signals through some or all of the boards on a panel to enable simultaneous testing of all the boards before separating them.



➤ Consider watchdog operation

If the circuit contains a watchdog ensure that this can be disabled for the duration of testing (either using a link or preferably using an 1149.1 controlled pin). Undetermined results can occur when a watchdog event occurs which may impact upon testing. It is preferable to ensure that the watchdog can only be disabled using XJTAG development system and not by software to avoid disabling by software faults. Alternatively, ensure that the watchdog has a timeout long enough to allow completion of all testing before it occurs.

➤ Use non-volatile storage for configuration information

Use XJTAG File I/O to program options, serial numbers, Ethernet MAC addresses etc. into non-volatile on-board storage devices as part of the test procedure.

➤ Test analogue circuits

Although 1149.1 does not explicitly include the testing of analogue circuits many tests can be performed with careful design. Techniques include using 1149.1 compliant outputs to pull comparator or amplifier inputs to fixed states and the use of comparator or amplifier outputs to provide inputs to 1149.1 compliant devices. Additional low cost DACs and ADCs can be added to provide supplementary controls and monitoring of analogue clusters. With a small amount of appropriate additional circuitry large amounts of analogue testing can be performed.

➤ Do not rely on programmable device I/O features

For example, try not to use the programmable pull-ups which are provided in the I/O pads of some FPGAs to enable external logic to operate. If the pull-ups required on an I2C bus were only provided by these programmable pull-ups then all devices attached to the I2C bus may not be testable by XJTAG. If you have to do this then make the I2C bus pins available at an external connector so that pull-ups can be added externally for testing purposes, or if the I2C bus is used to access an SDRAM module then provide a 'test' module fitted with additional resistors.

➤ Make full use of on-board intelligent devices and advanced XJTAG features

If all else fails and some part of the circuit cannot be made testable using standard 1149.1 features or real-time testing is required then consider using the advanced facilities of the XJTAG programming language XJEase to facilitate testing of these parts by making use of on-board intelligent devices. For example a small program can be loaded into an on-board flash or CPLD device which can enable the CPLD or a microprocessor to perform additional real-time test and configuration functions.

Glossary

ASIC	Application Specific Integrated Circuit
BSDL	Boundary Scan Description Language
DFT	Design for Testability
IEEE 1149.1	IEEE Standard 1149.1–1990 “Test Access Port and Boundary Scan Architecture” (see www.ieee.org)
I/O	Input / Output
JTAG	Joint Test Action Group
NTRST	Test Reset (Active low TAP Signal)
TAP	Test Access Port
TCK	Test Clock (TAP Signal)
TDI	Test Data Input (TAP signal)
TDO	Test Data Output (TAP Signal)
TMS	Test Mode Select (TAP Signal)
XJTAG	A suite of tools aiding the development and test of electronic systems