```
module mod9(clk, q, clear);
input clk, clear;
output [3:0]q;

wire [3:0]d;
wire C;

// define D-FF input boolean equations

assign d[0] = ~q[0];
assign d[1] = q[1]^q[0];
assign d[2] = q[2]&~q[1] | q[2]&~q[0] | ~q[2]&q[1]&q[0];
assign d[3] = q[3]&~q[1] | q[3]&~q[0] | q[3]&~q[2] | ~q[3]&q[2]&q[1]&q[0];

// decoder description

assign C = ~(~clear | (q[3]&q[0]));

/* you could also have done the decoder as follows:

wire y1,y2;

and(y1, q[3], q[0]);
not(y2, clear);
nor(C, y1, y2);

which would make it a gate level description
*/

// instantiate the 4 D-FFs

d_ff g1(q[0], d[0], C, clk);
d_ff g2(q[1], d[1], C, clk);
d_ff g3(q[2], d[2], C, clk);
d_ff g4(q[3], d[3], C, clk);

endmodule
```