ECE351 FSM homework problem

You are to design, simulate, synthesize and demonstrate the following FSM. This is a 2-week lab due Thursday, May 22nd before 0930.

You must demonstrate the FSM to either the TA or myself to receive 6 out of the 10 points. The TA's hours are posted. You can demonstrate it to me during my office hours or, if you can catch me, Tuesday or Thursday afternoons between 1400 and 1700.

FSM description: A vending machine sells candy for 30 cents. It accepts nickels, dimes and quarters and provides no change if more than 30 cents is deposited. Design a finite state machine to control the vending machine. The inputs to the machine are two signals indicating which coin has been deposited or that a coin release is requested. The 4 possible inputs are encoded by the two signals as:

00 nickel deposited
01 dime deposited
10 quarter deposited
11 coin release

Assume that your machine will receive a clock only when there is an input (a coin has been deposited or the coin release has been pulled). These two signals are synchonized with a clock. The outputs of your machine are two signals: one releasing the candy and the other releasing the coins.

Your simulation must test the following cases:

1. nickel -> nickel -> dime -> dime
2. nickel -> dime -> nickel -> dime
3. dime -> dime -> nickel -> change return
4. dime -> dime -> nickel -> dime

You must also simulate the above 4 test cases.

You will receive 4 points for turning in a correct timing diagram showing each of the above test cases. You will receive 6 additional points if you can synthesize the

FSM and correctly demonstrate all of the above test cases. Use two of the dip switches for the input. Use two LEDs to show the two FSM outputs.

Do not use a signal generator or a dip switch for the FSM clock!! You must use the pushbutton reset switch on the FPGA board as the clock for your FSM. This switch as switch debouncers on-board. You can assign this pushbutton as a clock. when you do all of the other pin assignments.