ECE 271 HW #4

(Due Thursday August 6th)

1. A digital system consists of 10 components. Three of the components have a failure rate of 300 FITs, 2 components 150 FITs and the remaining components 425 FITs. What is the system MTBF?

3 x 105 hrs

1. Briefly describe the three phases of failure rates over the lifetime of a product.

Infant mortality: early in the product lifecycle. Failures are due to design flaws and possibly misuse by the end-user.

Normal operation: middle portion of the lifecycle. Failures are relatively low because design flaws have been corrected.

Wear out: failures start to rise because of component failures

1. You are using a MT48LC64M8A2-7E:C SDRAM.
2. Describe the steps necessary to initialize this memory device before performing read or write operations

See page 11 of the datasheet

1. You have configured the memory to perform read operations with a burst length of 4. How do you ensure the write operations are only 1 location at a time and not also a burst of 4 locations?

Set bit 9 of the mode register.

1. What is the shortest amount of time it will take to read 64 consecutive memory locations assuming the fastest possible clock and a CAS latency of 3?

3 clocks for the first read (because of CAS latency) and 63 more clocks for the remaining read operations. The maximum clock frequency is 143 MHz (7 ns).

Hence it takes approximately 66 x 7 = 462 ns. (see figure 11 in the datasheet.)