

CORE Generator Components

The CORE Generator contains a library of parameterizable and fixed netlist LogiCORE cores along with data sheets for each core. LogiCOREs are designed and supported by Xilinx.

CORE Generator Interfaces

The CORE Generator batch mode interface allows you to interface the CORE Generator to system-level tools.

Generating a Core

Enter your core parameters, then simply click on the Generate button. The output is an optimized CORE for the targeted FPGA device family which includes the following files.

- A tailored Xilinx implementation netlist with complete relative placement information to guarantee performance
- VHDL or Verilog instantiation code
- VHDL or Verilog wrapper for simulation support
- A symbol for schematic capture tools

CORE Generator Platform Support

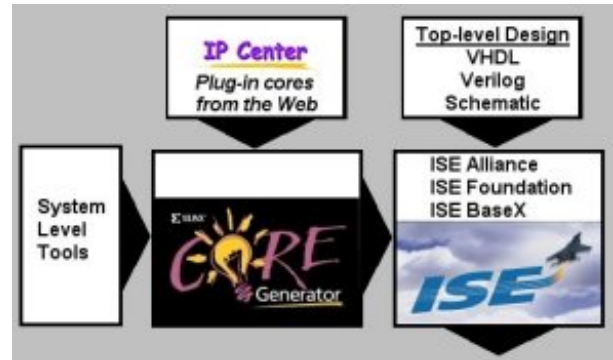
The Xilinx CORE Generator supports Windows 2000, Windows XP and Solaris 2.8 operating systems for PC and Workstation compatibility.

New Cores and Updates

New plug-in cores not already bundled with the CORE Generator can be downloaded from the IP Center Web site at www.xilinx.com/ipcenter/coregen/updates, or added to the Xilinx CORE Generator using the built-in CORE Generator Update Installer Tool.

Xilinx Core Generator

Achieve high performance results while cutting your design time



CORE Generator System Overview

The Xilinx CORE Generator System generates and delivers parameterizable cores optimized for Xilinx FPGAs. Use the Xilinx CORE Generator System to design high-density Xilinx FPGA devices and achieve high performance results while also cutting your design time.

The CORE Generator is included with the Xilinx ISE BaseX, ISE Foundation, and ISE Alliance Series software and comes with an extensive library of Xilinx LogiCOREs, including DSP functions, memories, storage elements, math functions and a variety of basic elements.

Xilinx Smart-IP technology produces cores with predictable performance. Core performance is independent of Xilinx FPGA device size and number of cores instantiated, even in large devices. Xilinx Smart-IP technology guarantees that there is no routing interference between multiple cores or between cores and other logic.

No Surprises! – The predictable and repeatable performance of CORE Generator cores allows large FPGA designs to maintain target clock speeds as the design process proceeds. If it is necessary to move to a larger device, the core performance does not change.

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