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INTRODUCTION

Due to higher system frequencies, new packages and programs like the "Energy Star" initiative, a strict limit on computer system power budgets is common these days. Allowable power dissipation for each device on a board needs to be minimal. CMOS devices have negligible static power dissipation, but when switching at a high frequency, dynamic power dissipation can significantly contribute to overall power dissipation. Capacitive output loading further increases this dynamic power loss.

This application note describes ways to estimate power dissipation of individual CMOS logic devices in a system. It will help users determine if their designs raise any power dissipation concerns. The equations used here are applicable to simple bus interface devices where the dominant power dissipation is in the output drivers rather than internal to the device. In more complex devices such as a large ASIC or processor where internal nodes may switch at higher frequencies and contribute significantly to overall power, other factors enter into the equations. In such cases the simplification used here may not yield accurate results. Please refer to individual datasheets or application notes in such cases. Examples are given using IDT FCT/FCT-T Logic devices. Power dissipation in a clock driver is of particular concern, because this kind of device has all outputs continuously switching. Charts relating thermal limits to maximum allowable power, frequency and load are also given for IDT FCT, FCT-T and clock devices.

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THERMAL LIMITS

One of the basic factors limiting permissible power dissipation in a device is maximum allowable junction temperature,

T_{JMAX}. T_{JMAX} is normally based on the limits imposed by die reliability. Based on this T_{JMAX} limit, maximum allowable power dissipation can be calculated as follows (assume a worst-case ambient temperature) :

$$\theta_{JA} = \frac{(T_J - T_A)}{P_D} \quad .... \text{ eqn (i-a)}$$

$$\Rightarrow \quad P_D = \frac{(T_J - T_A)}{\theta_{JA}} \quad .... \text{ eqn (i-b)}$$

$$\Rightarrow \quad P_{DMAX} = \frac{(T_{JMAX} - T_A)}{\theta_{JA}} \quad .... \text{ eqn (i-c)}$$

where,

θ_{JA} = Thermal resistance (this parameter is package specific & assumes no airflow. Adding or increasing airflow will reduce)

T_J = Junction temperature

T_{JMAX} = Maximum allowable junction temperature

T_A = Ambient temperature

P_D = Total Device Power dissipation

P_{DMAX} = Maximum allowable power dissipation (based on T_{JMAX})

IDT requires that all devices not exceed a upper temperature limit of 150°.

So, $T_{JMAX} = 150°C$

Therefore,
$$P_{DMAX} = \frac{(150°C - T_A)}{\theta_{JA}} \quad .... \text{ eqn (i-d)}$$

Referring to Table1, we see that the thermal resistance for the 20pin SSOP is 100°C/W with 0 LFM (linear feet per minute) airflow. The commercial temperature limit is 70°C so when we plug in these values in equation (i-d), we get

$$P_{DMAX} = \frac{(150°C - 70°C)}{100°C/W}$$

$$P_{DMAX} = 0.8W$$

DEVICE	PACKAGE	θJA (0 LFM)	PDMAX @ 70C
805/6,	PDIP - 20	75° C/W	1.06W
805T/6T,	SOIC - 20	90° C/W	0.88W
807T,	SSOP - 20	100° C/W	0.8W
810T,	QSOP - 20	108° C/W	0.74W
3805,	CERDIP - 24	93° C/W	0.86W
3807	LCC - 24	70° C/W	1.14W
	CERPACK - 24	130° C/W	0.615
88915TT,	PLCC - 28	97° C/W	0.82W
388915T	SSOP - 28	80° C/W	1.06W
3932	SSOP - 48	80° C/W	1.06W
	TSSOP - 48	94° C/W	0.94W

Table 1. Clock Driver Thermal characteristics

ESTIMATING TOTAL POWER DISSIPATION BASED ON DATASHEET SPECIFICATIONS

Based on datasheet specifications of the device and actual operating conditions, power dissipated by a device can be estimated to ensure that thermal limits as specified in the previous section are not exceeded. Device power dissipation consists of two basic components - the unloaded power dissipation inherent to the device and the "load" power dissipation which is a function of the device loading. Power dissipation in an unloaded CMOS logic device can be calculated using the following equations :

$$I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC} \quad .... \text{ eqn (ii-a)}$$

$$= I_{CC} + \Delta I_{CC} N_T D_T + I_{CCD} N_D f \quad .... \text{ eqn (ii-b)}$$

where,
I_C = Total Power Supply Current
I_{CC} = Quiescent (static) Power Supply Current
ΔI_{CC} = Power Supply Current for a "TTL" High (V_{IN} = 3.4V) input
N_T = Number of inputs at a "TTL" High level
D_T = Duty-cycle of the inputs at "TTL" High levels.
I_{CCD} = Dynamic Power Supply Current per unit frequency
f = Frequency of switching outputs
N_D = Number of switching outputs
V_{CC} = Power Supply voltage

Thus,
$$P_{D(unloaded)} = (I_C)V_{CC} \quad .... \text{ eqn (iii-a)}$$

$$= (I_{CC} + \Delta I_{CC} N_T D_T + I_{CCD} N_D f)V_{CC} \quad .... \text{ eqn (iii-b)}$$

Device power dissipation characteristics (I_{CC}, ΔI_{CC}, I_{CCD}) are typically specified in IDT datasheets. In cases where they are not explicitly specified, reasonable approximations can be obtained based on data. Sometimes the device dynamic power dissipation is expressed in terms of a capacitance -C_{PD}. C_{PD} is the equivalent device power dissipation capacitance and is an inherent device parameter. I_{CCD} and C_{PD} are equivalent parameters and the equation below shows how to

DEVICE	PACKAGE	θJA (0 LFM)	PDMAX @ 70°C
FCTxxx	PDIP - 16	75° C/W	1.06W
FCTxxxT	PDIP - 20	90° C/W	0.88W
FCT2xxxT	PDIP - 24	100° C/W	0.8W
FCT3xxx	SOIC - 16	90° C/W	0.88W
	SOIC - 20	93° C/W	0.86W
	SOIC - 24	70° C/W	1.14W
	SOIC - 28	63° C/W	1.27W
	SSOP - 16	130° C/W	0.615W
	SSOP - 20	100° C/W	0.8W
	SSOP - 24	100° C/W	0.8W
	QSOP - 16	130° C/W	0.61W
	QSOP - 20	108° C/W	0.74W
	QSOP - 24	99° C/W	0.8W
	CERDIP - 20	85° C/W	0.94W
	CERDIP - 24	65° C/W	1.23W
	LCC - 24	58° C/W	1.37W
	CERPACK - 24	105° C/W	0.76W
FCT16xxxT	SSOP - 48	80° C/W	1W
FCT162xxxT	SSOP-56	75° C/W	1.06W
FCT166xxxT	TSSOP - 48	94° C/W	0.85W
FCT163xxx	TSSOP - 56	85° C/W	0.94W
	CERPACK - 48	72° C/W	1.11W
	CERPACK - 56	68° C/W	1.17W

Table 2. FCT Bus Interface Thermal characteristics

convert between the two representations.

C_{PD} = Equivalent power dissipation capacitance

$$C_{PD} = \frac{I_{CCD}}{V_{CC}} \quad .... \text{ eqn (iv)}$$

For example, at 5V supply, a device with typical I_{CCD} = 60mA/MHz/bit has an equivalent C_{PD} of 15pF.
So alternately,
$$P_{D(unloaded)} = (I_{CC} + \Delta I_{CC} N_T D_T + C_{PD} V_{CC} N_D f)V_{CC}$$
$$.... \text{ eqn (iii-c)}$$

A CMOS device can be represented by the equivalent power dissipation model in Figure 1.
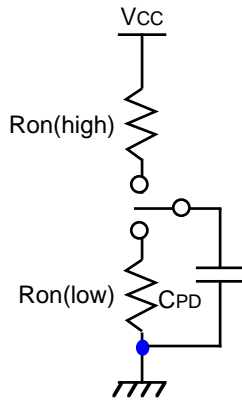
Figure 1. Power Dissipation Model - Unloaded case.

Registered Devices

In the case of registered or synchronous devices, the question of which frequency to substitute for "f" in equation (iii) arises. An approximation to the power dissipation in this case is given in equation (v) below.

$$\left(\begin{array}{c} I_{CC} + \Delta I_{CC} N_T D_T + \\ (N_{CP} \frac{f_{CP}}{2} + f_i N_i) I_{CCD} \end{array} \right) V_{CC} .... \text{ eqn (v)}$$

Devices such as the FCT374, FCT16823, etc. fall in this category.

Load Power Dissipation

Device loading can dramatically alter the overall power dissipation. Most CMOS loads appear capacitive and add to the dynamic power dissipation but draw no static power. Typical capacitive load presented by a single CMOS device is 5 to 10pF. This is almost as high as typical device power dissipation capacitance values, indicating that the load can constitute a significant portion of overall power dissipation.

Dynamic Power Dissipation for a capacitive load, C_L, is

$$P_{D(load)} = N f C_L V_{OH}^2 \quad .... \text{ eqn (vi-a)}$$

where,
N = Number of outputs loaded with C_L
f = Frequency of the switching outputs
C_L = Load capacitance per output
V_{OH} = Logic High voltage at the outputs (TTL Logic HIGH levels are typically 3.5V, CMOS Logic HIGH levels are typically V_{CC})

Using equations (iii-b) and (vi-a), total power dissipation for a device with capacitive loading is,

$$P_{D(loaded)} = (I_{CC} + \Delta I_{CC} N_T D_T + C_{PD} V_{CC} N_D f) V_{CC} = N f C_L V_{OH}^2 .... \text{ eqn (vii-a)}$$
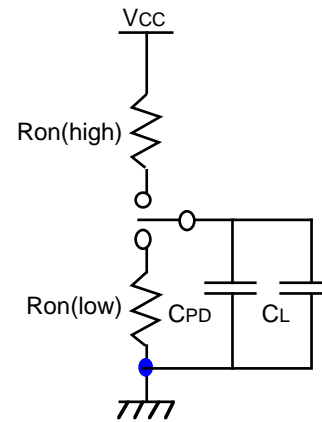

Figure 2. Power Dissipation Model with Capacitive loading

Figure 2 shows the equivalent device and load power dissipation model corresponding to equation (vii-a).

At high frequencies, the model represented by equation (vi-a) proves inadequate. Experiments on FCT-T devices have shown that equation (vi-b) is overly pessimistic in cases where the total capacitive load exceeds approximately 150pF. Thus the limits shown in Table 4 are on the conservative side for such loads.

Examples

This section shows a few examples of power dissipation estimations using the above equations.

Device	Number of Outputs	I_{CCQ} Typ.	I_{CCQ} Max.	ΔI_{CC} typ.	ΔI_{CC} Max.	I_{CCD} Typ.	I_{CCD} Max.
Units	—	mA	mA	mA/input	mA/input	mA/MHz	mA/MHz
FCT805/6	11	0	1.5	1.0	2.5	0.15/bit	0.2/bit
FCT805T/6T FCT810T	11 10	0	0.5	0.5	2.0	0.06/bit	0.1/bit
FCT807T	10	0	0.5	0.5	2.0	0.04	0.06
FCT3805 FCT3807	11 10	0	0.3	0	0.03	0.03/bit	0.045/bit
FCT88915TT	8	2.0	4.0	0.5	1.5	0.25/bit	0.4/bit
FCT388915	8	2.0	4.0	0	0.03	0.2/bit	0.3/bit
FCT3932	18	2.0	4.0	0	0.03	0.2/bit	0.3/bit
FCTxxx	8/9/10	0.2	1.5	0.5	2.0	0.15/bit	0.25/bit
FCTxxxT	8/9/10	0	0.1	0.5	2.0	0.15/bit	0.25/bit
FCT2xxxT	8/9/10	0	0.1	0.5	2.0	0.06/bit	0.12/bit
FCT16xxxT FCT162xxxT FCT166xxxT	16/18/20	0	0.5	0.5	1.5	0.06/bit	0.1/bit
FCT163xxx	16/18/20	0	0.1	0	0.03	0.05/bit	0.075/bit

Table 3. IDT device power dissipation current (Refer to current datasheets for latest specifications)

1. Consider a case where the FCT807T is used at 50MHz in the SSOP package. All outputs are used and loaded with 20pF. To ensure that this operating condition does not exceed the thermal limits imposed by the die and the package, an estimation of power dissipation under the stated conditions can be made as follows :

P_D(unloaded) = (0 + 1 x 0.5 x 2.0 + 10 x 50 x 0.04) mA x 5 = 0.105W
P_D(load) = 10 x 50MHz x 20pF x 3.4^2 = 0.1156W
=> P_D(loaded) = 0.2206W

This number is well within the PDmax limit indicated in Table 1.

2. To check whether it is safe to operate the 88915TT with 2Q at 100MHz and all outputs loaded with 20pF :

(Note that the 88915 has one output running at 2Q frequency, six outputs at Q frequency and one output at Q/2 frequency. This is equivalent to 4.25 outputs running at 2Q frequency)

P_D(unloaded) = (4.0 + 1 x 0.5 x 1.5 + 4.25 x 100 x 0.25) mA x 5 = 0.555W
P_D (load) = 4.25 x 100MHz x 20pF x 3.5^2 = 0.104W
=> P_D (loaded) = 0.659W

which is again less than the PDmax limit shown in Table 1.

Table 4, which follows, summarizes maximum frequency limits for IDT clock buffers under a set of assumed operating conditions as mentioned.

SUMMARY

Datasheet power specifications in individual devices can often be used to ensure that individual device reliability limits are met. They are also useful in calculating overall system power dissipation. This application note provides engineers with an equivalent power dissipation model and equations to use with FCT/FCTT logic and clock buffers. IDT datasheets specify power supply current limits. These can be plugged into the equations given in this application note to estimate total device power dissipation.

DEVICE	# of outputs	Load	Load	Package	Airflow	No power limitations upto:
FCT805/6	11	10pF	110pF	SOIC-20	0	64MHz
FCT805T/6T	11	10pF	110pF	SSOP-20	0	116MHz
FCT807T	10	10pF	100pF	SSOP-20	0	189MHz
FCT810T	10	10pF	100pF	SSOP-20	0	128MHz
FCT3805	11	10pF	110pF	SSOP-20	0	282MHz
FCT3807	10	10pF	100pF	QSOP-20	0	310MHz
FCT88915TT	8	10pF	80pF	PLCC-28	0	90MHz (2Q)
FCT388915T	8	10pF	80pF	PLCC-28	0	175MHz (2Q)
FCT388915T	8	10pF	80pF	SSOP-28	0	227MHz (2Q)
FCT3932	18	10pF	180pF	SSOP-48	0	59MHz
FCT3932	12	10pF	120pF	SSOP-48	0	80MHz
FCT3932	18	10pF	180pF	TSSOP-48	0	71MHz
FCT3932	12	10pF	120pF	TSSOP-48	0	54MHz

Table 4. IDT Clock Driver frequency limits (under assumed conditions)