ECE 371 Project #2

DUE: 1000 December 5

Figure 8.1 in your textbook shows a block diagram for a basic ARM memory system. In this project you are to design this memory system plus you must add one 8-bit input port and one 8-bit output port.

You must conduct a worst-case timing analysis to see how many wait states are required for the ports and the memory. Below are the specifications of the memory and I/O system:

- The memory system has 8K×32 of program memory and 8K×16 of data memory.
- The memory map is shown in Table 1.
- The RAM chips are the CY7C185-20, the ROM chips are 27C64-12, and all glue logic is in a PAL16R4-15C. Use the 573/574 devices for the ports. (All datasheets are on the course website.)
- All glue logic (including the wait state generator) are in the PAL16R4.
- MCLK is a 50% duty cycle, 40 Mhz clock signal. MCLK is used to generate any strobes and it is also used as the clock for the PAL.
- All program memory accesses are 32-bits, all data memory accesses are 16 bits and all I/O port accesses are 8-bits.

Function	Start	End
Program	00000000	3FFFFFFF
Data	C0000000	FFFFFFFF
I/O	80000000	BFFFFFFF
Unused	40000000	7FFFFFFF

Table 1: Memory map for project 2

The memory controller is implemented in the PAL and processes all signals shown in Figure 9 of Application Note 29 (with the address lines modified to comply with Table 1). The memory controller is implemented in the PAL, but **YOU DO NOT HAVE TO PROVIDE ANY DETAILS ON ITS INTERNAL CIRCUITRY.** Yes, this means you do not have to show the decoding circuitry or the wait-state generator circuitry. You must, however, use the propagation delays of the PAL when performing the worst-case timing analysis.

Your project report must contain

- a schematic of your design (NOTE: you need only show ARM signals needed for communications with the memory and I/O ports.)
- a timing diagram for read and write operations for both memory and I/O port accesses
- all calculations associated with the timing analysis
- a table showing how many wait states are needed to communicate with each type of memory and I/O port device.

Your project report must be typed. Schematics must be drawn with either some sort of graphics software or schematic capture system. Hand drawings are accepted only if drawn with a template.

ANY PROJECT REPORT SUBMITTED WITH A REPORT COVER WILL NOT BE ACCEPTED.