Integrated Circuit Testing for Quality Assurance in Manufacturing:
History, Current Status, and Future Trends

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Abstract—Integrated circuit (IC) testing for quality assurance is approaching 50% of the manufacturing costs for some complex mixed-signal IC’s. For many years the market growth and technology advancements in digital IC’s were driving the developments in testing. The increasing trend to integrate information acquisition and digital processing on the same chip has spawned increasing attention to the test needs of mixed-signal IC’s. The recent advances in wireless communications indicate a trend toward the integration of the RF and baseband mixed signal technologies. In this paper we examine the developments in IC testing form the historic, current status and future view points. In separate sections we address the testing developments for digital, mixed signal and RF IC’s. With these reviews as context, we relate new test paradigms that have the potential to fundamentally alter the methods used to test mixed-signal and RF parts.

I. INTRODUCTION

O

ver the years of its development, the integrated circuit technology has brought great progress to the design of high performance systems. Many challenges in the manufacturing process had to be solved to achieve this. One of the steps in this process, namely testing, is posing the most significant challenge to contemporary and future integrated circuit (IC) manufacturing. This is a continuing trend, because due to decreasing silicon cost and increasing complexity of integrated circuits, testing constitutes a very sizable portion of the IC manufacturing cost. This trend is further accentuated by the emergence of mixed signal, including radio frequency (RF) circuits, coupled with the competitive price pressures of the high volume consumer market. Frequently, the cost of testing a chip with a CODEC,1 an integrated digital signal processor (DSP), and other base-band circuitry reaches 50 to 50% of the total cost.

Due to unavoidable statistical flaws in the materials and masks used to fabricate IC’s, it is impossible to realize 100% yield on any particular IC; where yield refers to the ratio of good IC’s to the total number of IC’s fabricated. A good IC is one that satisfies all of its performance specifications under all specified conditions. The probability of a bad IC increases in proportion to its size and complexity. It is also increased by process sensitivities that occur in digital and analog IC’s that rely on the control and/or matching of IC components or parameters to achieve their specified functionality. The details that govern IC yield and the associated economics that drive IC manufacturing are very interesting, but beyond the scope of this paper. The interested reader is referred to the literature, e.g., [98], [99]. In any event, testing is an indispensable part of the IC manufacturing process.

Since testing is repeatedly performed at several manufacturing stages, such as after wafer fabrication and packaging, it is very important to understand its inefficiencies. Reducing or eliminating these inefficiencies enables a chip manufacturer to drive down the cost of the final product [1], [2]. It is also important to understand the reasons for and the costs associated with testing. It is in the chip manufacturer’s best interest to minimize the number of bad devices shipped to the customer. A bad device is an IC that fails to meet one or more specifications at any point in the manufacturing process. Poorly designed tests or parts not designed for testability can result in bad devices appearing as bad parts or good devices failing tests and appearing as bad. The shipment of bad devices leads to incurred replacement cost, loss of reputation, and possible loss of market share. The other side of this problem is not much better. When good parts are represented as bad, it reduces the chip yield and, correspondingly, it reduces the earnings of the chip manufacturer. At this point we should introduce the reader to the term DUT or device under test. DUT is a generic term used in the testing literature to refer to the component, or the bare IC die on a wafer, or the packaged IC, or the circuit board, etc. that is being tested. We will use this term frequently in this paper, mostly to refer to bare and packaged IC’s.

The major steps of a typical IC manufacturing process, with clear indication of the points at which the device testing is performed, are shown in the flow diagram of Fig. 1.

Testing, at different steps in the product development process, addresses different issues and presents different challenges. The initial testing is performed within the computer-aided design (CAD) environment. At this stage the
designer is verifying the functionality and the performance of the intended product. Many of the production tests, indicated in Fig. 1, are based on this activity.

After the wafer processing, the integrity of the wafer processing is evaluated by probing sites on the wafer that contain standardized device structures that are designed to evaluate process control. These test sites are stand-alone IC’s that are placed on the wafer either in place of a few primary IC sites scattered over the area of the wafer or in the scribe areas in between the primary IC sites. This test is intended to quickly identify any common catastrophic processing defects and to ensure accurate process control. If the wafer processing is found to be out of the manufacturer’s specification window; such wafers or the lots that include them may be scrapped prior to any functional testing. We should point out that the same device structures and/or additional ones on these test sites may be used to acquire the data for the SPICE models used in the simulation of the IC’s.

At the end of the wafer processing, every device (primary IC) on the wafer undergoes a set of performance or function related tests (commonly referred to as the test suite). The goal of this step is to eliminate DUT’s that fail to satisfy one or more of the expected performance specifications. Depending on the test philosophy of the IC manufacturer, the test suite used for wafer probing will either include a complete set of tests intended for the packaged devices or a subset. At this time, the bad devices are “electronically marked,” and this information is used in the next manufacturing step. The next step is to scribe the wafer and select the good dies for packaging. After the good IC dies are packaged, testing is again performed to ensure proper handling, wire bonding and packaging. The final test checks performance of the device over the specified temperature range.

A sample set of the qualified packaged IC’s is subjected to stress testing that is referred to as burn-in (i.e., operating the IC’s in an oven at elevated temperature for an extended period of time). After removing the devices from the oven, they are retested using the full test suite. The objective of this step is to eliminate the “weak” devices which are likely to fail during their early period of operation. This failure mode is referred to as “infant mortality” and it represents the initial portion of the aging or so called “bathtub curve” [6].

Finally, a smaller sample is retested, prior to delivery, for quality assurance (QA) purposes. Different manufacturers implement their own independent QA programs. However, the globalization of the microelectronics industry drives the establishment of QA standards such as the popular ISO9000 standard.

The repetitions of similar tests performed on every IC, makes the process appear inefficient. The number of repetitions is necessary to weed out bad IC’s as early in the manufacturing process as possible and to ultimately insure that no bad IC’s are shipped to customers. The cost associated with producing a bad device is magnified by a factor of ten as it propagates undetected through the chip and system manufacturing processes and ultimately to the field. Consequently, the number of tests and the total test time need to be balanced to achieve the requisite process quality assurance while keeping the manufacturing cost as low as possible. The feed-back of failure mode information to previous steps in the manufacturing process enables a closed loop control that is vital to continuously improving the efficiency and quality of the process. For this reason, simply limiting the number of tests performed at each step is usually an unacceptable cost reducing measure.

II. AUTOMATED TESTING

Historically, IC characterization and testing developed with the use of bench-top equipment. There are still parts, e.g., in the microwave and millimeter wave area, that can only be tested this way. These instruments have provided and continue to provide high performance and flexibility of use; both characteristics are very important during the characterization and debugging phases of IC development. As IC DUT’s became smaller and more complex, they also became more difficult to fully test on the bench. It also became important to have several synchronized instruments operating on the DUT simultaneously. This use of synchronized instruments became a vital approach for both the characterizing of IC’s in the R&D laboratory and the conduct of the production tests in the manufacturing environment. It was then seen that a streamlined interconnection of such instruments could simplify the entire testing procedure. At the simplest level, one instrument may trigger or control the instrument supplying the stimuli to the DUT or it may control the intervention of other measuring instruments.

The integration of a collection of interconnected and synchronized bench top instruments into a test station was marked by two significant developments. The first event was the introduction of standards for instrument interconnect and intercommunications; and the second was the availability of the microprocessor.

The IEEE 488 standard evolved in response to a growing demand for computer driven testing solutions. It evolved
Fig. 2. VXIbus electrical architecture (the power distribution bus is not shown) [92].

in the mid-1970’s out of the proposal for the byte serial protocol from Hewlett-Packard Company. At times it has been called the “ASCII bus” or the “General Purpose Interface Bus (GPIB)”. The standard [7] was designed to allow a user to easily interconnect GPIB configured instruments to each other and to a control computer (i.e., usually a PC with a GPIB plug-in card). It covers the communications protocols (for transmitting/receiving data and controlling communications on the bus), the multiconductor interconnection cables, and the plug-in fixtures.

The second breakthrough in the automation of bench top equipment was facilitated by the emergence of relatively inexpensive microprocessors, which enabled the development of more versatile and more reliable instrumentation. The fast development of digital VLSI rendered practical the incorporation of digitizing and data processing within the instrument. The inclusion of microprocessors enabled instruments to be developed that were easier to operate. The use of microprocessors also reduced operator error by eliminating most front panel controls and making the remaining controls more powerful.

These two developments lead to the evolution of new and more efficient protocols that advanced the integration and synchronization of instruments and computers.

The early 1980’s saw an emergence of VME (Versa Module Europa) computer bus technology. It began with Motorola’s VERSAbus. After adopting Eurocard module dimensions, VERSAbus became VMEbus (IEEE 1014 standard, 1987). This new standard provided specifications for an open architecture computer bus with wide bandwidth. The protocol for VMEbus proved to well be suited for a wide variety of computer plug-in cards; but is not so for data acquisition boards. Consequently, VMEbus was never well accepted by instrument manufacturers.

In the late 1980’s, a number of technical representatives from the instrumentation manufacturers formed a committee to formulate the additional standards necessary for an open architecture instrumentation bus based on VMEbus and the IEEE 488 standards. This gave birth to the VXIbus, an acronym that stands for VMEbus Extension for Instrumentation. The VXIbus can be logically grouped into eight buses, as shown in Fig. 2. Global buses are accessible and shared by all VXI modules. Unique buses are routed from the slot 0 module (the main control unit) to other modules on a one-to-one basis. Private buses are local buses between adjacent modules [92].

VXIbus enables the control of signal characteristics and propagation delay via a well defined backplane environment [8]. With tighter electrical characteristics comes greater flexibility and higher bandwidth communications between instruments. VXI provides modularity and ease of use, while maintaining compatibility with GPIB. The growth in high volume discrete electronic component manufacturing (resistors, capacitors, diodes, etc.), and the need for repeatable measurements, further stimulated the automation of existing test methods.

At the time of the development of the GPIB standard, semiconductor and discrete component manufacturers like Fairchild, RCA, Western Electric, TI, etc. began building their own automated testers. These developments were driven by the pressure of increasing demand for higher IC production and the associated need to perform large volume batch testing. The fact is these “homegrown” systems were very difficult to build reliably and they conformed to few if any standards.

High demand in the consumer electronics market, coupled with the fact that it was difficult and expensive to build the test equipment in-house, created the right environment for the emergence of the third party manufacturers of automated test systems. ATE to test digital IC’s appeared first; and ATE for digital and analog IC’s were separate systems. The analog and mixed-signal ATE industry was started when Teradyne, Inc. and the LTX Corporation were founded in the late 1960’s,
and the early 1970’s, respectively. These companies began by developing automated test equipment (ATE) to test linear analog IC’s, where the void was greatest. Over the next several years the capabilities of their ATE products evolved to serve the testing needs of mixed-signal (digital and analog) IC manufacturers. In Fig. 3 we graphically show the time-line for the evolution of ATE technologies. It can be debated whether the development of “analog only” ATE has disappeared or not. The fact is that today’s mixed signal ATE’s, even if equipped with “analog only” instruments, rely totally on digital signal processing (DSP) based measurement methods (i.e., the measured analog signals are digitized and DSP algorithms are used to extract the desired performance parameters). For this reason Fig. 3 shows the development of “pure analog” or “analog only” ATE to have ended with the emergence of mixed-signal ATE. Moreover, the trend among digital ATE vendors is to offer ATE’s with some mixed signal capabilities. Thus, the contemporary ATE industry offers products with varying ratios of analog and digital functionality (i.e., “big D little A” or “big A little D” configurations and variations in between).

Mixed-signal ATE systems are sophisticated computer controlled systems which perform automatic testing of DUT’s that include single components, packaged and bare IC’s, circuit boards, and complete systems. The allocation of the ATE’s functionality and the control of its operation are achieved with software. The ATE generates and applies the stimuli to the IC, it senses and digitizes the IC’s responses, and it analyzes these responses. Consequently, contemporary ATEare comprised of the following five functional modules: STIMULUS, MEASUREMENT, TESTER CONTROL, PROCESSING, and SIGNAL HANDLING; as shown in Fig. 4.

The TESTER CONTROL, i.e., the top block in Fig. 4, controls the entire ATE under the guidance of a test plan. It establishes the controls for the PROCESSING, MEASUREMENT, and STIMULUS blocks needed to implement the test plan. Test plans are written in a high level programming language. Due to its efficiency, modularity, and versatility, C language has become the most popular language for this task. It is also in this portion of the ATE where the interface (menus and icons) between the test developer (and ATE operator) and the ATE is determined. The PROCESSING block provides computing power necessary for preprocessing the data that is to be sent to the STIMULUS block. The STIMULUS block, in turn, is responsible for the final shaping of the signals that are to be applied to the DUT. The PROCESSING block also does the postprocessing of the digitized signals provided by the MEASUREMENT block. The SIGNAL HANDLING block embodies all the hardware used for routing the signals to and from the DUT.

In addition to the functional partitioning shown in Fig. 4, every ATE is physically comprised of a test head connected to a main cabinet containing the processor and the instruments. The physical appearance of a typical ATE is shown in Figs. 5 and 6. The main cabinet houses the STIMULUS, MEASUREMENT, PROCESSING, and TESTER CONTROL blocks. SIGNAL HANDLING is a primary the function of the ATE’s test head. It also includes signal routing through adapters, fixtures, and cables between modules in the ATE and the DUT. Thus, signal handling is an area that requires special consideration. The amount of degradation experienced by signals, especially for analog signals at high frequencies, passing through switch contacts and cables cannot be underestimated [9].

Because the signal handling requirement is unique to an ATE, the development of this hardware is very closely tied to the growth of the ATE industry. The instrumentation found in the main cabinet, on the other hand, evolved separately with little influence from the ATE industry except to make them programmable and compact. Most of these instruments were developed as bench-top (stand alone) units as early as the 1950’s. Simple hardware controllers were used in the 1950’s but true automation occurred only subsequent to the availability of low cost, powerful microprocessors.

Originally ATE vendors used in their equipment a mix of proprietary instrument interfaces with GPIB controllers. Subsequent ATE models incorporated prevailing instrument and computer bus standards. The emerging bus standards have been incorporated within later ATE generations to various extent. Today, this trend continues, with majority of ATE industry converging on VXIbus based instruments and several
vendors introducing optical fiber as means of communicating between internal subsystems.

In addition, the performance of the instruments available within an ATE framework has undergone a tremendous improvement. Today’s ATE provides a measurement environment with a noise floor between 120 and 140 dB. This type of environment is necessary in the testing of high resolution analog-to-digital and digital-to-analog converters. Similarly, RF testing also requires a very low noise environment for low signal power measurements. Since today’s ATE was developed using IC’s developed in yesterday’s technologies, even the most advanced ATE is challenged to test IC’s that represent the latest state-of-the-art. For example, the increasing performance of IC’s for storage devices is resulting in increasingly more stringent demands on the timing parameters of today’s ATE’s. The clock jitter (phase noise) of no more than 10 ps rms is required to properly test the read channel IC’s that are realizing more than 100 Mb/s. data rates. Some of the mixed-signal ATE vendors provide special modes which increase the digital capture rates up to 400 MHz. Table I gives a general list of the instruments available in a truly mixed-signal ATE. The parameters listed in this table represent typical values, and they are often the differentiating factors that drive the IC manufacturer’s choice between the ATE’s offered by different vendors.

One of the first obstacles the ATE industry had to overcome, was signal handling and conditioning. As stated in the intro-
duction, there are two embodiments of an IC DUT that the ATE has to interface with, i.e., die on a wafer and package. In both cases the signal path from an ATE to the DUT is routed through a multilayer device interface board (DIB), such as that shown in Fig. 7. Device interface boards can be either square or round. The round DIB’s have diameters between 12 in and 18 in, depending on the tester type. Typically the DIB’s are constructed with 2–4 separate, uncommitted planes (layers) which can be used for separate ground planes and shielding. In addition the DIB’s have planes (layers) dedicated to set power supplies (5V, 15V, etc.). The access to ATE resources is gained via contact pads radially located on the ring around the perimeter of the board. These pads make contact through the spring loaded coaxial pins to the resources located in the test head.

During the wafer test, the signals are delivered to and from the IC via probe card [3]. To accommodate such interface, the device interface board has an opening in the center (usually 3 to 5 inches in diameter). The small pads are located on the perimeter of that opening. The interconnection between the probe card and the device under test board is achieved through the spring loaded shielded pins. To maintain the signal integrity of the connection between the probe card and the IC, this interface has to be very reliable and resilient. Probe card resiliency is specified in hundreds of thousands of touchdowns (typically 100,000 to 300,000). The three most commonly used probe card types are the ceramic blade, metal blade, and epoxy ring. The choice of a probe card style is dependent on different factors such as maintenance and signal aberrations. Fig. 8 shows an example of a probe card used for testing of the low pin count devices.

The diameter of a probe card ranges anywhere from 4 to 8 in, depending on the test system. The diameter of the probe tip is usually between 5 and 15 mils (where 1 mil = 0.001 in). Most commonly used materials for standard probes are tungsten, rhenium tungsten, beryllium copper, and palladium. The planarity of the probes depends on the chip area and typically ranges from less than 0.5 mil for a small die to below 1 mil for a large die. The probes are laid out radially with ground layers placed in the way that allows placement of bypass capacitors as close to the probes as possible.

A considerable amount of effort is currently being devoted to the development of high speed and RF probing. A recent utilization of the same technologies that are used in IC manufacturing, leads to introduction of higher density and higher performance probe cards [4], [5], [89].

Packaged IC’s are tested by placing a socket adapter on the DIB. The physical admissions of the packages are very
different for different package types. They also exhibit very different electrical characteristics. The important issues in selecting the socket type are the lead inductance of high speed (>10 MHz) paths and the series resistance of the leads. These characteristics affect the fidelity of the signals brought in and out of the DUT. The most prominent vendor names in the socket adapter industry are Yamaichi and Johnstech. As an example, Fig. 9 shows a socket for a 28 PLCC package mounted on a DIB. Shown is a close-up of the center of the DIB with a mounted socket adapter.

The type of socket adapter shown in Fig. 8 is used during “hand testing,” that is when the devices are inserted into a test fixture manually. For large volume automated testing this socket is removed and the DIB is directly connected to the automated handler. Automated handlers are the instruments which bring DUT’s into contact with the DIB. After the test is
completed, the automated handler places the DUT in the appropriate bin, e.g., separate bins for good and bad devices (the details of the handler operation are determined by commands in the test plan). Some products, e.g., microprocessors, are tested to more than one performance criteria; thus, additional bins are used to separate parts that satisfy the different criteria.

The second significant achievement in the ATE development was the simplification of the interface between the ATE and the test developer/operator. It was largely the computational power and programming flexibility of the DSP, coupled with the emergence high performance A/D and D/A converters, that enabled the development of user friendly and flexible virtual instruments.\textsuperscript{4} In today’s ATE, test instruments for specific applications (e.g., video, telecommunications, hard disk drives, etc.) are created by configuring the ATE’s resources using software.

\textsuperscript{4}Using analog channel/digitizer/DSP and flexible software, it is possible to generate various instruments based on the same principles of digitizing events and digital signal processing.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typical Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage force range resolution</td>
<td>±0.5V to ±60.0V 12 to 14 bits</td>
</tr>
<tr>
<td>Voltage measure range resolution</td>
<td>±0.5V to ±60.0V 12 to 16 bits</td>
</tr>
<tr>
<td>Current force range resolution</td>
<td>±1mA to ±200mA 12 to 14 bits</td>
</tr>
<tr>
<td>Current measure range resolution</td>
<td>±3.7μA to ±200mA 12 to 16 bits</td>
</tr>
<tr>
<td>Meter input impedance</td>
<td>up to 1 GΩ</td>
</tr>
<tr>
<td>Precision Waveform Sources and Digitizers</td>
<td></td>
</tr>
<tr>
<td>Bandwidth</td>
<td>10 to 500 kHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>16 to 22 bits</td>
</tr>
<tr>
<td>Distortion</td>
<td>75 to 110 dB</td>
</tr>
<tr>
<td>High Speed Waveform Sources and Digitizers</td>
<td></td>
</tr>
<tr>
<td>Bandwidth</td>
<td>1 to 10 MHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>10 to 12 bits</td>
</tr>
<tr>
<td>Distortion</td>
<td>40 to 60 dB</td>
</tr>
<tr>
<td>RF Sources and Measurments</td>
<td></td>
</tr>
<tr>
<td>Frequency Ranges</td>
<td>0.001 to 6GHz</td>
</tr>
<tr>
<td>I/O power</td>
<td>-130 to +30dBm</td>
</tr>
<tr>
<td>2 port S parameter measurement range</td>
<td>-70 to +20dBm</td>
</tr>
<tr>
<td>Digital Input/Output</td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>up to 50MHz\textsuperscript{*}</td>
</tr>
<tr>
<td>Number of Formats</td>
<td>10 - 13 (drive and compare)</td>
</tr>
<tr>
<td>Data Capture</td>
<td>up to 50MHz\textsuperscript{*}</td>
</tr>
</tbody>
</table>

\textsuperscript{*} - purely digital ATE’s provide much higher digital rates

Some of the mixed-signal ATE vendors provide special modes which increase the digital rates and digital capture up to 600MHz.
For the initial “home grown” ATE systems, the human-machine interface was the low level machine language code prepared by the test engineer. The design and implementation of tests in these early systems were encumbered by an interface that had its own steep learning curve. As time progressed the programming evolved to higher level languages, i.e., FORTRAN, Pascal, and C, and to a window based graphical user interface (GUI). With a GUI the test development environment evolved into one that is intuitive and easy to navigate. Moreover, it freed the test engineers to focus their efforts on the important testing issue rather than writing and debugging code. Fig. 10 shows an example of the program development window for a typical ATE. We see buttons or icons for file management, program compilation and launching, program and test debugging, and many other utilities designed to make the test development easier. Here the user can select a set of functions to be included in the test plan, start the execution of the program, stop the execution at any arbitrary point, and direct the flow of the output data.

There are many utilities which allow the user to interrogate the current states of the ATE and to change them, if desired. All the information describing the state of each instrument is available in form of windows. The user can verify and/or change the settings of voltage/current levels, select among available filters, select the mode of operation, timing sets, etc. All these capabilities are available through an easy to follow point-and-click environment. The examples of such utilities is shown in Fig. 11. The panel in this figure left shows graphical representation of the arbitrary waveform generator (AWG). It also shows the status of the connections and the waveform parameter settings. The user is permitted to change some of the waveform parameters when the program is stopped at a break point.

When digital inputs are needed, digital pattern editing resources are available at the click of a button. Fig. 11 shows the digital pattern editor window. The window is divided into three areas; namely, a spreadsheet style pattern display, a graphical pattern display, and a text timing and vector display. Through this window, the user can change and monitor the timing relations between various digital signals. The spreadsheet style display section allows the user to input instrument specific instructions. This allows triggering of the signal generators and digitizers. These instruments are built with ADC’s and DAC’s, therefore the time when the samples are sent out of the instrument can be precisely controlled.

The graphical waveform analyzer is shown in Fig. 13. Data stored in any numerical array can be displayed and edited in this window. Data contained in a previously stored file can be read and displayed using this tool, as well. The generation of data segments for arbitrary waveform generators (AWG) can also be accomplished with this tool. The data obtained by the digitizer or the digital capture instruments can be displayed here too. The ATE will update these displays when ever the program is restarted or suspended at a break point.

The important functions of data logging and the binning of results are governed by the test plan. Fig. 14 shows a typical data log or results window. The data output can be saved in various file formats and later used for further analysis. This window shows an easy to read way of presenting numerical values of data measured and/or calculated during tests, as defined in the test plan.

Test program development is completely under the test engineer’s control. Any valid application within the software system can be opened during development or debugging sessions. All mixed-signal ATE vendors provide test development environment emulation software that can be used on any workstation or PC connected to the network that includes the ATE. This arrangement allows for easy transfer of data and test programs between the ATE and the engineer’s desktop computer. As a result, most of the test development can be performed prior to the physical availability of the DUT.

The easy to use ATE environment described in this paper is in effect a direct port of advances that have made workstations and PC’s more intuitive and friendly to use. The drive to sim-
plify ATE programming will continue until the state is reached where the software driving the system is transparent, and the test engineer can solely concentrate on generating the test plan and analyzing the results. Many ATE vendors are seriously pursuing the integration of the IC design and test activities into a single “user friendly” environment. Computer models that emulate the ATE are being developed to be incorporated into the same CAD tools used during the design phase. This will allow the test engineer to exercise the model for DUT (i.e., SPICE or HDL) within an emulated test environment. It is anticipated that this combined environment will yield a better understanding of the DUT’s functionality and testability, and a more efficient and robust overall test strategy.

III. DIGITAL TESTING

A. Methods

In the 1970’s and 1980’s, there was a major divergence between the growth paths for analog and mixed-signal circuits on one hand, and digital circuits on the other. Digital circuits experiences an exponential growth in their level of integration and performance.

This is illustrated in Fig. 15 for the case of microprocessors which are perhaps the best symbols of the rapid increase in complexity and performance of digital circuits. A major consequence of such growth in complexity was that conventional testing techniques, dubbed functional techniques, were no longer sufficient for digital circuits. Instead, a host of new techniques were developed to meet the challenge of testing complex digital circuits. At the same time, the evolution of test equipment, including ATE, was also driven by the need to test such complex yet high-performance digital circuits. The variety of test techniques for digital circuits, available today, can be broadly classified into the following categories:

1) functional testing which relies on exercising the DUT in its normal operational mode, and consequently, at its rated operating speed; 2) testing for permanent structural faults (like stuck-at faults, stuck-open faults, bridging faults, etc.) that do not require the circuit to operate at rated speed during test; 3) testing based on inductive fault analysis in which faults are derived from a simulation of the defect generation mechanisms in an IC (such faults tend to be permanent, and do not require the circuit to be tested at rated speed); 4) testing for delay faults that require the circuit to operate at rated speed during test; 5) current measurement based testing techniques, which typically detect faulty circuits by measuring the current drawn by the circuit under different input conditions while the circuit is in the quiescent state.

The functional approach to testing, which relies on exercising the DUT in its normal operational mode, is the oldest method of testing and verifying the operation of digital circuits. In this approach, the designer and/or test engineer generate sequences of input patterns, dubbed test vectors sequences, given the design details at different levels of abstraction. The popularity of this approach stems from the following two reasons: 1) such tests verify that the circuit operates according to specifications, at least under some input conditions, and 2) the test vectors are easily derived by simply formatting the test cases used by the designer during creation of the design, thereby saving test generation time. Moreover, functional tests are well known to detect a reasonably large percentage of the faults in an IC.

However, the functional testing method has some major shortcomings, as well [56]. Foremost among the deficiencies

The literature on most of the topics to be covered in this section, is vast. Consequently, only a few representative works are discussed and/or cited, in the discussion that follows.
Fig. 15. Graphs illustrating growth in CPU and memory size (number of transistors).

(a)  
![Graph showing number of transistors per chip over years](image)

(b)  
![Graph showing chip area over years](image)

The fact that test sequences generated using the functional approach tend to be unacceptably large for all but trivial digital circuits. For example, a thorough functional test set for a 32-bit adder with carry input to the least significant bit-position, requires the application of about $2^{32}$ input patterns. This is an impossible proposition for even the fastest ATE available. Moreover, a 32-bit adder represents only a small portion of complex digital circuits like microprocessors. Testing circuits like microprocessors using functional tests alone, is not even remotely feasible. Fault coverage of functional test vectors has also come under increasing scrutiny as the stringency of test specifications have grown over the years. While functional test vectors tend to detect a large percentage of faults in an IC, they also tend to miss a nontrivial percentage of faults. At the present time, functional test vectors are typically fault simulated to estimate their fault coverage, which can be a computational resource intensive process that offsets the advantage of easy test vector generation. Furthermore, the correlation between fault coverage estimates obtained via fault simulation, and the ability of functional test vectors to identify failing IC’s, can be poor. Thus, fault coverage estimation for functional test vectors remains an open issue, thereby limiting the usefulness of functional vectors in today’s environment of tight quality control.

Structural fault model based test techniques represent the most thoroughly investigated alternative to the functional testing approach since the 1950’s. A fault model is usually an artificial model of failures in digital circuits, such that tests for such faults in an IC expose actual failures in the IC. The earliest, and the most widely used structural fault model is the single stuck-at fault model, in which one interconnection line between low-level design units (like gates) is assumed to be permanently stuck at a logic value 0 or 1, one at a time. This is illustrated in Fig. 16 for a simple digital circuit. While this fault model may appear to be a highly artificial one, experience has shown that this fault model can be very useful in identifying faulty IC’s. Moreover, experience and theoretical investigations suggest that test vectors generated using the single stuck-at fault model are usually effective in identifying faulty chips in the presence of multiple faults which rarely mask each other’s impact on circuit behavior, completely.

Furthermore, the behavior of a digital circuit in the presence of a stuck-at fault can be mathematically analyzed using Boolean algebra. Numerous techniques to identify test vectors that expose specific stuck-at faults in a given design purely Boolean-algebraic, search-algorithm based, and some combination of the two have been developed over the years, using this fault model. Many of these techniques, have been implemented in commercial CAD tools, and are used throughout the semiconductor industry today. The major problems with the stuck-at

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Fault simulation efficiently simulates and compares the behavior of a given circuit in fault-free condition, to its behavior in the presence of one or more well-defined faults (in accordance with a selected fault model.)

Another common name for this fault model being the single stuck-line or SSL fault model.

This process is commonly referred to as test pattern generation (TPG), and with the proliferation of computer implementations of various methods for TPG, as automatic TPG or ATPG.
fault model are twofold: 1) the computation process to identify tests (TPG, see footnote 2) can be extremely resource and time intensive and 2) the stuck-at fault model is not good at modeling certain failure modes of CMOS, the dominant IC manufacturing technology at the present time.

Consequently, alternative fault models like transistor stuck-OPEN and stuck-ON fault models [24], [39], [51], [78], and bridging fault models [27], [52], [58] have gained popularity in recent times. Efforts have also been made to develop effective TPG tools that use very low-level circuit models called switch-level models [21], [48]: switch-level circuit models use primitives that fall in-between transistor-level models like those used for SPICE simulation, and gate-level circuit models that are commonly used with the stuck-at fault model. At the present time, the search for alternatives to the stuck-at fault model that are better suited for CMOS circuits, and the search for computer implementation techniques for TPG that require less time and computing resources, continue to be active areas of research. Simultaneously, the stuck-at fault model continues to be widely used for generating test vectors which are likely to expose failing IC’s that are not identified as faulty by other testing techniques.

Recognition of the limitations of the permanent fault models for digital circuits, especially in CMOS technology, has led to the development of an interesting approach to fault modeling, designated inductive fault analysis (IFA), and more recently, inductive contamination analysis (ICA) [37], [40], [53], [59], [69]. In these approaches, candidate faults in a given circuit are first identified through simulation of the recognized modes of failure (like particle contamination) in a specific IC manufacturing process, applied specifically to a given layout of a given circuit: an overall view of IFA is shown in Fig. 17 based on the framework presented by Ferguson and Shen [40]. The resultant faults consist of deviations in the various layers of the IC, from the designed layers, like extra blobs of metal causing short between two wires, breach in the gate oxide, etc. The impacts of these faults on the behavior of the given circuit are then extracted via simulation, and are usually modeled as permanent faults. Tests for these permanent faults are generated in a final step, typically by means of some computerized search procedure. The main advantage of IFA is that it uses detailed process information to decide on a list of target faults, and hence, can claim the resultant list of faults to be “realistic” as opposed to “artificial” as is the case with the stuck-at fault model. A major problem of IFA, however, also stems from this reliance on detailed process simulation, the procedure is resource and time-intensive, leading to high cost.

Delay faults represent a different face of fault model based testing in which faults are assumed to affect the performance of the circuit, without affecting its functionality. In other words, a circuit with delay fault is presumed to operate correctly at sufficiently low speed, but does not operate correctly at the rated speed. At the present time, delay faults are broadly classified into two categories: 1) gate delay faults, where the delay fault is assumed to be lumped at some gate output and 2) path delay fault, where the delay fault is the result of accumulation of small delays as a signal propagates along one or more paths in a circuit. Although delay faults were studied in some depth as early as 1985 [55], interest in delay faults have picked up only since the late 1980’s. A slew of automatic TPG or ATPG techniques for delay faults, under various assumptions of observability and controllability of the internal flip-flops in a digital design, have been developed [17], [28], [30], [34], [43], [50], [60], [67]. As with stuck-at faults, these techniques use computerized search algorithms, or some combination of Boolean algebraic processing and search, to identify the test vectors for delay faults. Unlike tests for stuck-at faults where the impact of a fault is usually not completely masked by the presence of other faults in the DUT, tests for delay faults can suffer from a problem of robustness, i.e., a test for one delay fault may be invalidated by excess delay in parts of the circuit that are not the target of the test being applied. For an excellent discussion of robustness of delay faults and the relationship between robust tests for gate and path delay faults, the reader is referred to [67].

For common digital circuits of today, e.g., those manufactured in CMOS, all of the previous testing techniques rely on voltage measurements during testing to determine whether the DUT operates according to expectation, or not. Techniques that are based on the measurement current represent an orthogonal approach. In such methods the current consumed by the DUT is measured, under different input conditions, to decide whether the DUT is good or bad. Since high-precision current measurement is usually a slow process, taking several milliseconds, almost all of the current measurement based testing techniques rely on the measurement of quiescent current of the DUT, for different input conditions [62], [73]. Such techniques are commonly referred to as IDDQ test techniques. Some studies have also been made about the possibility of using current measurements while the circuit is not in quiescent mode [57], [77], but this approach remains a research topic, at this time.

**Fig. 17. Framework of fault extraction in CMOS circuit using IFA, as presented by Ferguson and Shen [40].**
nanoamperes at most, for state-of-the-art processes, assuming supply voltages in the range of 2.0–4.0 V. Hence, if the DUT consumes significantly more current in the quiescent state, e.g., tens to hundreds of microamperes, the DUT is judged to be faulty. Such increased levels of $I_{DDQ}$ can be caused by a variety of factors like metal-to-metal shorts, defective transistors, etc. However, depending on the actual failure mechanism, some of these faults may not be caught by any other test method except for a nearly exhaustive functional test set—which, as discussed earlier, is impractical. Recent studies [56], have confirmed the routine occurrence of such faults in CMOS circuits, thereby boosting the case for $I_{DDQ}$ testing significantly. Related studies have also shown that there is a good correlation between failure in $I_{DDQ}$ tests, and early life failure of IC’s, i.e., $I_{DDQ}$ tests can also act as good indicators of potential reliability problems for IC’s. The major disadvantage of IDDQ testing is the fact that high-resolution current measurement is a very slow process, even with state-of-the-art test equipment. As a result, $I_{DDQ}$ tests are usually very costly in tester time, in a production environment. Moreover, classification of chips that fail $I_{DDQ}$ tests only, but pass all other functional tests and structural fault model based tests, is usually a hard problem on account of the cost of rejecting “good” DUT’s.

Testing of digital circuits usually goes hand-in-hand with design-for-testability (DFT) which represent design principles and methodologies aimed at enhancing the controllability and observability of internal nodes in a circuit, with minimal area and performance overhead. DFT techniques can be classified into two broad categories: 1) ad hoc techniques, and 2) systematic techniques. Ad hoc DFT techniques are usually applicable to specific designs only, but cannot be generalized to cover many different types of designs. They include such measures like control and observation point insertion, as illustrated in Fig. 18, and the partitioning of long counters and shift-registers, etc. Systematic DFT is essentially another name for structured, modularized digital design methods which are reusable, and hence, can be used with a variety of designs, have minimal dependence on chip parameters, and are usually highly automated.

Among the variety of systematic DFT techniques that have been investigated by researchers, scan design methods are possibly the most well-known and widely used methodology. The foundation of scan design lies in the Huffman model of sequential circuits shown in Fig. 19; whereby any arbitrary sequential circuit can be viewed as a composite of one combinational logic block and one or more memory elements, with every feedback loop from output of the combinational block to its input(s) passing via a memory element; the memory elements are clocked latches or flip-flops in the case of synchronous designs. In scan design methodology specially designed memory elements are used so that all, or some subset of these memory elements can be fully controlled and observed via some special access mechanism in the test mode: such access mechanism usually consists of one or more shift registers designated scan chains9 formed out of the memory elements themselves, or of a 2-D grid-like access mechanism. This basic idea has been implemented in numerous variations by many CAD tool vendors and digital IC vendors, some of the notable ones being: 1) multiplexer-scan commonly designated as MUX-scan (virtually all DFT tool vendors support this approach, which can be attributed originally to Williams and Angell [81]); 2) level sensitive scan design commonly designated as LSSD (IBM) [38]; 3) scan path (NEC) [45]; 4) modular port scan design or MPSD (TI) [65]; and 5) scan/set logic (Sperry-Univac) [76]; and 6) random access scan (Fujitsu) [18], etc.

When all memory elements in the DUT are replaced with scan elements, the design is designated as full scan design. The main advantage of full scan design is that it converts a sequential circuit (which has feedback loops and memory) into

9Of course, one needs to verify that the scan chain itself is fault-free, which is not a hard problem if some constraints are imposed on the types of memory elements that can be used in the circuit.
a combinational one (with no feedback loops or memory) for testing purposes; which in turn, simplifies test generation for the DUT considerably. If some, but not all, of the memory elements are replaced with scan elements, then the design is designated a partial scan design [54]. Experiments show that with careful selection of the scan elements, partial scan designs can often have most of the benefits of full scan design. This can occur even though the resultant partial scanned design has memory elements in it, in the test mode. Of course, depending on the number of flip-flops scanned, the overhead due to the partial scan can be significantly less than the area overhead of full scan.

In 1990, IEEE approved the standard 1149.1 test access port and boundary scan architecture [49] for digital circuits, which recognizes scan as the key component in easing testing problems for large digital circuits and systems. This standard is commonly referred to as the Joint Test Action Group (JTAG) standard, since it was developed by the JTAG consisting of members from Europe and North America. It is also referred to as boundary scan, since a major part of the standard is based on the use of special scan cells at the boundary of IC’s. This standard establishes a systematic design procedure for chips and boards, with guaranteed access to chips fully assembled on aboard. A schematic view of the DFT structures in a board employing boundary scan for all its chips, is given in Fig. 20.

Any design compatible with IEEE Standard 1149.1 must have a few key components: 1) a test access port (TAP); 2) a TAP controller; 3) an instruction register (IR); and 4) some mandatory test data registers (TDR’s). The TAP controller, IR, and TDR’s constitute the test logic indicated in Fig. 20. The standard specifies the behavior of the TAP controller, and some mandatory instructions that must be supported by the test logic. In addition, the standard allows manufacturers of IC’s to include additional TDR’s, and to support additional instructions, which may be revealed to the buyer (public instructions) or may not be revealed to the buyer (private instructions). A typical organization of the test logic in a JTAG-compliant IC is shown in schematic, in Fig. 21. For an excellent discussion of the JTAG standard, implementations of the various parts of the test logic, and useful extensions to the specified standard, e.g., simultaneous access to multiple scan chains under the control of private instructions, the reader is referred to [63].

DFT techniques for circuits possessing regular and repeated structures have also received tremendous amount of attention, over the years. It was shown as early as 1973 [42] that ripple-carry adders (recall the difficulty of functionally testing a 32-bit adder) can be tested very thoroughly, assuming no more than one adder stage is faulty at a time, using only eight tests, independent of the size of the adder; this is illustrated in Fig. 22. Whenever a circuit has this property, it is designated C-testable [42]. It has been shown that with the use of appropriate DFT techniques, test set sizes for many useful arithmetic circuits like ALU’s, multipliers, etc. can either be made constant (i.e., the circuit can be made C-testable), or made to grow very slowly with circuit size [26], [29], [35], [71], [74]. At the same time, it has been shown that microprocessor-like circuits (designated instruction-set processors) which have a well-defined register-transfer model, can usually be tested thoroughly using register-transfer operations can be used to exercise different parts of the DUT [20], [31].

As digital circuits have grown large, and as the availability of transistors/gates on an IC has steadily increased with improved fabrication technologies, various techniques have been developed to include some testing functionality into the logic itself: this is commonly referred to as built-in self test or BIST. While the idea of a digital circuit testing itself is many decades old (for example, the earliest switches from AT&T had some self testing capabilities) the use of BIST in commercial designs has become popular only recently. The general structure of a digital circuit using BIST is shown in Fig. 23. Response verification in BIST is usually done by comparing the response of one part of the circuit, with the response from another part (in the case of regular circuits), or using feedback shift registers acting as signature analyzers [13], or some combination of the two.

There is, however, wide variation in the circuitry used to generate patterns, when using BIST, depending on the type of patterns that are generated. The types of patterns used in BIST range from deterministic [15], [41], [64], [80], [82], which is typically used with highly structured circuits like...
Over the last couple of decades, evolution of ATE aimed at complex digital circuits mirrors the tremendous growth in the variety of testing methods for digital circuits. The features that have emerged as the key to effective testing of very high-speed complex digital parts are: 1) independent control and observation capability for each pin of the DUT; 2) real-time timing control, allowing timing of a test pattern at any pin to be changed in any cycle; 3) built-in calibration subsystems; 4) presence of a high-performance host processor to manage operations of the various ATE subsystems, and to provide a workstation-like user interface; 5) a rich software environment that integrates CAD tools and database management system with the test operating system to provide a seamless path from pattern files generated by designers and/or ATPG tools, to actual waveforms being applied to, or observed at, the pins of the DUT; and 6) development of sophisticated mechanical structures that can act as an effective interface between the advanced electronics of the ATE and that of the DUT. As mentioned in Section II, the instrumentation present in most state-of-the-art ATE is more or less similar, nowadays. This is true, individually, within the class of ATE aimed at digital circuits and the class of ATE aimed at mixed-signal circuits. However, there is still considerable difference in the focus of instrumentation between these two classes of ATE. The key issues of instrumentation and software environment of ATE have already been discussed, in significant detail, in Section II, and hence, are not repeated here.

The primary problems faced by ATE aimed at purely digital circuits, is the rapidly increasing performance of digital circuits that constitute the DUT’s. Today, large 200 MHz digital circuits (like CPU’s) are becoming commonplace, 500 MHz digital circuits are expected to become commonplace in the next few years, and large 1 GHz digital circuits are being contemplated. Problems faced in testing these kinds of ultra high-speed digital circuits are twofold: 1) the ATE available often does not have the instrumentation necessary to test the DUT at the rated speed; 2) analog circuit problems are creeping back into the business of testing digital circuits. Recently, considerable effort has been focused on the former problem, with the primary goal of formulating techniques to test ultra high-speed digital circuits using lower speed ATE [14], [16], [23]. The latter problem remains essentially an open issue.

IV. MIXED-SIGNAL TESTING METHODS

During the period of explosive growth in the size and complexity of digital IC’s, the growth in size and complexity of mixed analog-digital IC’s (including operational amplifiers, voltage regulators, ADC’s and DAC’s) was modest in comparison. The most dramatic advancements in mixed-signal circuits during the past two decades have been in performance, e.g. resolution, signal-to-noise, and signal bandwidth, as opposed to size or complexity. These developments lead to more stringent requirements and challenges for the analog instrumentation. They have also enabled significant advancement in the data acquisition capabilities of ATE. Consequently, the vendors of analog ATE concentrated their efforts on developing new circuit design techniques to improve their product’s performance in the areas of nonlinear distortion, resolution, bandwidth, low noise, etc. needed to support emerging analog and mixed-signal IC’s. Nonetheless, perhaps the three most significant advances in the development of mixed-signal ATE were auto-calibration, DSP based measurements, and the improvement of the test plan development and debugging environment.

The accuracy of analog instruments is limited by component variations over temperature changes, random differences between replaced components, and component drift over extended periods of time. Given a specific set of components, system errors due to the temperature variation can be minimized by bringing the instrument to the thermal temperature constant. The elevated temperature is selected because it is easier to control the heating of the instrument than its cooling. This method has been in use for many years in the bench-top instrumentation environment. To eliminate the remaining errors within the measurement instrumentation, the calibration of the instrument is required immediately before or after each measurement. Variations of this method are used throughout the ATE industry in the form of auto-calibration [10], [11]. The test system monitors changes in the environment and automat-
ically adjusts some of its instrumentation parameters (delays, offsets, etc.). Some of the problems associated with calibration are eliminated due to better temperature and relative humidity control in today’s facilities, and tighter tolerances on the components used within instruments.

Arguably the most important advancement in evolution of mixed signal ATE was the introduction of DSP techniques into the world of measurement and instrumentation. It should be pointed out that DSP’s would have found limited use in analog ATE if it were not for concomitant advances in analog-to-digital converter (ADC) and digital-to-analog converter (DAC) devices. The important feature of sampled systems and digital signal processing is the fact that once the signal is captured/digitized, with the microprocessing power available, the engineers have control of virtually any set of variables they choose [12]. The introduction of sampled systems, digitizers and arbitrary waveform generators, made it possible to perform synchronization between events on a sample (vector) by sample basis [83], [84]. Because of this, the DSP based testing offers the benefits of accuracy, flexibility, throughput, and repeatability which are not as easily realizable with continuous time-based instrumentation. In addition, conventional analog instruments are much less accurate in measuring dynamic parameters than they are in measuring constant events. This weakness is totally eliminated by application of the DSP-based instrumentation [83].

DSP techniques combined with the advances in IC technology led to many new and imaginative ATE solutions. A full synchronization of analog and digital systems within today’s ATE’s simplifies the dynamic testing by application of the coherence principle [83]. Coherent testing is a systematic method for testing unknown or arbitrary wave shapes. When a sinusoidal waveform with frequency $F_s$ is sampled at the rate of $F$, one can define a unit time interval comprised of $M$ signal cycles and $N$ sampling intervals. If $M$ is a prime number and the relation in (1) holds, then the samples within this unit time interval are unique. In other words

$$\frac{F}{F_s} = \frac{M}{N}$$

(1)

this coherence ensures that the location of the $N$ samples is controlled and repeatable. A longer waveform can then be constructed by graphically superimposing several unit time intervals. If the waveform is $K$ unit time intervals long and (1) is satisfied, then the resulting pattern will be comprised of $K$ repetitions of the same $N$ samples. $N$ is typically chosen to be a power of two to accommodate fast Fourier transform (FFT) algorithm. The application of the coherency principle makes testing of data converters more efficient and reliable by simplifying the analysis of the spectra resulting from the FFT and Chirp-Z transforms of the time domain signals. This way the dynamic performance, e.g., signal-to-noise (SNR), total harmonic distortion [THD], can be reliably tested [85]. In addition, typical data converter parameters such as the linearity, quantization error, missing codes, and the settling time can be tested with more flexibility.

The decreasing cost of DSP’s has enabled DSP’s to be allocated on a per instrument basis. The recent advancement allows for some of the signal analysis to be performed locally to the instrument capturing the data [86]. This approach can perform “real time” signal analysis using the techniques developed by the adaptive signal filtering theory [87]. The allocation of more “computational power” to the individual instruments makes the implementation of “virtual instruments” even more flexible and time efficient.

The third major advancement in the mixed-signal ATE was the introduction and continuous improvement of test plan debugging methods [91], [93], [94]. Prior to the introduction of the debugging tools, the task of test plan development was a very tedious and painful process. With today’s graphical user interface and menu driven debugging tools, it is impossible to imagine how the work of a test engineer could be accomplished prior to emergence of these tools.

As implied earlier, advancements of the performance of integrated circuit ADC’s and DAC’s directly enabled the spread of DSP’s into today’s ATE’s. Of particular note the application of sigma-delta modulation [95] to waveform generators and digitizers made testing of high resolution (>18 b) audio devices possible. Also, advances in direct digital synthesis and the performance of phase lock loop circuits brought the ATE higher precision clocking schemes and time measurement instruments. The computing power of the ATE can be used to emulate traditional control loops. Here, the array processor operates at a much higher frequency than the signal frequency within the emulated loop. The DSP engines, coupled with programmable digital channels, provide a wide variety of digital waveforms needed for the testing of complex communication devices. The testing of read channel devices for hard disk drives is made possible by the application of the programmable arbitrary waveform generators (see the specifications shown in Table I).

Demands on the analog testing capabilities of mixed-signal ATE are continuously growing. The trend of ATE vendors has been to incorporate additional functionality into their newer ATE models to meet new testing demands. Recent developments in personal wireless communications has created an abrupt new demand for RF (<3 GHz for now) testing capabilities, which are being added to new generation of mixed signal ATE. Heretofore the RF ATE market has been a niche market dominated by companies like Hewlett-Packard and Roos Instruments. However, the trend of integration of more and more functions into ATE will likely continue for the foreseeable future and the coexistence of all digital, baseband analog and RF instruments on a single ATE platform is in the works. LTX, Teradyne, and Hewlett-Packard are working on such systems.

If one contrasts this discussion of the development of mixed-signal IC testing methods with that of the previous section on digital IC testing methods, the following important observations can be made. First the major advances in digital IC testing have been in development of fault based methods of testing while the significant advances in mixed-signal testing have been in the capabilities of the ATE. The test methods used for mixed-signal IC’s are essentially the same
The digitizing receiver may be a more elaborate design. The can be a comparator with reference supplied via A T1 or A T2. pins to the test system for measurement. A digitizing receiver a voltage from AB1, and switch five drives voltages from the and AB2 buses; switch 4 can drive the pin with a current or node high or low. Switches 4 and 5 connect the pin to the AB1 is shown in Fig. 24. Switch 1 disconnects the circuit core, so boundary modules. The proposed functionality of such module can be in turn connected to the external test pins A T1 and one or both of the on-chip global buses AB1 and AB2, which achieved by connecting any point in the mixed signal circuit to the 1149.1 shorts-and-opens test), for two-probe parametric testing, and it is being considered for many more kinds to the digital case. A sign of change in this scene has been the recent application of BIST methods to test an ADC on a mixed-signal IC [100]. The on-chip tests described in this paper are frequency response (FR), SNR, gain tracking (GT), intermodulation distortion (IMD), harmonic distortion (HD); i.e., classical ADC functional quantities.

Over the last three to four years, the work to standardize the mixed signal testing has gained enough followers that the extension to P1149.1 standard is currently under consideration by an IEEE committee. The preliminary P1149.4 mixed-signal boundary scan standard extends the IEEE 1149.1 digital boundary scan standard (described in Section III), by the addition of the analog and parametric measurement capabilities. 1149.4 is intended to aide in automation of mixed-signal board testing, and to reduce test interconnect. This is an attempt at the application of many benefits delivered by 1149.1 in digital testing directly to mixed signal testing. The P1149.4 may prove useful for simple shorts-and-opens testing (similar to the 1149.1 shorts-and-opens test), for two-probe parametric measurement, and it is being considered for many more kinds of measurements [101], [102].

The interconnections for particular measurements can be achieved by connecting any point in the mixed signal circuit to one or both of the on-chip global buses AB1 and AB2, which can be in turn connected to the external test pins AT1 and AT2. The resources to perform the tests are provided by analog boundary modules. The proposed functionality of such module is shown in Fig. 24. Switch 1 disconnects the circuit core, so the test circuitry can control the pin. Switches 2 and 3 pull the node high or low. Switches 4 and 5 connect the pin to the AB1 and AB2 buses; switch 4 can drive the pin with a current or a voltage from AB1, and switch five drives voltages from the pin to the test system for measurement. A digitizing receiver can be a comparator with reference supplied via AT1 or AT2. The digitizing receiver may be a more elaborate design. The switches shown in this figure represent the functionality and not physical implementation. The implementation of connecting and disconnecting subcircuits to and from the test buses and pads are left to individual designers.

Mixed-signal systems are much harder to characterize and measure than pure digital systems. Systems with extreme high frequencies, small amplitudes, or high precision components may prove difficult to test with P1149.4. Since P1149.4 performs static tests much like 1149.1, some nonstatic or feedback dependent circuits may also be hard to test [102].

There are still many open issues with this proposal. It is believed that implementation of the global bus will be difficult if not impossible for high frequency circuitry. The effects of presence of these busses on the overall performance of the IC’s is also of concern.

V. RF TESTING METHODS

Radio frequency (RF) circuits have been around for many years; but not until the recent explosion in personal wireless communications industry was there a need for investment in high volume RF testing capabilities. When RF IC’s were exclusively for modest volume military, government and niche commercial applications, there was little demand for high volume RF ATE capabilities. The demand for large volume and low price of the RF integrated circuits (RFIC) for consumer communications products has stimulated the ATE industry to respond with the introduction of RF measurement upgrades to already existing lines of mixed signal ATE.

Over a decade of the experience in analog base-band testing is now being extended to RF measurements. The DSP- based FFT spectrum analyzer is the work-horse of today’s ATE’s [96]. Let us review the block diagram of the typical DSP based frequency analyzer shown in Fig. 25.

The input signal is passed through an (variable) attenuator and an anti-aliasing (low pass) filter to respectively provide measurement range and to remove the unwanted high frequency components that are outside of the frequency range of the instrument. Next, the signal is sampled and converted to digital format by ADC. The DSP (often called an array processor in the ATE literature) calculates the spectrum of the waveform using the FFT and passes the results out to the display. In an ATE environment the array storing the spectrum components is normally further processed to obtain the SNR, THD, and/or RF measurements.

To apply this approach to the RF signals, the signals to be analyzed must be converted to frequencies within the range...
Fig. 26. Block diagram of the DSP-based RF spectrum analyzer concept.

\[ V_{R1} = S_{11} \cdot V_{i1} + S_{12} \cdot V_{i2} \]
\[ V_{R2} = S_{21} \cdot V_{i1} + S_{22} \cdot V_{i2} \]

Fig. 27. S-parameter definition.

of operation of the ATE. This is achieved by application of mixing techniques. The block diagram shown in Fig. 25 is modified in Fig. 26 to include the mixer. Fig. 26 shows the block diagram of a DSP based RF spectrum analyzer. This is the basic idea behind the implementation of the modern RF instrumentation. Typical RF measurements like scattering-parameters, noise figure, and intermodulation are built upon this basic model. The local oscillator (LO) signal is selected to bring the signal down to the frequency range of the ATE digitizer.

The fundamental mathematical network description for the terminal or port behavior of an RF network are the scattering or S parameters. Similarly the characterization and testing of RF circuits, has been historically based on the measurement of S parameters. S parameters relate to the incident and reflected power flow that occurs in a network, as observed at its ports [96]. Unlike the impedance, admittance, and hybrid parameters that equivalently relate the voltages and currents existing at a network’s ports, the corresponding S parameters relate the incident and reflected waves observed at the same ports. They describe the bidirectional wave propagation in the network. The definition of S parameter terms and the equations relating all the parameters are given in Fig. 27.

To extend the instrument shown in Fig. 26 to the measurement of S parameters, it is necessary to introduce a bidirectional coupler for measurements of the incident and reflected waveforms in the path between the signal source and the DUT. This approach puts the radio and microwave interface right next to the DUT and mixes the signals down to the frequency band of operation of the digitizers. Fig. 28 shows a typical arrangement for the S_{11} parameter measurement [90]. The RF signal is guided via a controlled impedance environment to the input of the DUT. The power level is adjusted to meet the specifications of the DUT. The incident and reflected waveforms are digitized with the high speed or high resolution digitizer, depending on the bandwidth requirement of the particular measurement. The particular arrangement in Fig. 28 shows a single digitizer architecture which allows measurement of the incident and reflected waveforms through the same signal path. The digitizer is controlled by the digital vector patterns, which allows for fully coherent data capture. The digitized representation of the waveforms is sent to the DSP to be processed. From here on, the DSP that is either central or local to the digitizer is used to transfer this data from time-to-frequency domain. The same DSP is used for analysis of the resulting spectrum and calculation of the reflected and incident signal power levels. These values are used to calculate the S_{11} parameter for the DUT.

VI. NEW PARADIGM FOR MIXED-SIGNAL AND RF TESTING

If one contrasts the discussion in the previous two sections regarding the development of mixed-signal and RF IC testing methods with that of Section III on digital IC testing, the following important observations can be made. First the major advances in digital IC testing have been in the development of fault based methods of testing, while the significant advances in mixed-signal and RF testing have been in the capabilities of the ATE. Digital ATE capabilities have advanced too, but their development has been driven by the extensive R&D in nonfunctional methods of testing. The test methods used for mixed-signal and RF IC’s are essentially the same functional tests performed in the time of bench top testing, except for adaptations needed to translate these measurements to a DSP based measurement environment. A by-product of this translation is that the measurements are more robust and reliable, but much of the same functional parameters are still being measured. Research and development in nonfunctional analog (baseband and RF) testing methods, such as fault based analog testing, has thus far been subcritical and not very productive. We suspect that this is due to the fact that analog IC complexity has not yet rendered functional testing impractical, and that analog fault base testing is seen to be less tractable than it is for the digital case. The advances in the signal handling between the ATE and DUT have also been largely occurred in the ATE. Nonetheless, the advancing complexity and performance of mixed-signal and RF IC’s is stressing functional test methods and the ATE to their limits.

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Given the context provided by the previous sections, we are in a position to consider some potential future directions for mixed-signal and RF IC testing. We believe the time is ripe for sort of fundamental changes that will open new R&D opportunities for the industrial and academic circuits and systems community. Unless a fundamental departure from the current testing paradigm occurs, the future will likely be dominated by packing increasingly more resources into the ATE. We submit that the limit to this approach, which has served the semiconductor industry well since the mid-1970’s, is near at hand. This limit is not one of technology, but economics. Simply put, the ATE are becoming too costly and they are unavoidably one generation behind the advancing mixed-signal IC performance curve. Furthermore, functional tests are becoming increasingly more difficult and time consuming to perform. Thus, simply maintaining the status quo in mixed-signal and RF testing will become less and less acceptable. It is time to consider new testing paradigms. We believe that the most fertile paradigms will come from efforts where academe and the industrial IC test community work in partnership. It was this view that brought the authors of this paper together. Our purpose in this section is to stir the pot by identifying the critical limits of the current mixed-signal IC testing paradigm and to relate some potential alternative approaches for the reader’s consideration.

The BIST work of Roberts et al. [100] represents the kind of fresh approaches that are needed. “Analog fault modeling” and other unconventional testing methods need to be investigated in a pragmatic way as well. There are some reports on the application of inductive fault analysis (IFA) to the modeling the faults in analog IC’s. Proponents of this technique argue that IFA based testing combines the circuit topology and process defect data to arrive at the realistic fault models that are specific to the circuit. This information can be exploited by test engineers to generate effective and economic tests [69]. Some other work has concentrated on adapting digital circuit test techniques to the testing of analog IC’s. These attempts have lead to methods for analog test generation and fault simulation that are mapped into the digital domain. The analog circuit is mapped to a digital representation using a standard continuous to discrete transformation. This technique is proposed as a more cost effective simulation-based means of analog test generation [97]. This type of R&D activity has to grow to critical mass if the escalating costs of mixed-signal and RF IC testing are to be countered. The insidious types of fault that are particularly problematic in analog IC’s are the performance failures that are caused by one or more random mismatches in ratioed components (e.g., capacitors, transistor gm’s, etc.), even when all the process parameters are within acceptable range. Such a fault occurs when a random physical mismatch combines with a sufficient degree of circuit sensitivity to realize a performance failure. The circuit sensitivity that relates the failed performance parameter to the mismatch, is inherent to the circuit schematic and/or the physical layout. Only when a circuit is sufficiently insensitive to a particular mismatch, such that it can only produce a performance failure when the process parameters are out of acceptable range, does the mismatch not represent a potential fault. As in digital circuits, fault detection in analog circuits depends on observability and controllability of the DUT. BIST approaches can enhance both of these qualities.

When trying to improve a process, it is often helpful to identify the weakest parts or links in the process. Is often in addressing the weakest link where the most impact can be realized for a given amount of effort. We believe the weakest links in the current ATE based test process for mixed-signal and RF IC’s to be the SIGNAL HANDLING function of the ATE and the interface between the DUT and ATE. For analog baseband and RF tests, the signal handling and ATE/DUT interface must be robust, well modeled, and well controlled. As described in section II, the physical separation between the ATE and DUT is quite large in physical and electrical dimensions. Also, the device interface board or DIB (with either a probe card or socket adapter) serves as the primary interface between the ATE and DUT. All the electronics used to facilitate this interface are mounted in a limited area (see Fig. 7) on to the DIB. These electronics are usually a collage of small scale integrated IC’s and discrete components. The wiring may involve custom interconnect fabricated on to one or more of the un-dedicated DIB planes or it may involve (all or in part) discrete wiring. In comparison to the DUT and ATE, this critical interface is surprisingly low-tech and ad hoc. An example of a loaded DIB is shown in Fig. 29. The problems with this setup require little explanation: the design and implementation of DIB electronics are ad hoc, the resulting circuitry is not well posed for accurate simulation, and the functionality is limited by the constrained space on the DIB and a discrete circuit implementation.

Testing is part of the overhead associated with IC manufacturing; and, as such, testing is ultimately an economically driven process. The objective is to achieve the requisite quality control derived from testing at the lowest cost. With testing approaching, for some mixed-signal IC’s, up to 50% of the manufacturing cost; reducing test costs is of keen interest.

Fig. 29. Loaded DIB (photo).
to IC manufacturers. However, reductions in test costs that lessen quality control will have a detrimental impact that more than compensates for the savings. The cost of testing can be broken down into three components; namely, the cost of test development, the cost of using the ATE on a per part basis, and the cost of design for testability. The cost of test development covers the cost of designing the tests to be conducted, writing software to program the ATE, the design and construct of the DIB interface electronics. The cost of ATE usage is largely the allocation of the cost of owning, operating and maintaining the ATE equipment to each part tested or to each part delivered to customers (in dollars per unit time). The cost of the design for testability is the real-estate used on the chip for either testability features or BIST; and the cost of developing the associated on-chip electronics and integrating them into the DUT. To achieve a systemic reduction in the cost of testing necessitates a coordinated effort to address these cost components in a systematic way.

To understand the cost issues, let us briefly examine what has driven these cost components in recent years. To match the increasing complexity of mixed signal and RF parts, and the demand for more sophisticated tests, the complexity and cost of ATE have been escalating since the 1980’s. That is as the performance, frequency, and features of mixed-signal IC’s have advanced, the ATE industry has responded with new models and plug-in features. Furthermore, as we alluded earlier, the ATE are perpetually obsolete in that they must follow, rather than lead, the IC performance advancement curve. It is difficult to compare the current ATE with early systems from the early 1980’s, due to the improved performance of instrumentation and increased complexity of the latest models. A comparison of the configuration from ten years ago to an identical model sold today indicates that there has been about a 50% decrease in the price per ATE function. Most of this decrease is due to increases in the levels of integration and decreases in the cost of the subassemblies. On the other hand, the new ATE models are packed with increasingly more capabilities that are needed to test IC’s of escalating complexity and performance. Thus the price of ATE systems has been continuously escalating; and, due to the inherent obsolescence, there appears to be no end in sight. Any new testing methodologies associated with fault based testing or any other form of nonfunctional testing will likely, in the current IC testing paradigm, necessitate corresponding changes in the ATE and further increased ATE costs.

Another consequence of the increased complexity of ATE systems, is that the qualifications and salaries for test engineers have escalated to rival those for the circuit design engineers. Their work involves the design of the tests (usually in collaboration with the circuit designers), development of ATE test programs, and design and construct of DIB electronics to interface the DUT to the ATE. We submit that the current IC testing paradigm does not take full advantage of the talents of contemporary test engineers. The compensation and utilization of test engineers is an important component in the cost and quality of IC testing.

Design for testability has become an increasingly important part of the design of all integrated circuits. With design-
IC's include substantial digital circuitry that is often made important to also review digital IC testing. First, mixed-signal manufacturing industry. Although our prime focus has been importance of this area which is so vital to the semiconductor to relate to the circuits and systems community the growing historic, current status and future. Our objective has been assurance in manufacturing from several view points; i.e. available today as the DUT.

A TE could be through the TID, which would be in very close proximity to the DUT. This is illustrated in Fig. 30. Besides the impact on the quality of the DIB interface electronics, the TID could relieve the DUT designer of the need to be concerned about incorporating into the DUT features that make it work within the ATE environment that are not needed in the application environment, e.g., buffers to drive the ATE loads. The implementation of the DIB interface electronics as an integrated TID, could open up a tremendous number of possibilities that were not possible in a piece-part design. Perhaps, most important it could greatly reduce the design cycle and risk that was tolerated with the piece-part design, even if the TID were to have comparatively greater functionality and complexity. A VLSI approach to the ATE-DUT interface, such as the TID, could allow this interface to realize equivalent benefits from the rich VLSI CAD environments available today as the DUT.

VII. CONCLUSION

In this paper we have discussed IC testing for quality assurance in manufacturing from several view points; i.e. historic, current status and future. Our objective has been to relate to the circuits and systems community the growing importance of this area which is so vital to the semiconductor manufacturing industry. Although our prime focus has been on the testing of mixed-signal and RF IC testing, we felt it important to also review digital IC testing. First, mixed-signal IC’s include substantial digital circuitry that is often made independently testable (i.e. a design for testability strategy). Second, the R&D effort for digital and analog IC (baseband and RF) testing have followed different paths that were driven by both economic considerations and the different ways digital and analog IC’s advanced over the past 25 years.

We showed in Section II that the emergence of dedicated automatic test equipment (ATE) in the 1970’s forever changed the testing of digital and analog IC’s. ATE systems were shown to have advanced remarkably in both testing functionality and ease of use. However, due to fast advancing complexity of digital IC’s, the testing R&D and the development of ATE for digital IC’s responded to the realization that functional testing was quickly becoming impractical. Thus, as we showed in Section III, a rich lore of theoretical and experimental literature, circuit architectures with testability features, and CAD tools emerged to support a wide range of nonfunctional testing strategies. In contrast, we showed in Section IV that the major advancements in analog and mixed-signal IC’s were in performance, e.g., resolution and dynamic range. Consequently, the testing methods remained functionally based and the development of ATE for analog and mixed signal IC’s responded to the challenges of testing to increasingly higher standards of performance. RF IC’s, which were largely developed for military and government systems, were shown in Section V to be the last frontier for ATE developments. We also recounted that RF analog IC’s testing has and continues to be based on functional tests.

In response to the need to test IC’s with increasingly higher levels of mixed-signal integration, and the emergence of high volume commercial applications of RF IC’s, we showed in Sections II, IV, and V that the current trend for ATE is to merge the functions needed to test digital, mixed-signal, and RF IC’s into a single ATE platform. In order to keep pace with the need for new test features, the ATE are fast escalating in both complexity and cost. At the same time the complexity and frequency range of mixed signal IC’s (including RF) are causing functional testing and testing at full speed to reach practical limits. In Sections II and VI we also showed that the signal handling interface between the ATE and DUT via the DIB to be the weakest link in the current testing paradigm. Consequently, the priorities associated with design for testability and the role of the test engineer in IC manufacturing have advanced significantly. Commensurate with their escalating responsibilities, the test engineer’s qualifications, capabilities, and salaries have all advanced. Based on these developments and looming deficiencies, we made the case in Section VI that time was prime for the development of new test paradigms. In Section VI we introduced the concept of the Test Interface Device or TID. The TID is a low volume, application specific IC that can be designed to house needed testing resources not currently included on the ATE and to facilitate the signal handling between the DUT and ATE.

REFERENCES


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