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# Digital Integrated Circuit Design I

## ECE 425/525

### Mechanics

*Professor R. Daasch*

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**<http://ece.pdx.edu/~ecex25>**

# Course Mechanics

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Instructor: W. Robert Daasch, [daasch@ece.pdx.edu](mailto:daasch@ece.pdx.edu), FAB 160-14

Office Hours: MW 12:30PM-2:30PM or by appointment

URL: <http://ece.pdx.edu/~ecex25/>, PDF notes available from there see bullet marked "Chapters".

Text: *CMOS VLSI Design, 4th Edition*, Weste and Harris

Others: *Introduction to VLSI Circuits and Systems*, J.P. Uyemura

*CMOS Digital Integrated Circuits (Analysis and Design)*, 2nd Edition, Kang and Leblebici

*Digital Integrated Circuits, A Design Perspective*, J.M. Rabaey

*VLSI Design Techniques for Analog and Digital Circuits*, Gieger, Allen and Strader

*The Modern VLSI Design*, W. Wolf

*The Design and Analysis of VLSI Circuits*, L. Glasser and D. Dobberpuhl

# Robert Daasch, A Quick Bio

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- Professor Electrical and Computer Engineering
- Founder and Director of Integrated Circuits Design and Test Laboratory
- PSU ECE faculty since 1986
- Prior academic appointment Illinois Institute of Technology
- Courses taught: Computer networks design and modeling, parallel computing, scientific computation, digital circuits, linear circuits, semiconductor devices and integrated circuit design and test
- Research: Design and test of digital and analog integrated CMOS circuits

# Course Summary

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- Chapters 1-3 (Light on Chap. 3, Fabrication);  
introduction to the NFET and PFET, modeling, fabrication as well as the passive linear and nonlinear circuit elements in a modern CMOS technology.
- Chapters 4-7;  
The next three chapters address key figures-of-merit for VLSI chips. Chapter 4 is a chapter on logical effort for delay modeling. Chapter 5 outlines key issues of power dissipation. Chapter 6 is a bit misplaced to my mind about the dominant role of interconnect (wire) in integrated circuit design. Chapter 7 introduces the conversion from the ideal design world to the manufacturing of physical (real) chips. Chapter 6 will be touched on briefly in lecture and will be discussed again in the second term 426/526.
- Chapter 8;  
is about simulation. Much of this chapter will be addressed through your laboratory work and not much lecture time will be devoted to this chapter.

# Course Summary

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- Chapters 9-10;  
These chapters form the core of using CMOS to design and build digital combinational and sequential logic circuits.

# Course CAD

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- Cadence; schematics, simulation, layout, extraction, design rule checking
- The lecture will focus on behavior of n(p) channel MOS enhancement devices with depletion and zero threshold devices used in some circuits.
- Design rules are scalable by a factor lambda ( $\Rightarrow \lambda$ )
- Devices models are based on CMOS n-well technology
- The day-to-day responsibility of the TA is supporting the laboratories. This includes help with the software, answering general questions about the laboratories and related lecture content. The TA evaluates and assigns grades for all laboratories.

# Course Grading

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- Grade based on 400 total points
  - Midterm is worth 100 pts
  - Final is worth 200 pts
    - No make-up exams without prior written (email) approval at least one week before exam.
    - Exams are in-class, closed book and notes, calculators are allowed
    - Final exam is scheduled by the university.
  - Four labs normalized at the end of the quarter to 100 pts
  - The average grade for the course will be a *B* or *B<sup>-</sup>*
  - Any student with a 95% or higher will receive an *A* for the course
  - A total score of less than 50% will be assigned a grade no higher than *C<sup>-</sup>*.

# Course Grading

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- As determined by the instructor a failing percentage may be set and graded with an *F*.