Syllabus
ECE 575/675
Fall 2006
26 September 2006

Instructor: W. Robert Daasch, daasch@ece.pdx.edu, 725-5409, FAB 160-14
Textbook: Essentials of Logic Testing, Bushnell
Meeting: NH 454 Tu/Th 4:00pm-5:40pm
Office Hours: MW 2PM-4PM and by appointment

Topical Outline
Testing modern digital IC electronics follows a path founded on well-known engineering principles. It has not been a path entirely of its own choosing because of the traditional separation design and test. Because of the of the increasing complexity of design, not the least of which is the mixture of analog and digital sub-systems on the same IC, new areas in IC test should be expected. The course will follow a traditional path with the addition of the role IC design plays in evolution of IC testing.

The topical outline for the course is divided into three parts. The first part reviews topics in integrated circuit technologies and fault modeling. The second part introduces types of digital IC test; parametric, scan, and functional testing. As time permits, the third part is reserved for topics such as memory test, defect screening, SOC testing etc.

Grading
The grade for course will be based on

100/300 Completion of three homework assignments at three week intervals from the textbook and supplementary problems.

100/300 Take-home Midterm Exam

100/300 Final Exam

Coverage
Chapters 1-4, 5(light), 6-8, 12-13, 15