Logic Simulation using Verilog XL:

This tutorial includes one way of simulating digital circuits using Verilog XL. Here we have taken an example of two cascaded inverters. The name of this schematic is inverter.

Important Point:

The names of the schematic and the pins in the schematic should not start with a number and should not be keywords in verilog (e.g. and, nand). The length of the names should not be more than 15 characters. You should not use '+' and '-'signs for the names of the pins and the schematics.

1. Open the Schematic cell view:

From the Library manager read the inverter schematic cell view. Save the schematic. The inverter schematic is shown in Fig 1.

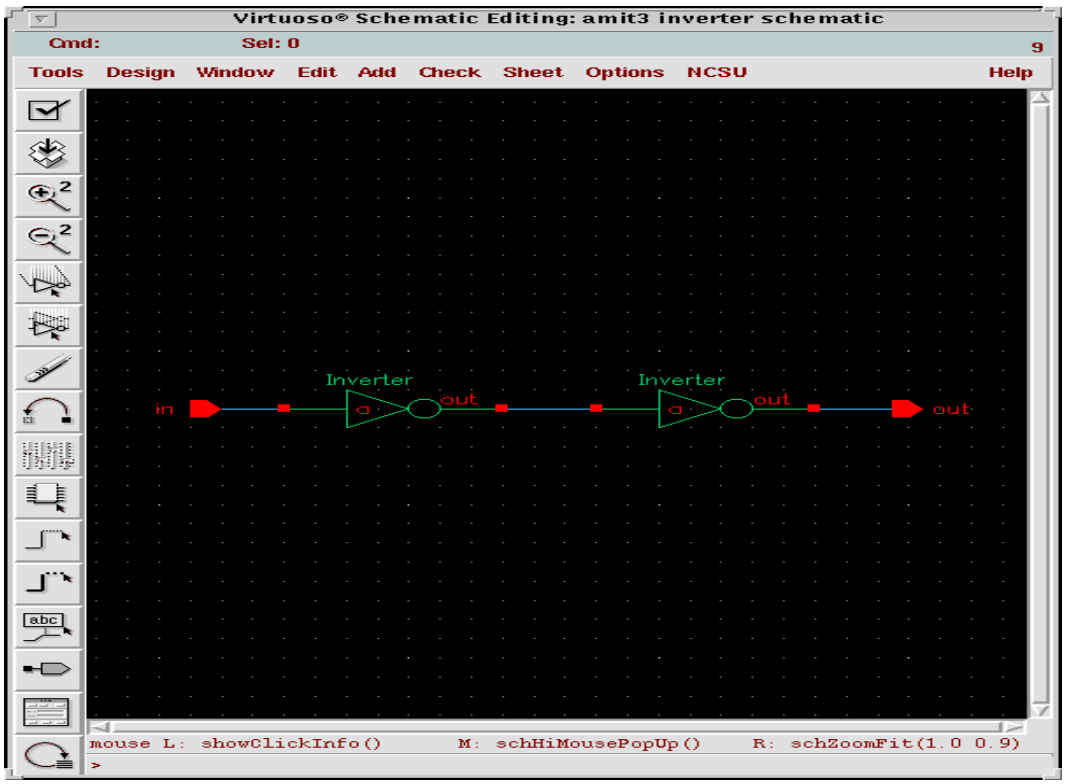

Fig 1: Inverter

2. Initializing Verilog Integration:

a. In Fig 1 select ***Tools –> Simulation –> Verilog - XL***. The "Setup Environment" window opens as shown in Fig 2.

b. In Fig 2, enter inverter.run1 in the **Run Directory** text box. All other default values are correct. Click ***OK***.

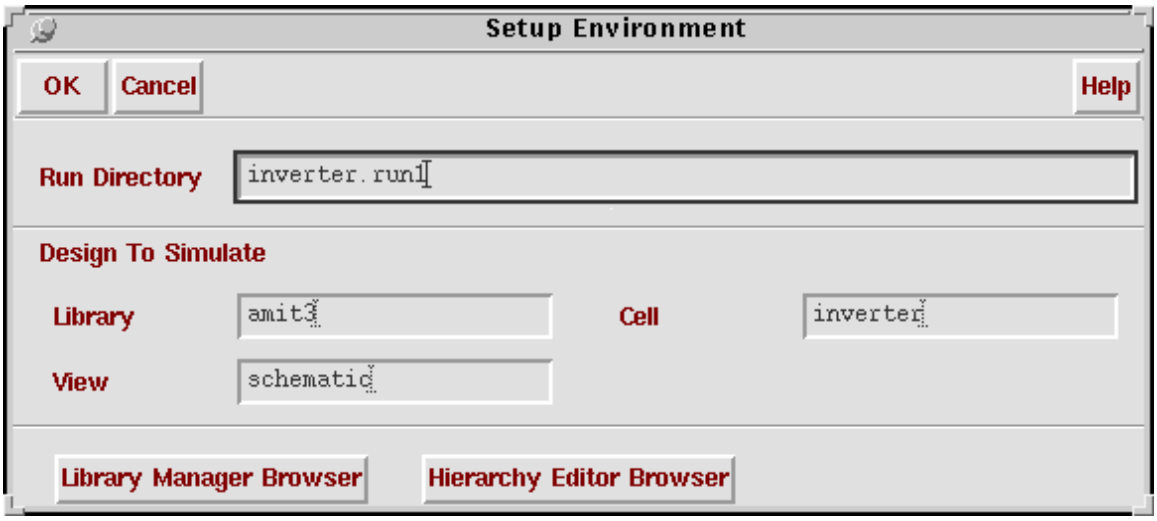

Fig 2: Setup Environment

c. The “Virtuoso Schematic Composer Analysis Environment for Verilog-XL Integration” window opens as shown in Fig 3 and the inverter.run1 directory is created.

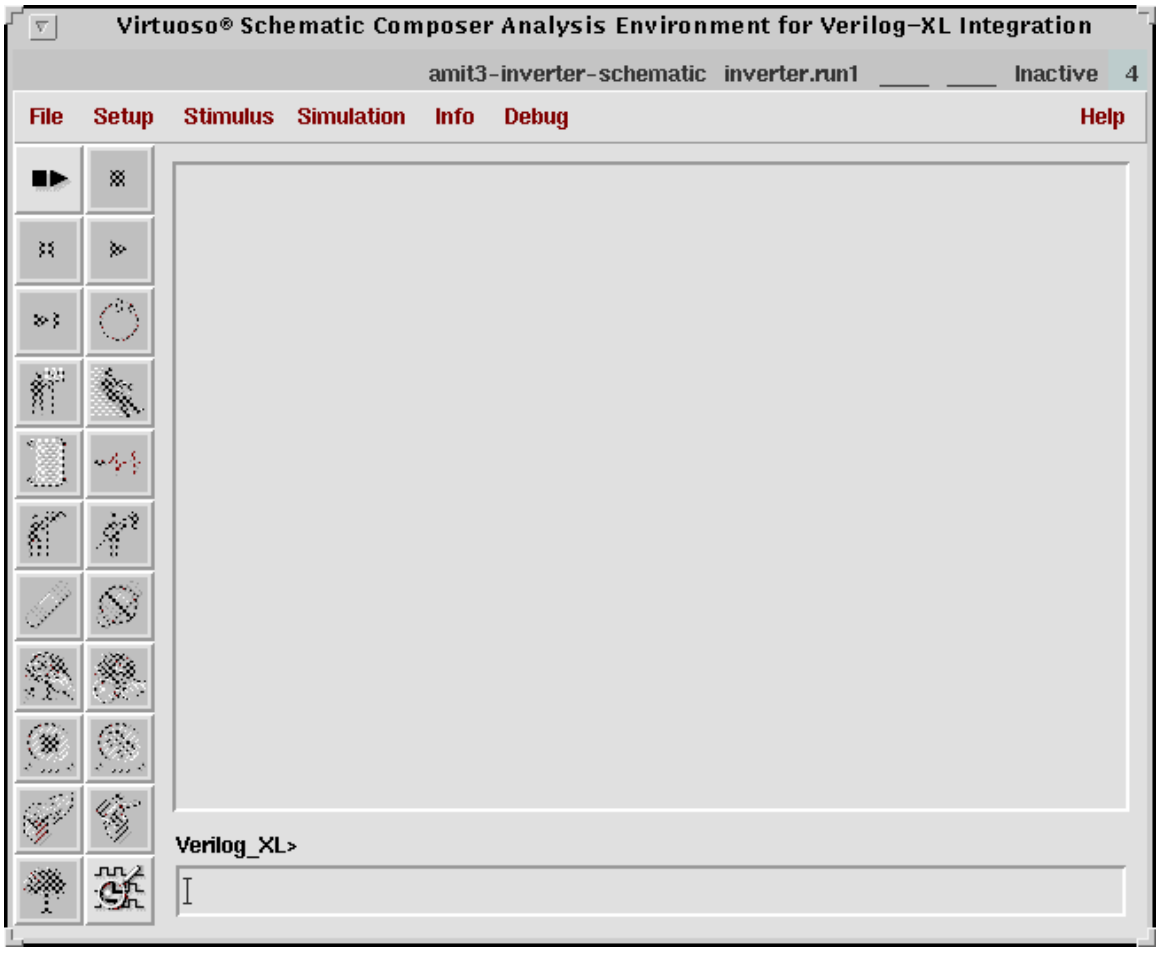

Fig 3: Environment for Verilog-XL Integration

3. Setting the Netlist Options:

a. In Fig 3 set the netlisting options by selecting ***Setup –> Netlist***. The "Verilog Netlisting Options" form opens as shown in Fig 4.
b. The default settings are as shown in Fig 4. They are all correct.

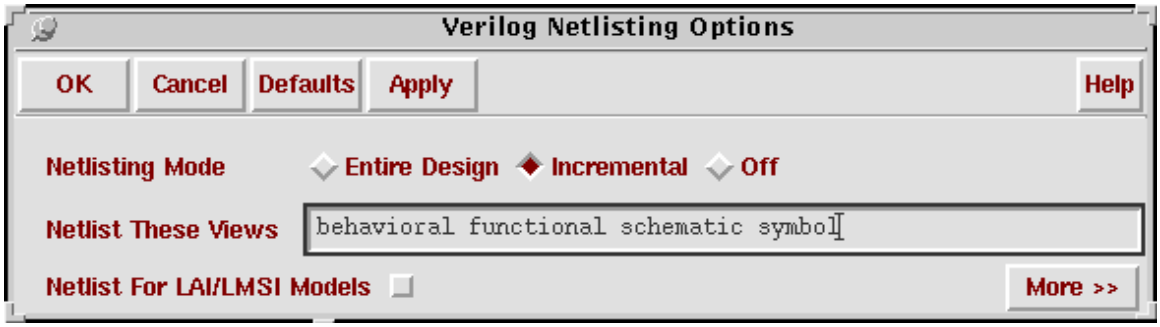

Fig 4: Verilog Netlisting Options

c. In Fig 4 click ***More>>***
Additional netlisting options are added to the form as shown in Fig 5.

d. In Fig 5 set **Global Power Nets** to *vdd* and set **Global Ground Nets** to *gnd.* (The names for the **Global Power Nets** and **Global Ground Nets** should be set as per the names of the power and ground pins in your schematic).
e. Select **Generate Pin Map**.
f. Select **Declare Global Locally**.
g. The **Drop Port Range** and **Preserve Buses** options are selected by default. It doesn't matter if we select or deselect them.
h. Click ***OK***. Thus setting the Verilog Netlisting Options is done.

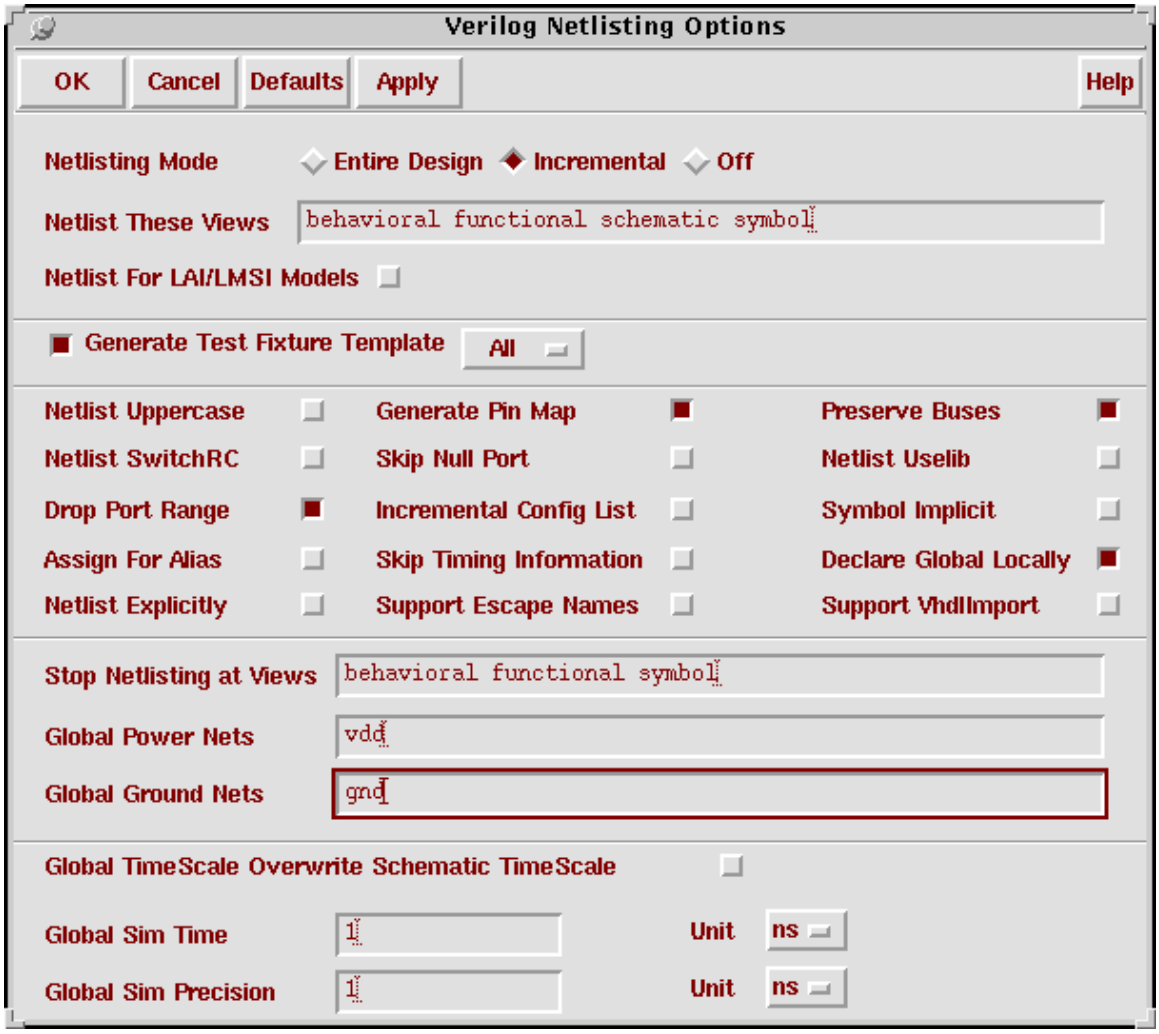

Fig 5: Additional Verilog Netlisting Options

4. Creating the Stimulus File:

a. In the "Virtuoso Schematic Composer Analysis Environment for Verilog-XL Integration" window select ***Stimulus –> Verilog.***
b. A dialog box appears as shown in Fig 6. Click ***No*** in the dialog box.

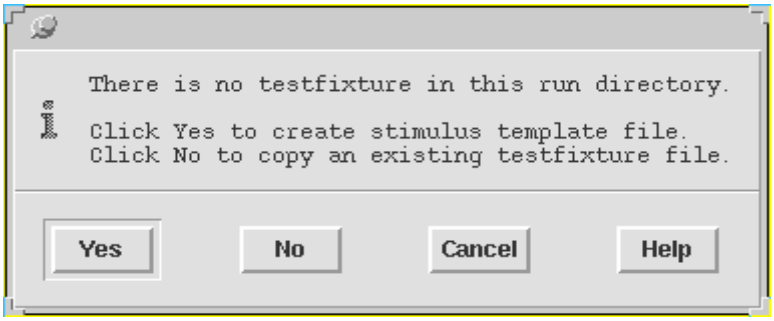

Fig 6: Dialog Box

c. A “Stimulus Options” form opens as shown in Fig 7. The default **Mode** is **Copy**.

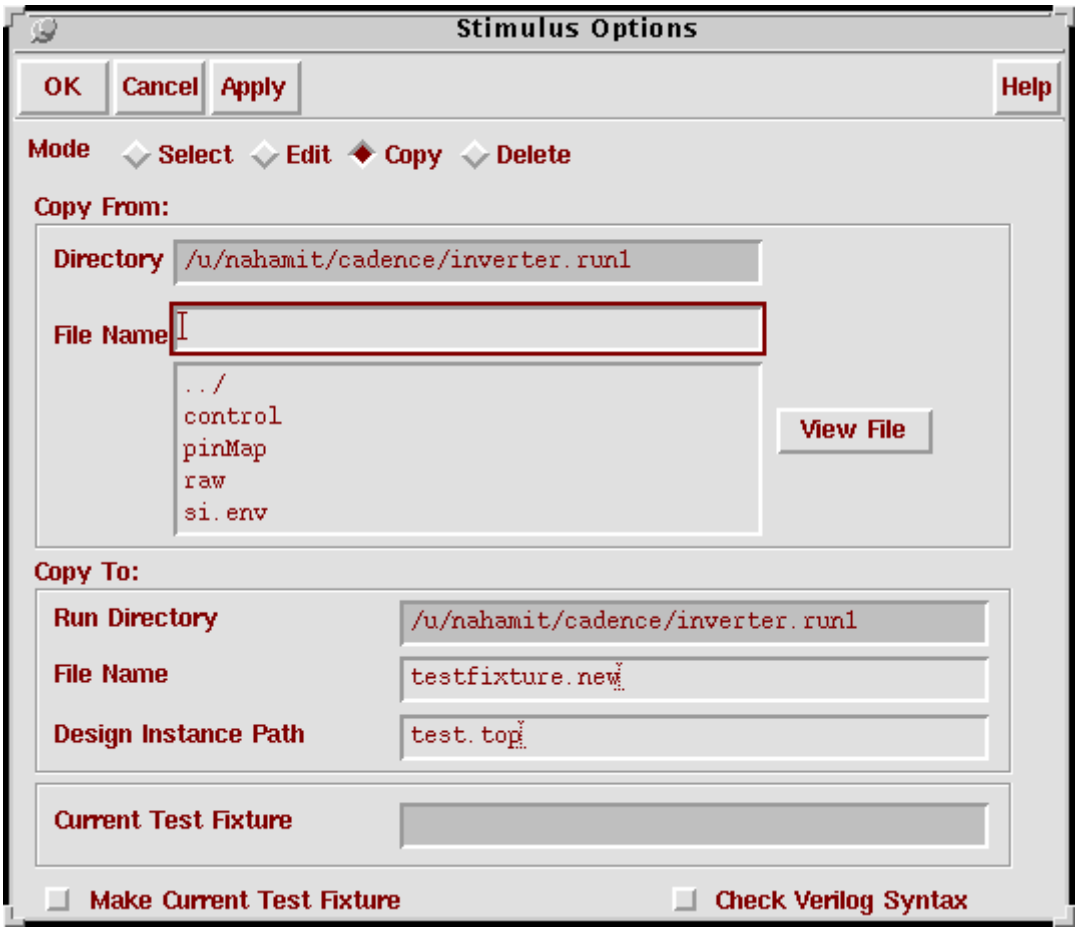

Fig 7: Simulation Options

d. In Fig 7 select the verilog file generated using BitGen in the **File Name** text box. The verilog file selected can be seen in Fig 8.

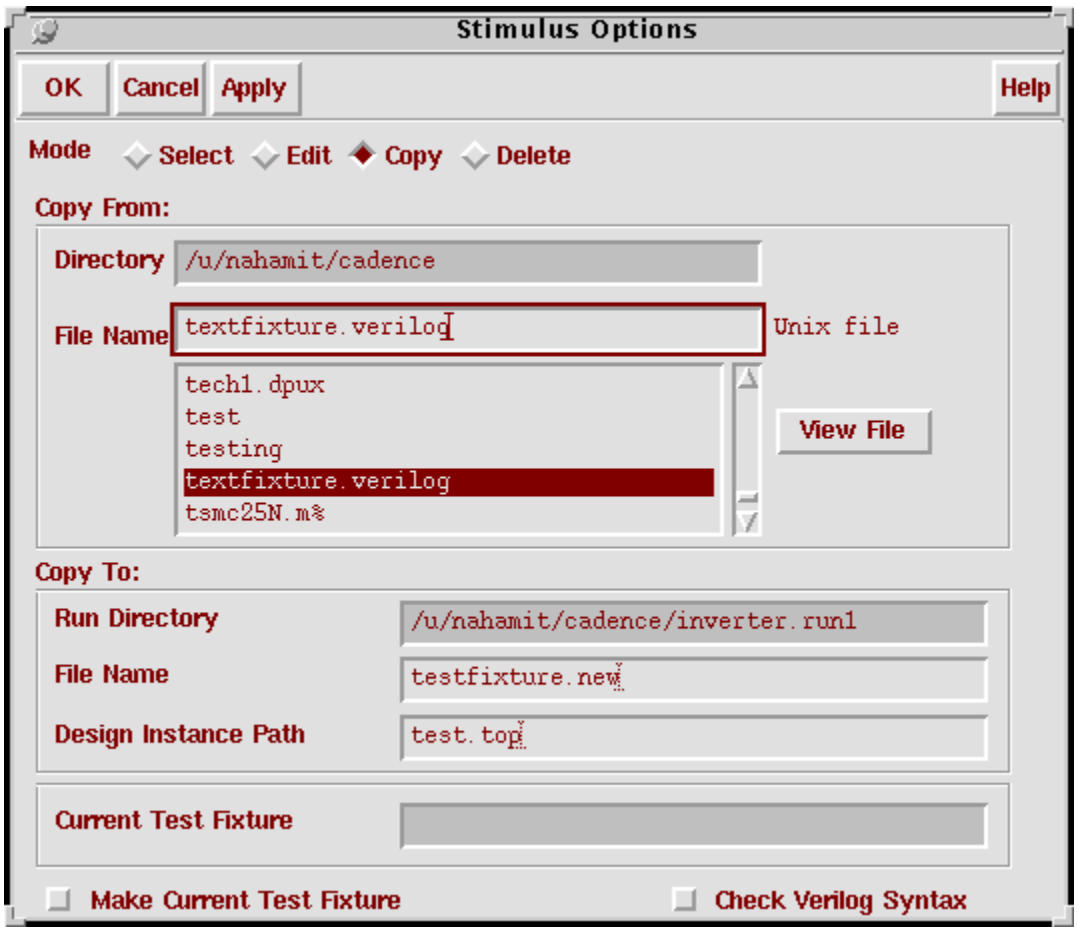

Fig 8: Simulation Options (Verilog File selected)

e. You can view the stimulus file by clicking **View File** in Fig 8.
f. Click **OK** in Fig 8.
g. Another "Stimulus Options" form opens as shown in Fig 9.

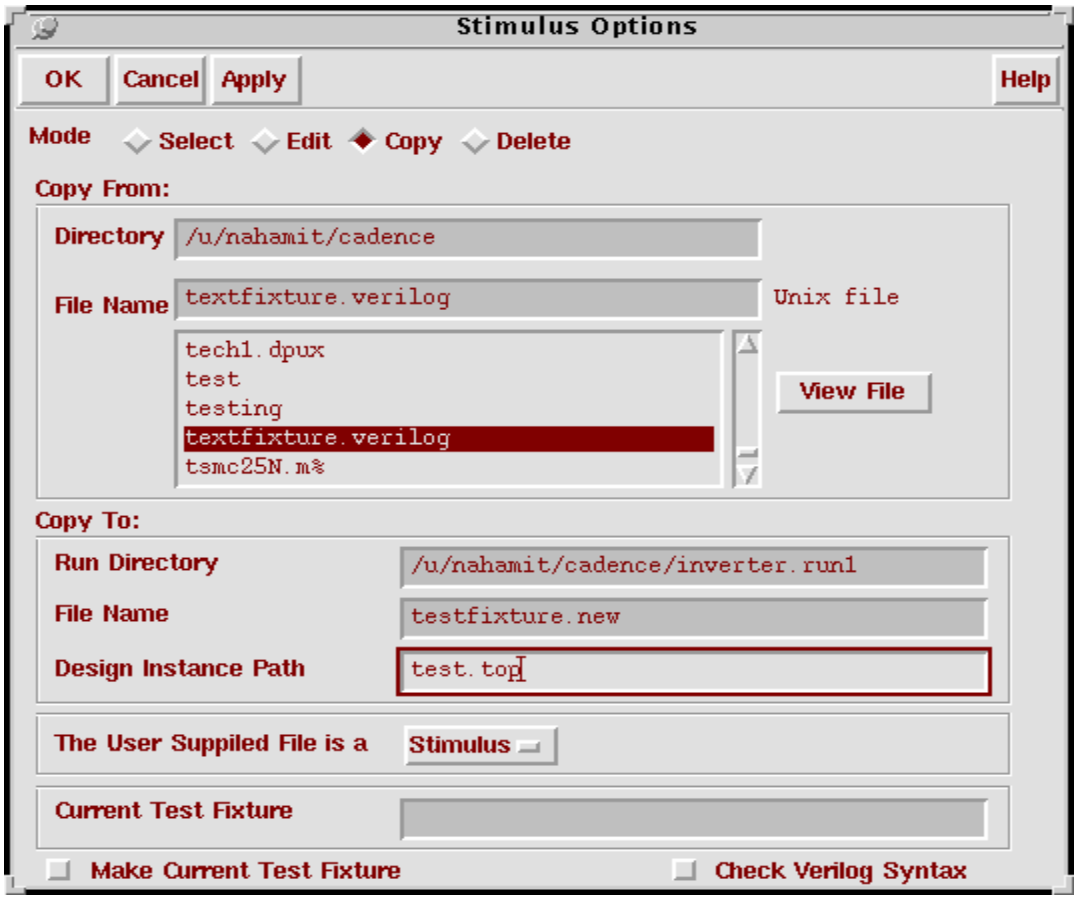

Fig 9: Simulation Options

h. Click **OK** in Fig 9.
i. In the "Virtuoso Schematic Composer Analysis Environment for Verilog-XL Integration" window again select ***Stimulus –> Verilog*.**
j. The "Simulation Options" window opens as shown in Fig 10.

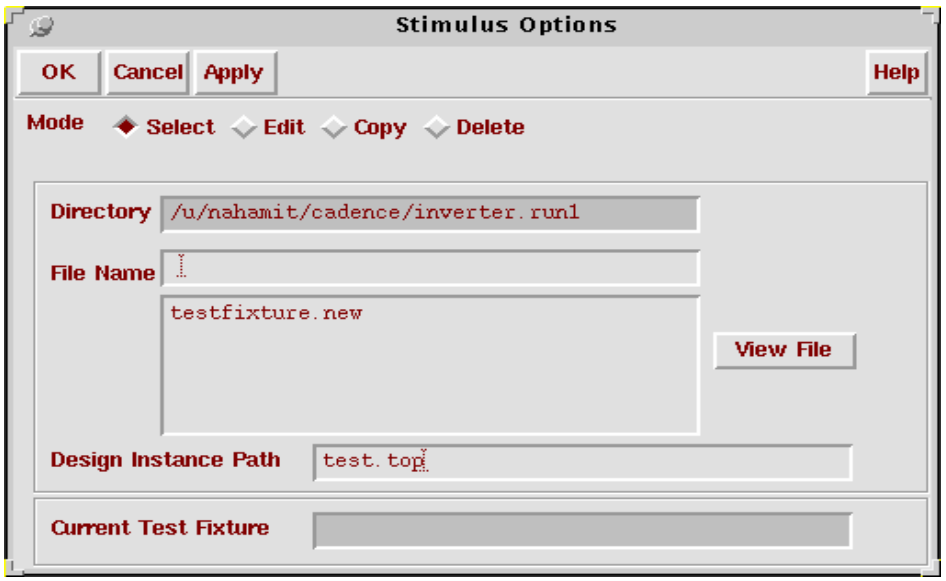

Fig 10: Simulation Options

k. In Fig 10 select textfixture.new and click **OK**.
l. Thus creating the netlist and the stimulus file is done.

5. Starting the Simulation:

a. In the "Virtuoso Schematic Composer Analysis Environment for Verilog-XL Integration" window click ***Setup –> Record Signals ….*** The "Record Signals Options" form opens up as shown in Fig 11.

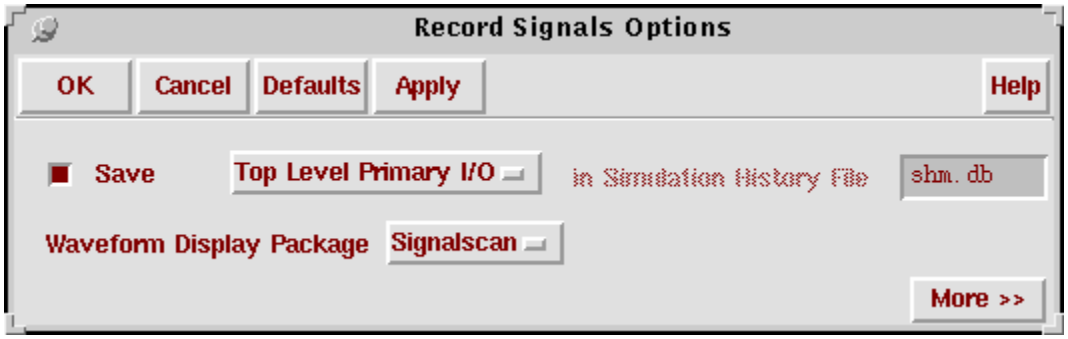

Fig 11: Record Signals Options

b. In Fig 11 change the **Top Level Primary I/O** tab to **All Signals** as shown in Fig 12.

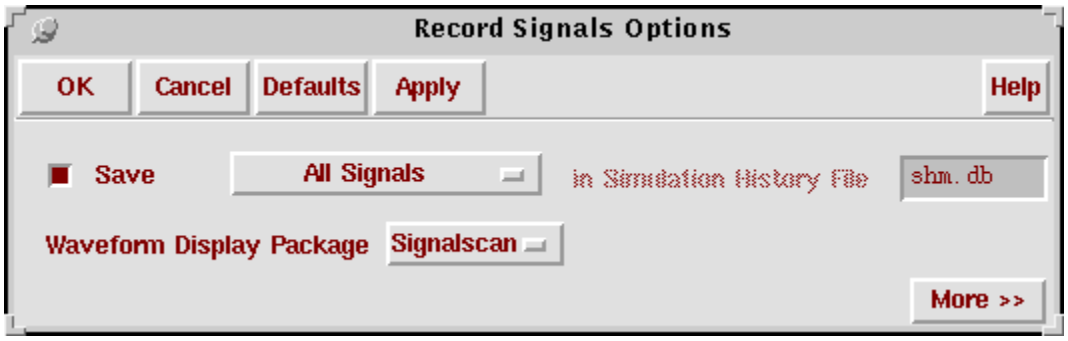

Fig 12: Record Signals Options

c. In Fig 12 click **OK**.
d. In the "Virtuoso Schematic Composer Analysis Environment for Verilog-XL Integration" window click ***Simulation –> Start Interactive.*** At this stage the stimulus and the netlists are compiled. If there are any errors in the netlist or the stimulus file then the errors show up. If everything is correct, then the stimulus file and the netlists are compiled and the window shows up as shown in Fig 13.

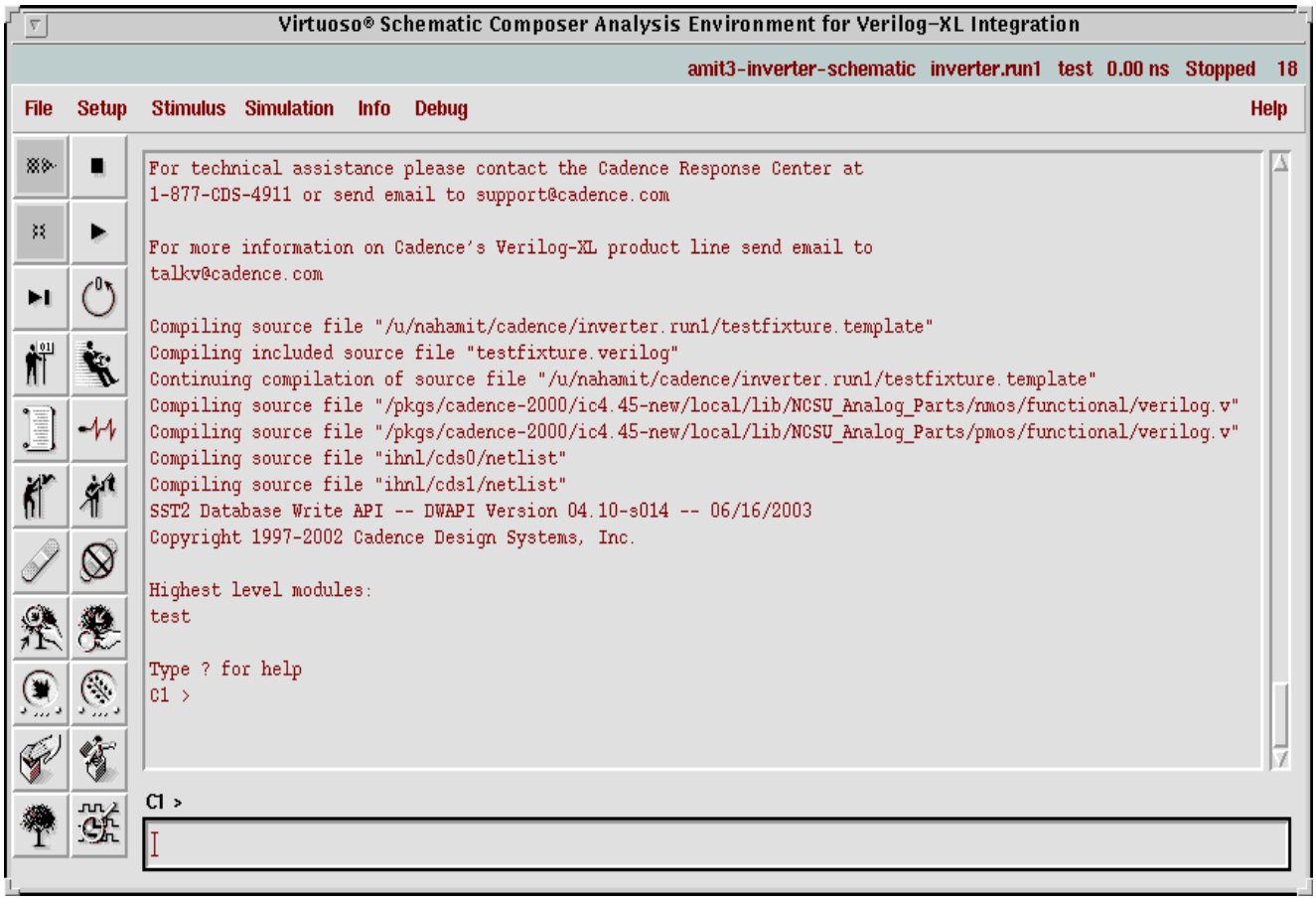

Fig 13: Compiling the netlists and the stimulus file

e. In Fig 13 click ***Simulation –> Continue.***
f. Fig 13 now shows up as shown in Fig 14. Thus the simulation is complete.

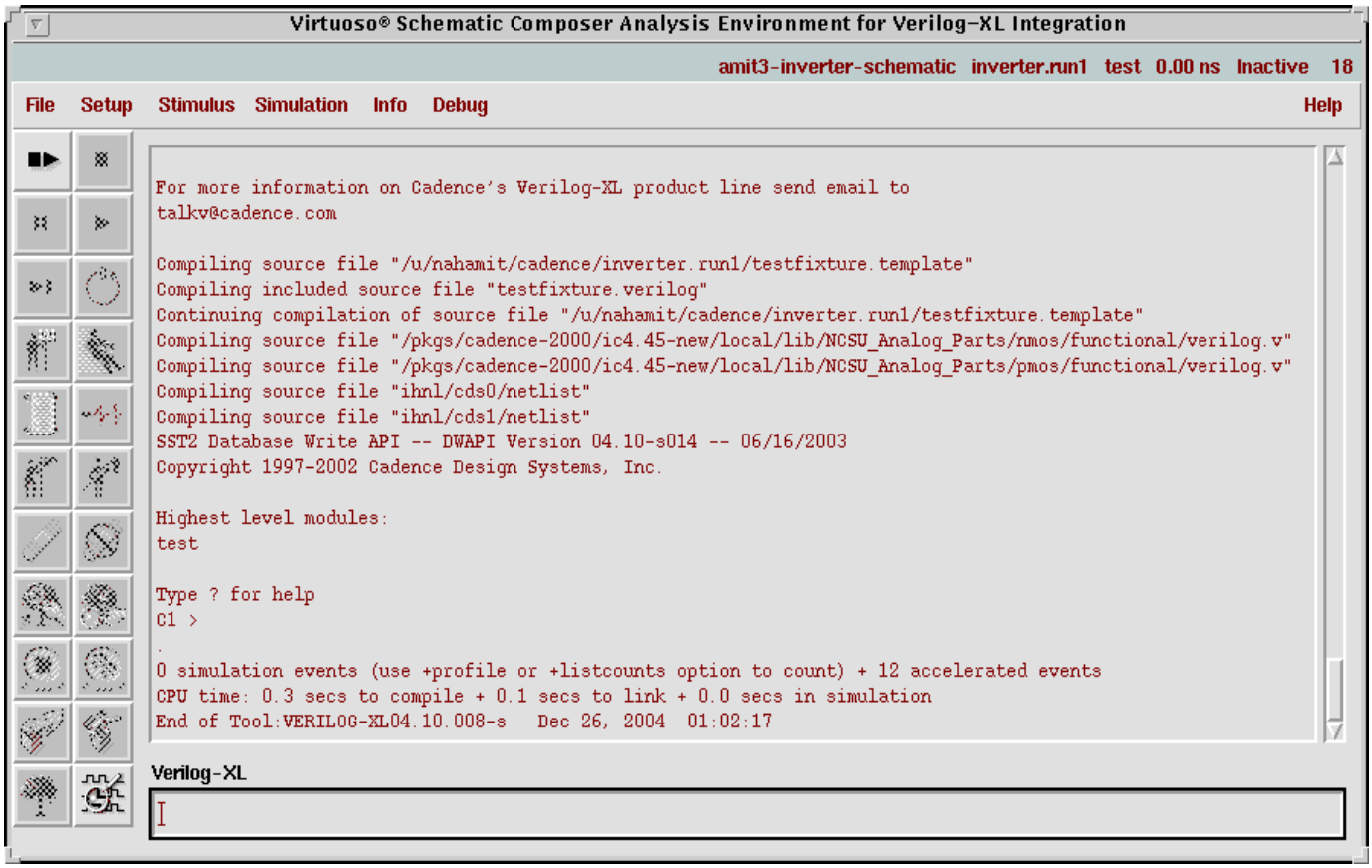

Fig 14: Simulation is complete

6. Viewing the Waveforms:

a. In Fig 14 click on the **View Waveforms** button. (This is the button which is enabled in Fig 14 in lower left corner).
b. On clicking **View Waveforms** a Logic Verification tool **SimVision** opens as shown in Fig 15.

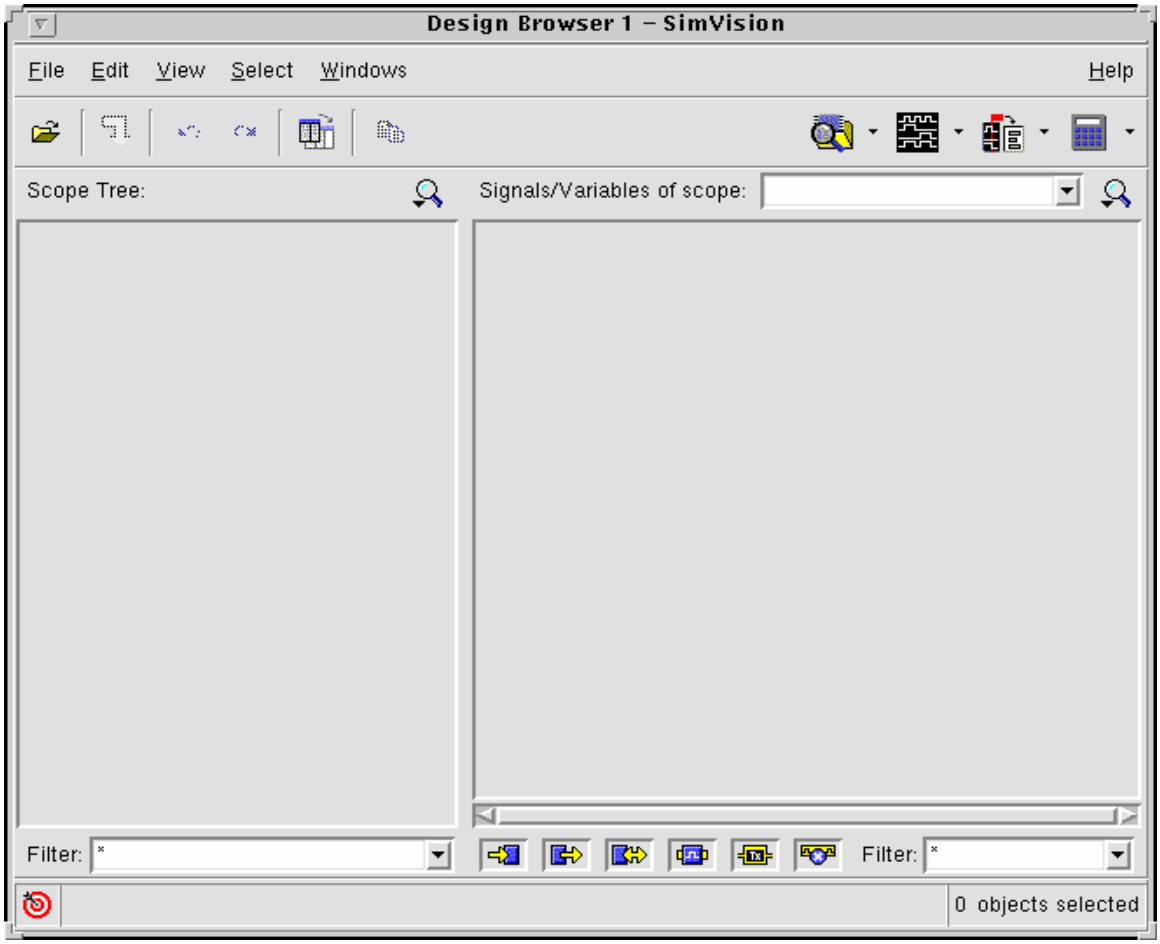

Fig 15: SimVision

c. In Fig 15 click ***File –> Open Database.*** The "Open Database" window opens as shown in Fig 16.

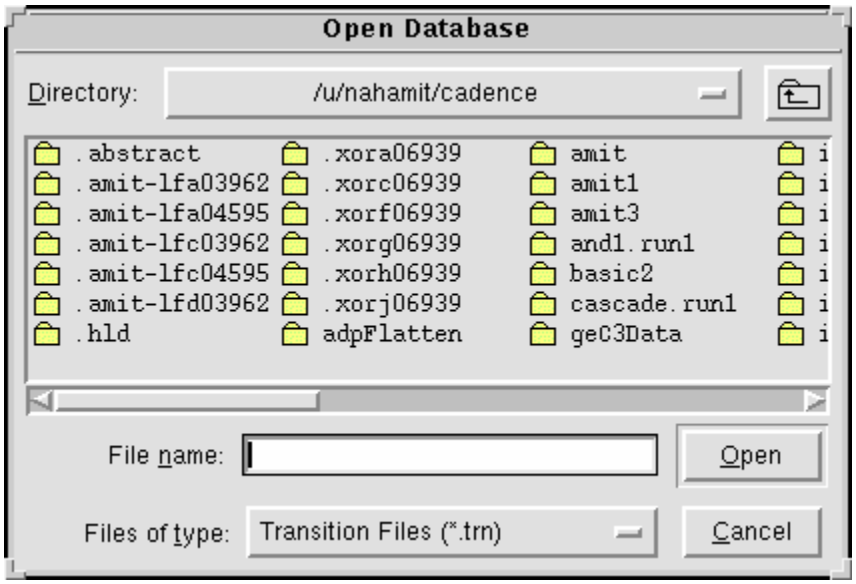

Fig 16: Open Database

d. In Fig 16 browse to *../inverter.run1/RunObject.0/shmDir/shm.db/* and select the file *shm.trn* as shown in Fig 17.

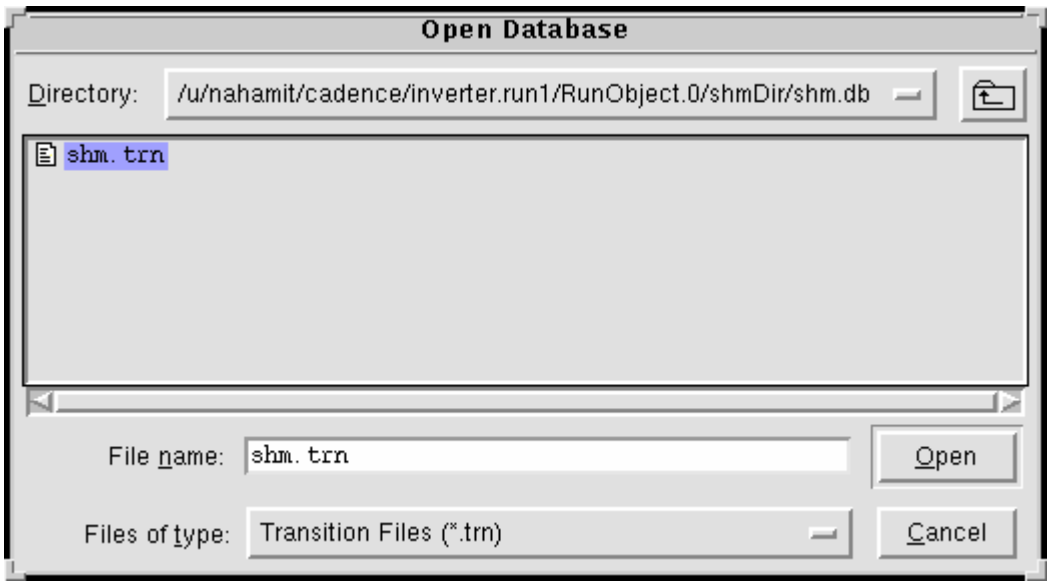

Fig 17: Selecting the file

e. In Fig 17 click **Open**.
f. Now the "SimVision" window appears as shown in Fig 18.

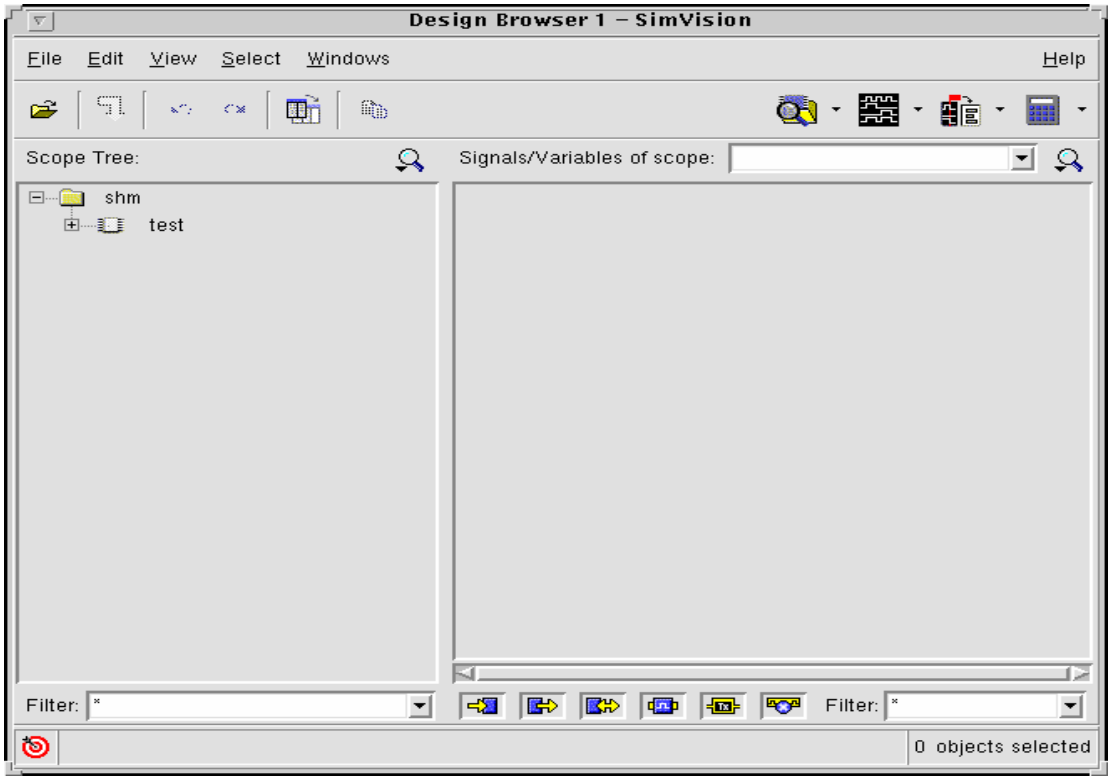

Fig 18: SimVision after opening database

g. In Fig 18 the circuit hierarchy can be seen as shown in Fig 19.

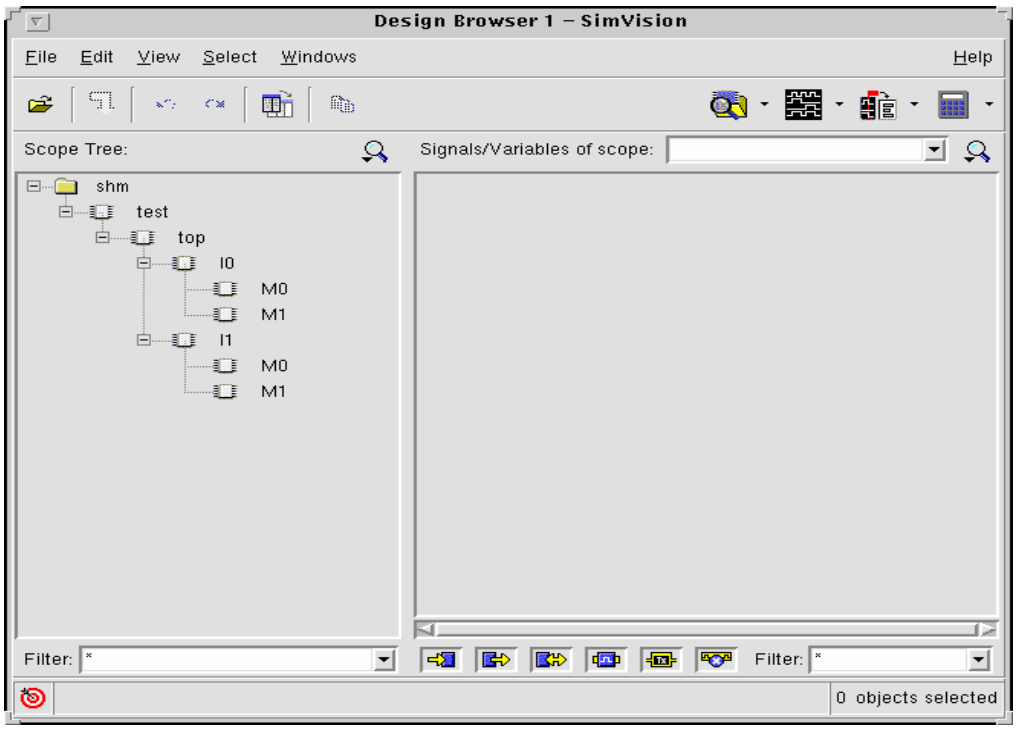

Fig 19: Hierarchy of the circuit

h. In Fig 19 click on test and the signals on the top level of the circuit appear as shown in Fig 20.

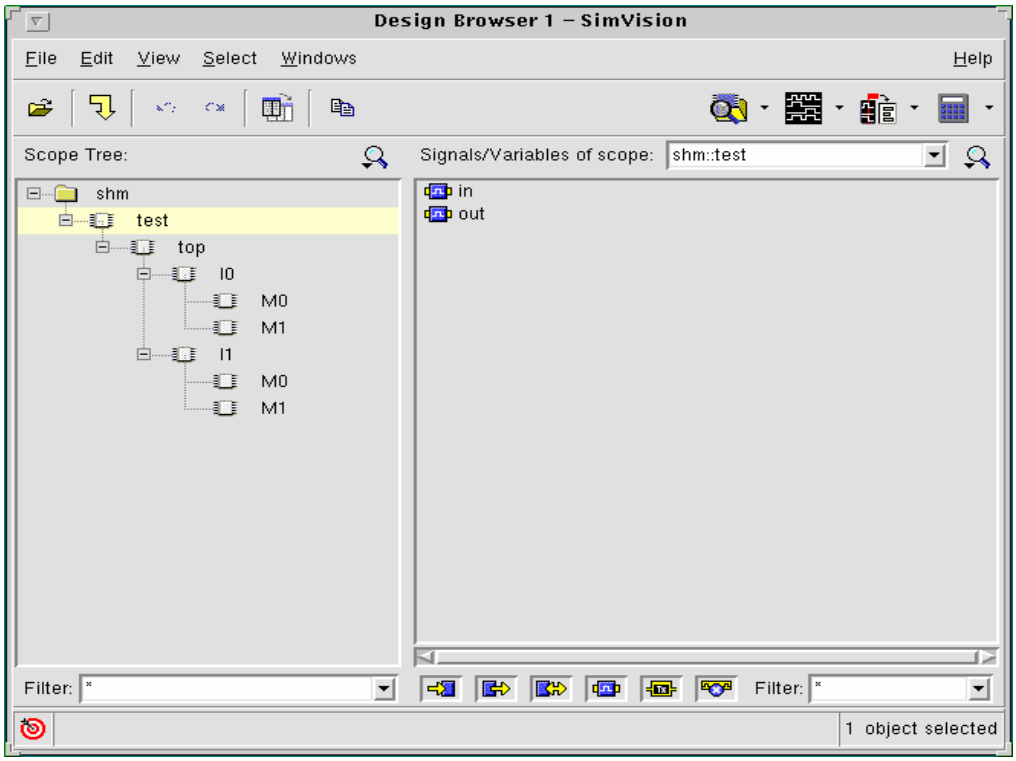

Fig 20: Hierarchy of the circuit

i. In Fig 20 select the signals to be viewed and click on the button circled in Fig 21.

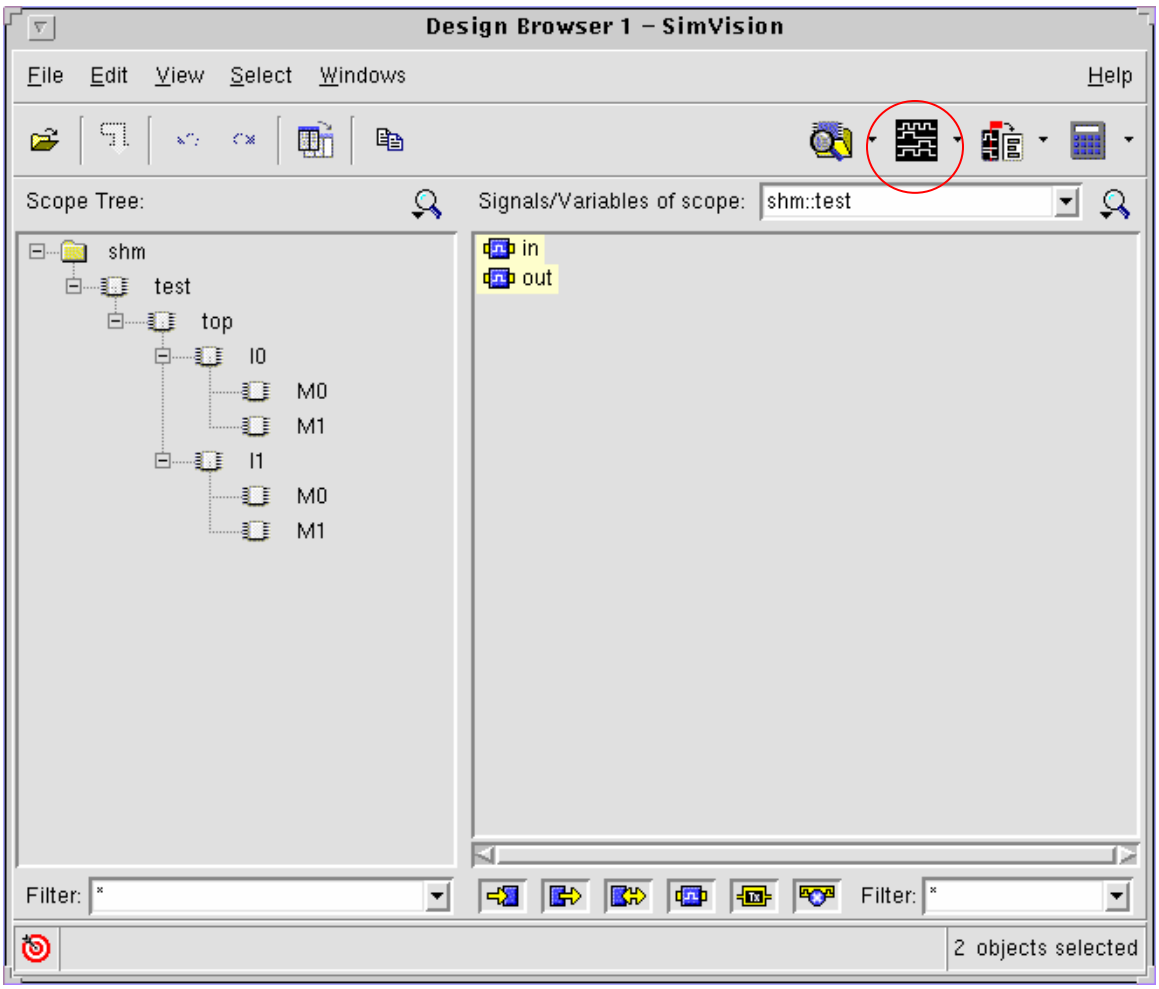

Fig 21: Simvision

j. Now " Waveform 1 – Simvision " window opens as shown in Fig 22

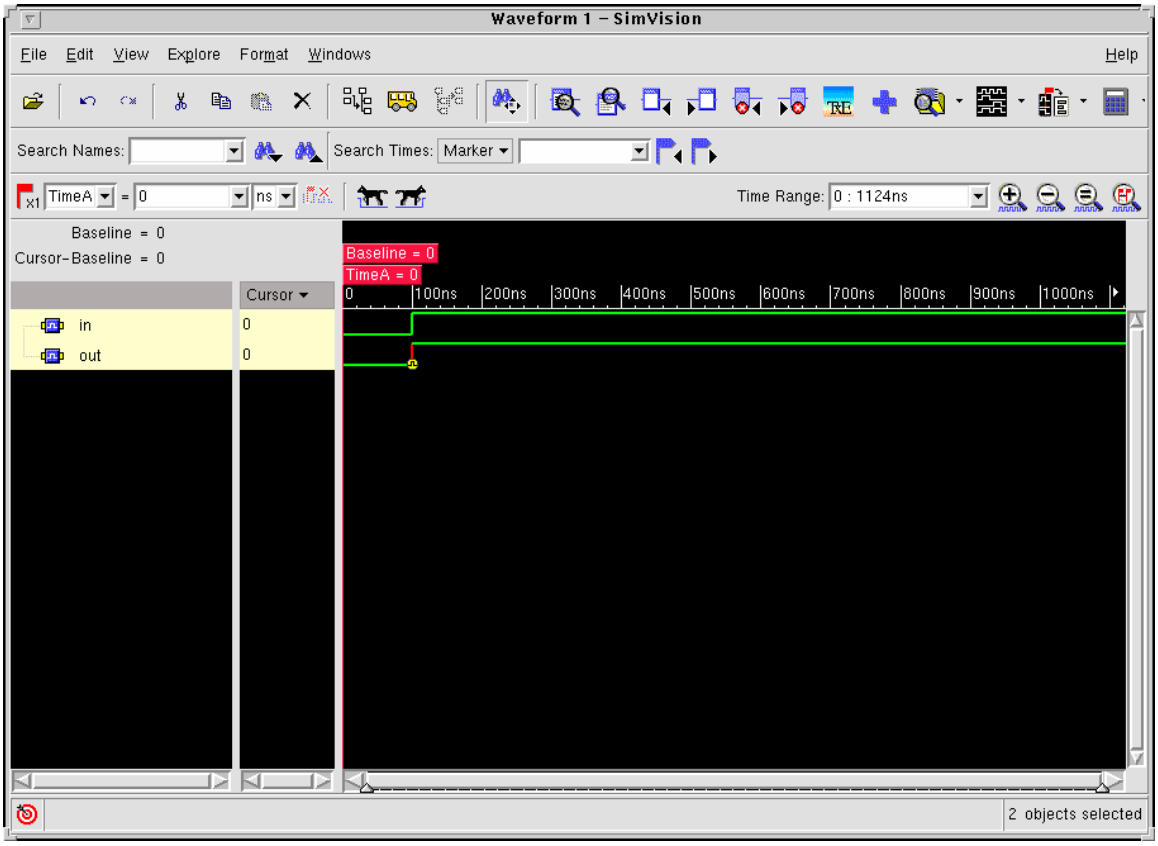

Fig 22: Waveform 1- Simvision

k. The waveforms at all the hierarchies of the circuit can be viewed in a similar way.