Creating a verilog netlist for a schematic:

The verilog netlist is necessary for automatic layout (placement and routing) tools. It contains information about the I/O pins and the connectivity of the entire schematic. Here we have taken an example of two cascaded inverters and the netlists are created for this example. The name of this schematic is inverter.

Important Point:

The names of the schematic and the pins in the schematic should not start with a number. The length of the names should not be more than 15 characters. You should not use '+' and '-'signs for the names of the pins and the schematics.

1. Open the Schematic cell view:

From the Library manager read the inverter schematic cell view. Save the schematic. The inverter schematic is shown in Fig 1.

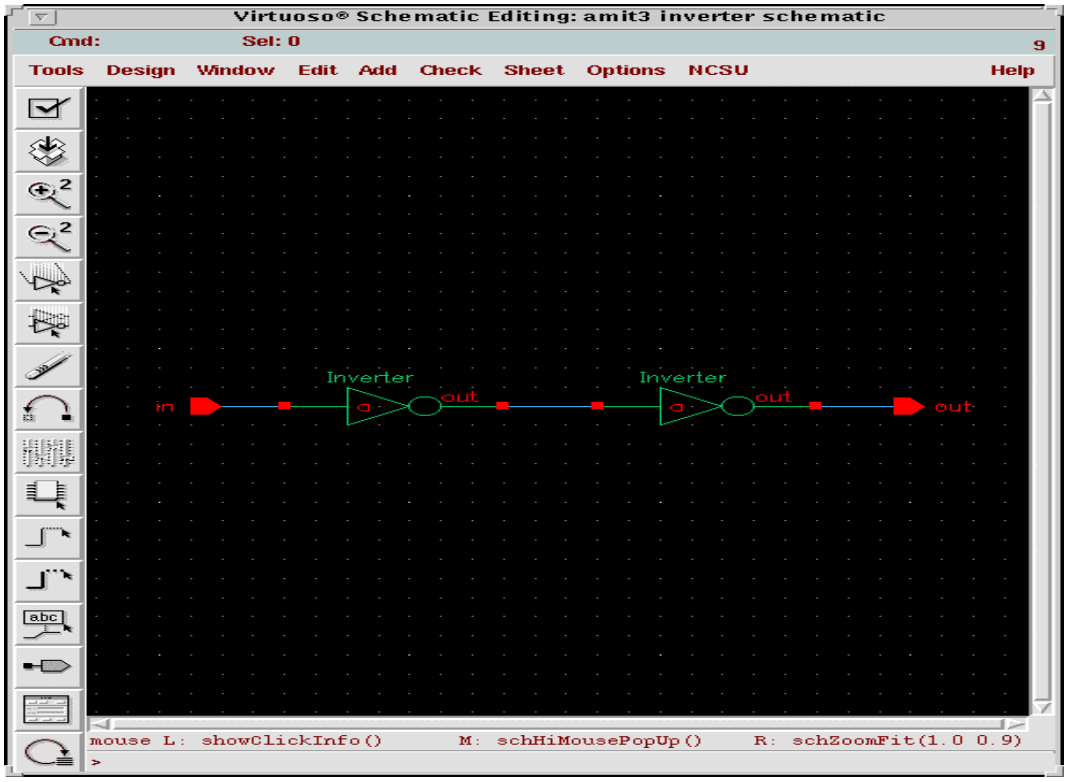

Fig 1: Inverter

2. Initializing Verilog Integration:

a. In Fig 1 select ***Tools –> Simulation –> Verilog - XL*** . The "Setup Environment" window opens as shown in Fig 2.

b. In Fig 2, enter inverter.run1 in the **Run Directory** text box. All other default values are correct. Click ***OK***.

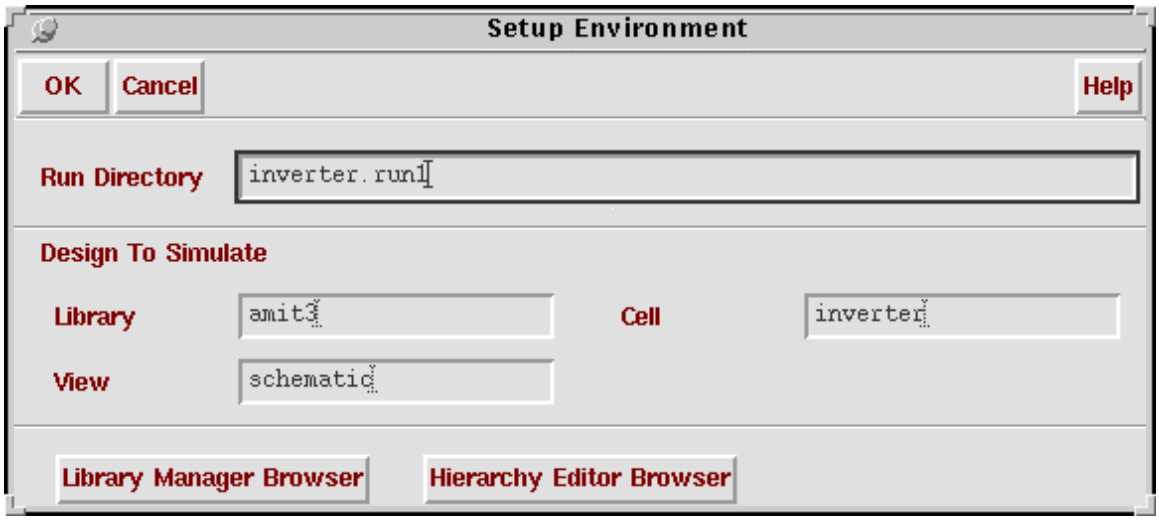

Fig 2: Setup Environment

c. A "Simulation Option Warning" appears as shown in Fig 3. Click ***CLOSE*.**

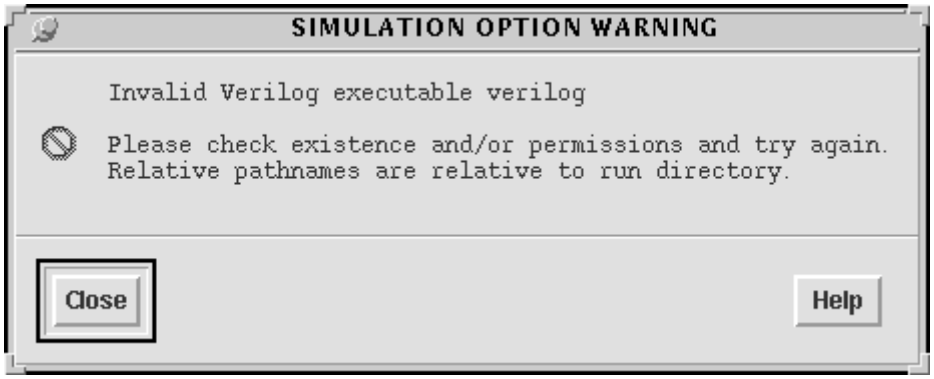

Fig 3: Simulation Option Warning

d. The "Virtuoso Schematic Composer Analysis Environment for Verilog-XL Integration" window opens as shown in Fig 4 and the inverter.run1 directory is created.

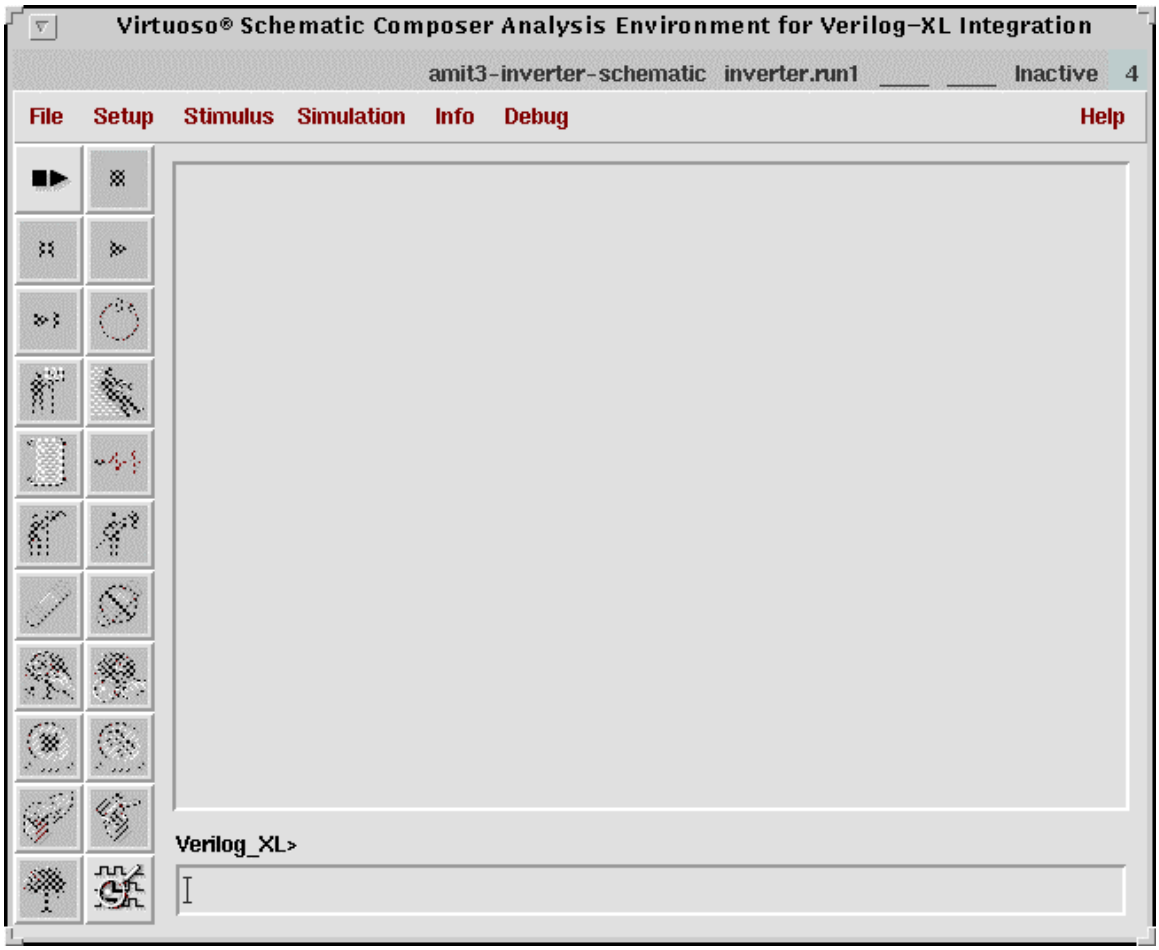

Fig 4: Environment for Verilog-XL Integration

3. Setting the Netlist Options:

a. In Fig 4 set the netlisting options by selecting ***Setup –> Netlist***. The "Verilog Netlisting Options" form opens as shown in Fig 5.
b. The default settings are as shown in Fig 5. They are all correct.

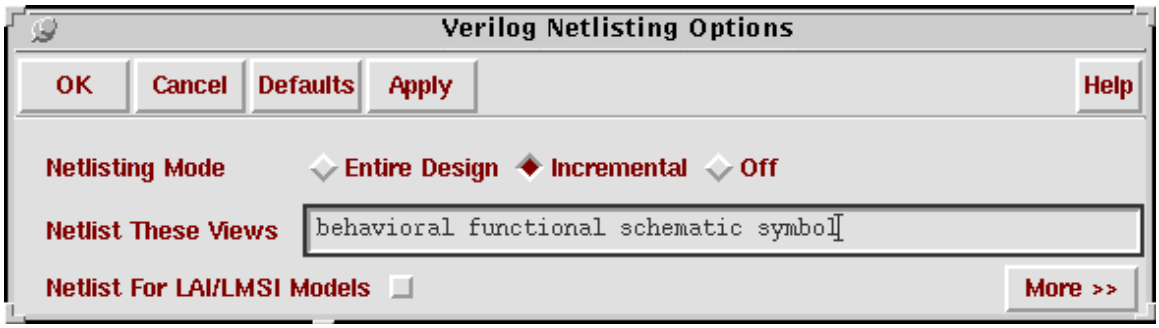

Fig 5: Verilog Netlisting Options

c. In Fig 5 click ***More***>>
Additional netlisting options are added to the form as shown in Fig 6.

d. In Fig 6 set **Global Power Nets** to *vdd* and set **Global Ground Nets** to *gnd*..
e. Select **Generate Pin Map**.
f. The **Drop Port Range** and **Preserve Buses** options are selected by default. It doesn't matter if we select or deselect them.
h. Click ***OK***. Thus setting the Verilog Netlisting Options is done.

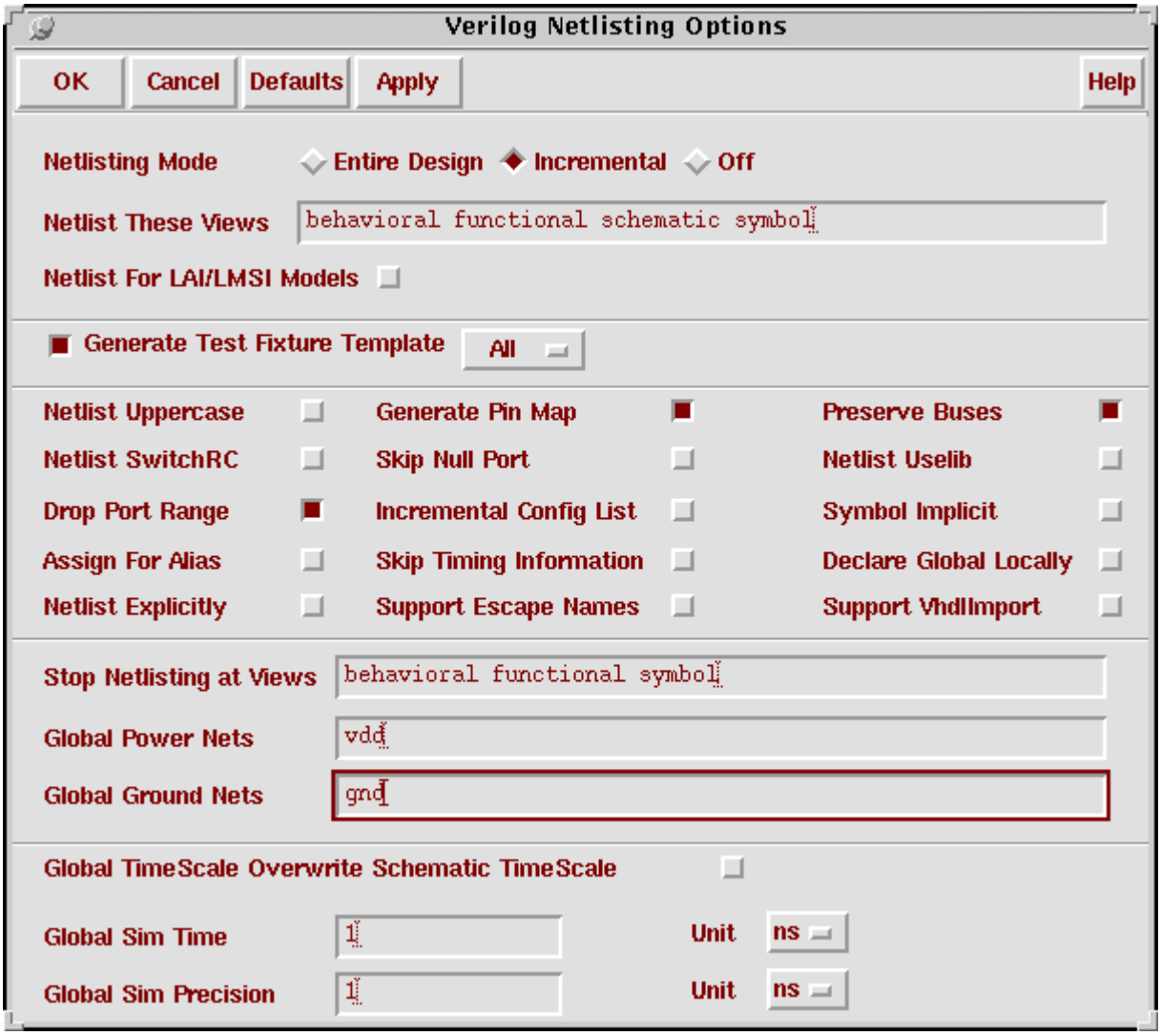

Fig 6: Additional Verilog Netlisting Options

4. Creating the Stimulus File:

a. In the "Virtuoso Schematic Composer Analysis Environment for Verilog-XL Integration" window select ***Stimulus –> Verilog.***
b. A dialog box appears as shown in Fig 7. Click ***Yes*** in the dialog box.

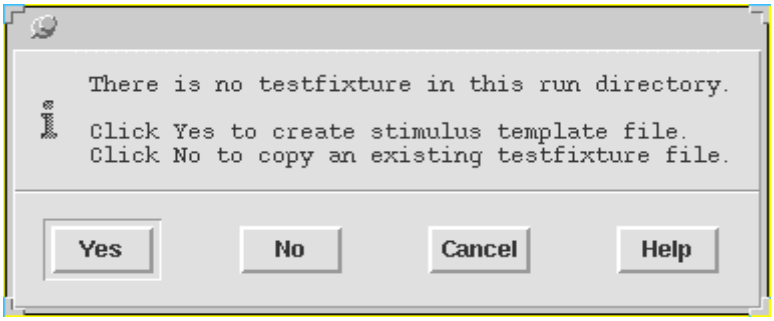

Fig 7: Dialog Box

c. A “Stimulus Options” form opens as shown in Fig 8. Select **textfixture.verilog** as the **File Name** and then click ***OK***.

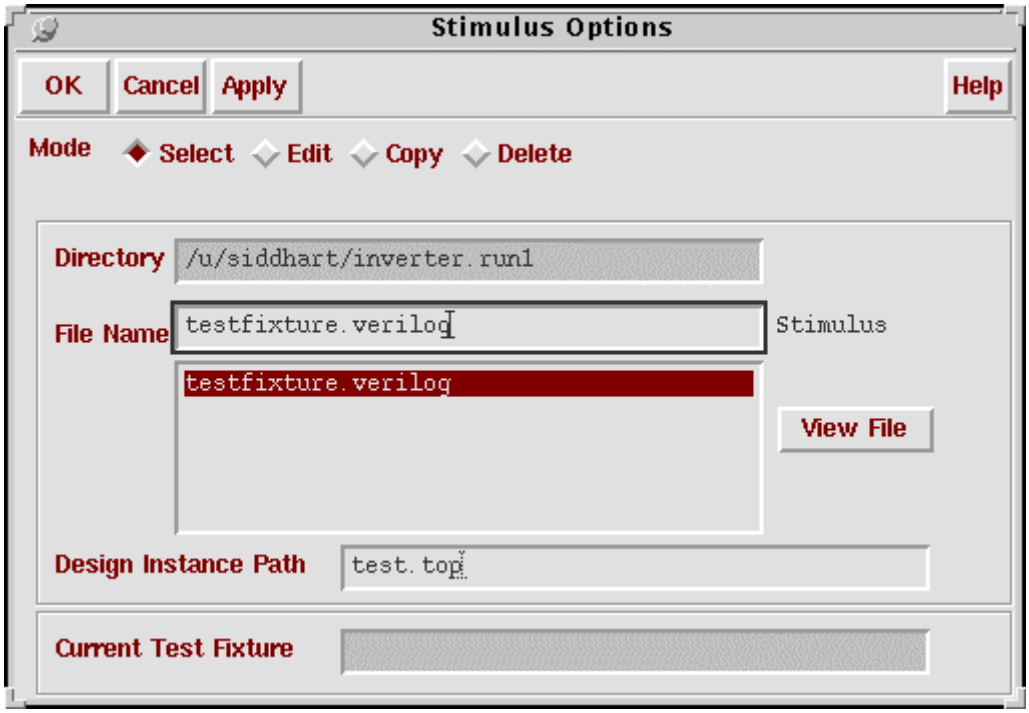

Fig 8: Simulation Options

d. Thus the netlist is created for the schematic.

5. Creating the Verilog Files :

Now we need to make the verilog files from the netlists which are created.

a. Go to the directory

Hostname.ece.pdx.edu >cd /home/ece/siddart/inverter.run1/ihnl.

It has several cds directories. The cds directories have the netlists of all the schematics in the hierarchy. In the "Virtuoso Schematic Composer Analysis Environment for Verilog-XL Integration" window select ***File -> View Netlist Result -> verilog.inpfiles***. The "verilog.inpfiles" window appears as shown in Fig 9. It shows you which cds directory has the netlist for which schematic. Save all the netlists in the silicon ensemble directory with a .v extension.

b. Run the Verilog correction (verilog_correction) script on the netlist of the top cell. This file is run by the following command.

Hostname.ece.pdx.edu > verilog_correction old verilog file name.v > new file name.v

Reason for verilog netlist correction:

In the verilog netlist the power and ground nets are named as cds_globals.vdd_ and cds_globals.gnd_.In our schematic the power and ground nets are named as vdd and gnd. So cds_globals.vdd_ and cds_globals.gnd_ needs to be changed to vdd and gnd.

NOTE: If the power and ground nets in your schematic are named as vdd! and gnd!, this verilog_correction script needs to be changed. In this case the cds_globals.vdd_ and cds_globals.gnd_ needs to be changed to vdd_ and gnd_.

Thus the Verilog files for all the schematics are ready.

Important Point: Make sure that the verilog module name and the LEF file macro name is the same for every standard cell.

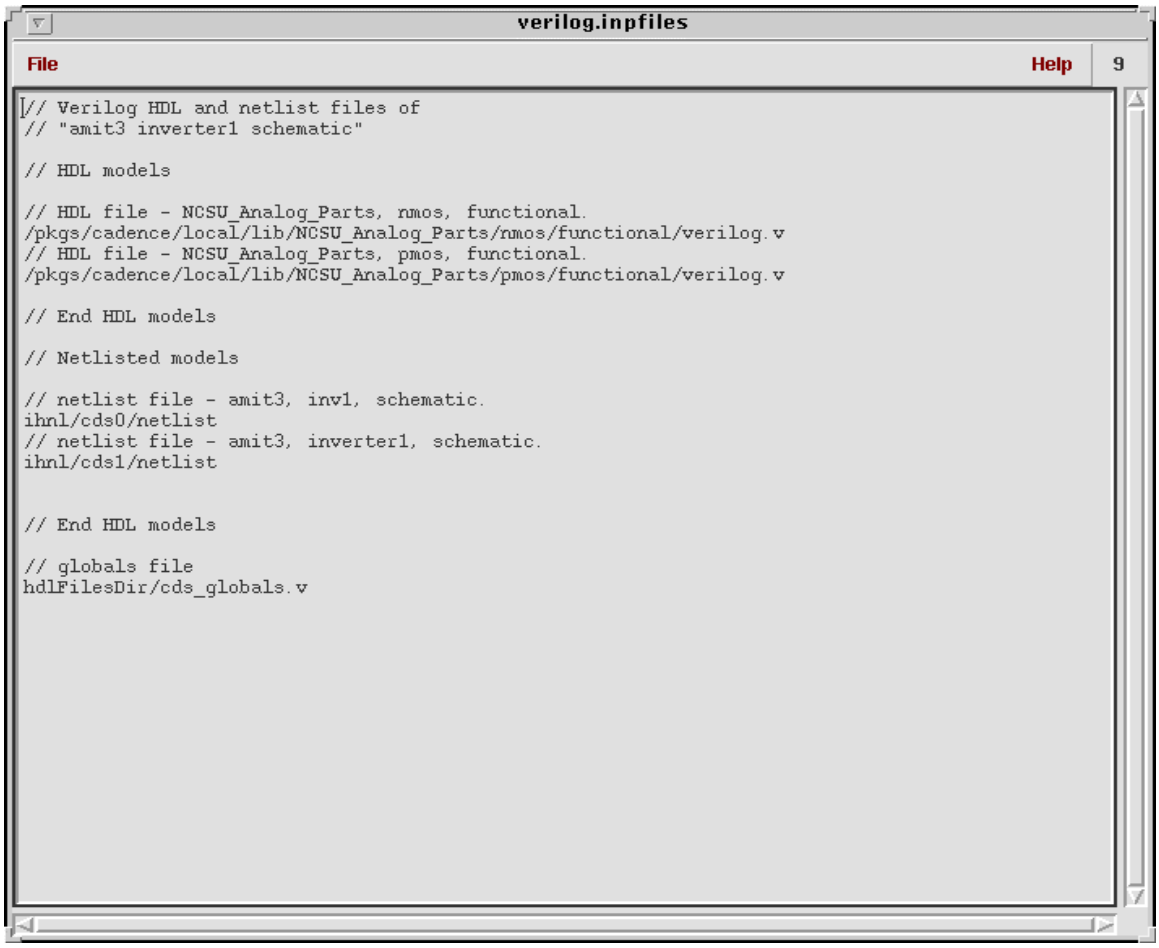

Fig 9: verilog.inpfiles

Thus the verilog netlists for your design have been created. Now use Tutorial 4 to do placement and routing using Silicon Ensemble.