Analog Artist Tutorial

This tutorial is designed to introduce you to the tools we will use in ECE 746. It will introduce you to the **Cadence Environment**, specifically **Composer**, **Analog Artist** and the **Results Browser**.

The following typeface and color conventions will be used in this document:

- General Text: add cadence
- Commands / Menu Selections: **`add cadence`**
- Screen Output: *add cadence*

1. Starting the Cadence Environment:

% **`add cadence`**

Use the following commands to start Cadence applications:

openbook   Cadence online documentation

icde &   Basic digital and analog design entry
icds &   Front end design
icms &   Front end analog, mixed signal and microwave design
icca &   Cell based chip assembly
layout &   Basic layout with interactive DRC
layoutPlus &   Basic layout plus automated design tools
msfb &   Mixed-signal IC design
icfb &   Front to back design

spectre <input file> &   Spectre circuit simulator
verilog <input file> &   Verilog HDL simulator
signalscan &   Analog/digital waveform display

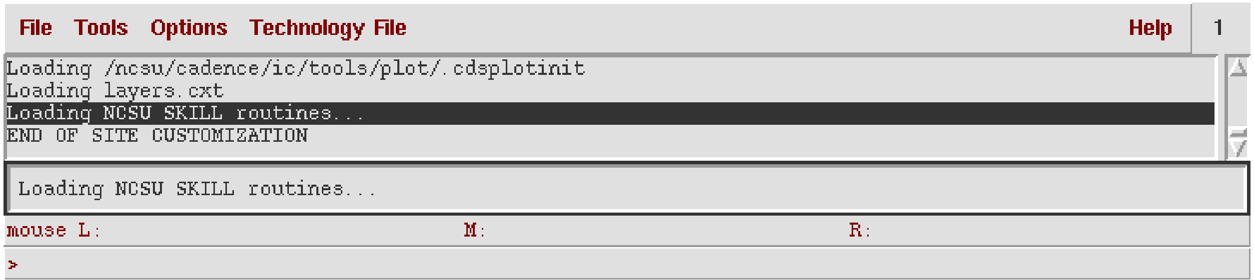
We are now using version 4.4.5 of the Cadence IC tools. If you require version 4.4.2, please type "add cad442" instead.

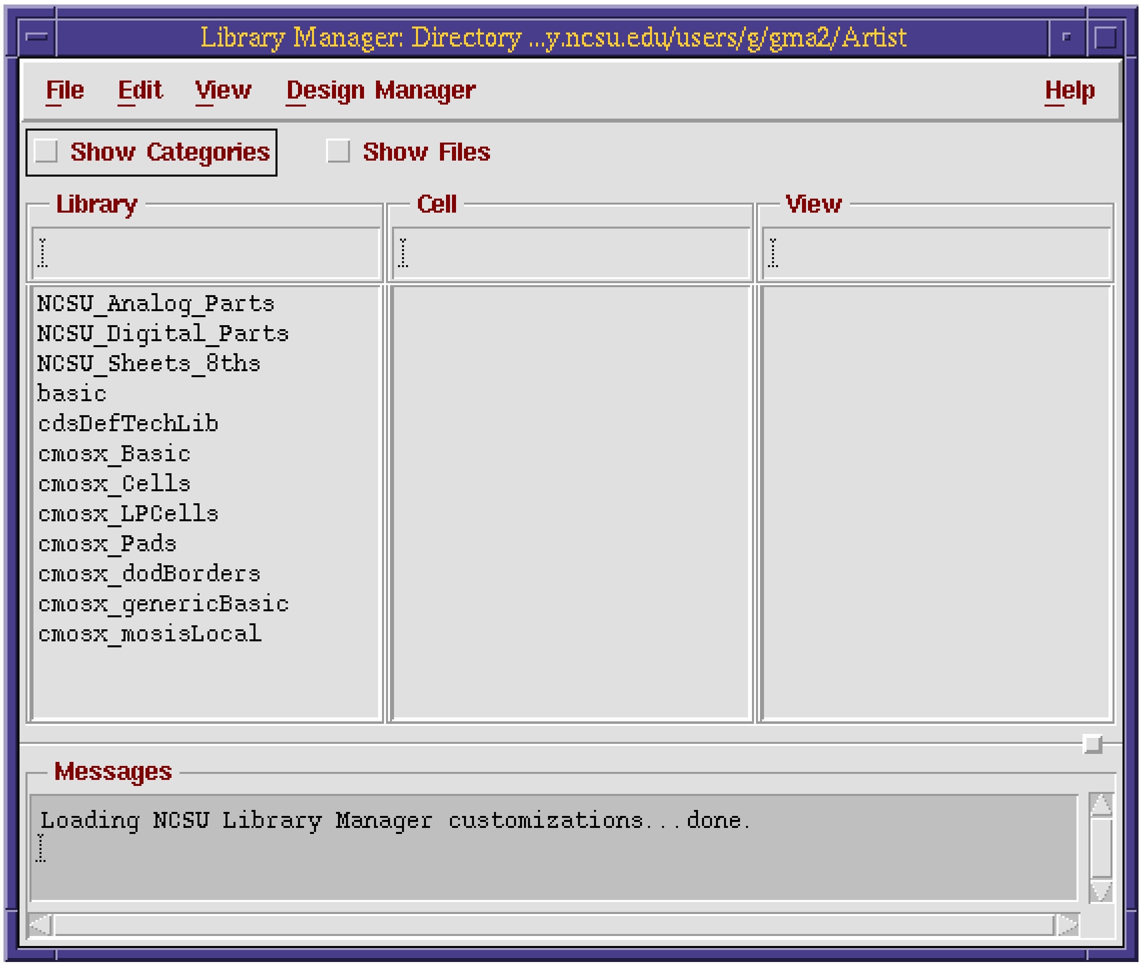
Problems with the tools? Wondering where SimWaves went? Check the FAQ at

http://www.ece.ncsu.edu/cadence/doc/cdsuser/

% **`mkdir Artist`**
% **`cd Artist`**
% **`icfb &`**

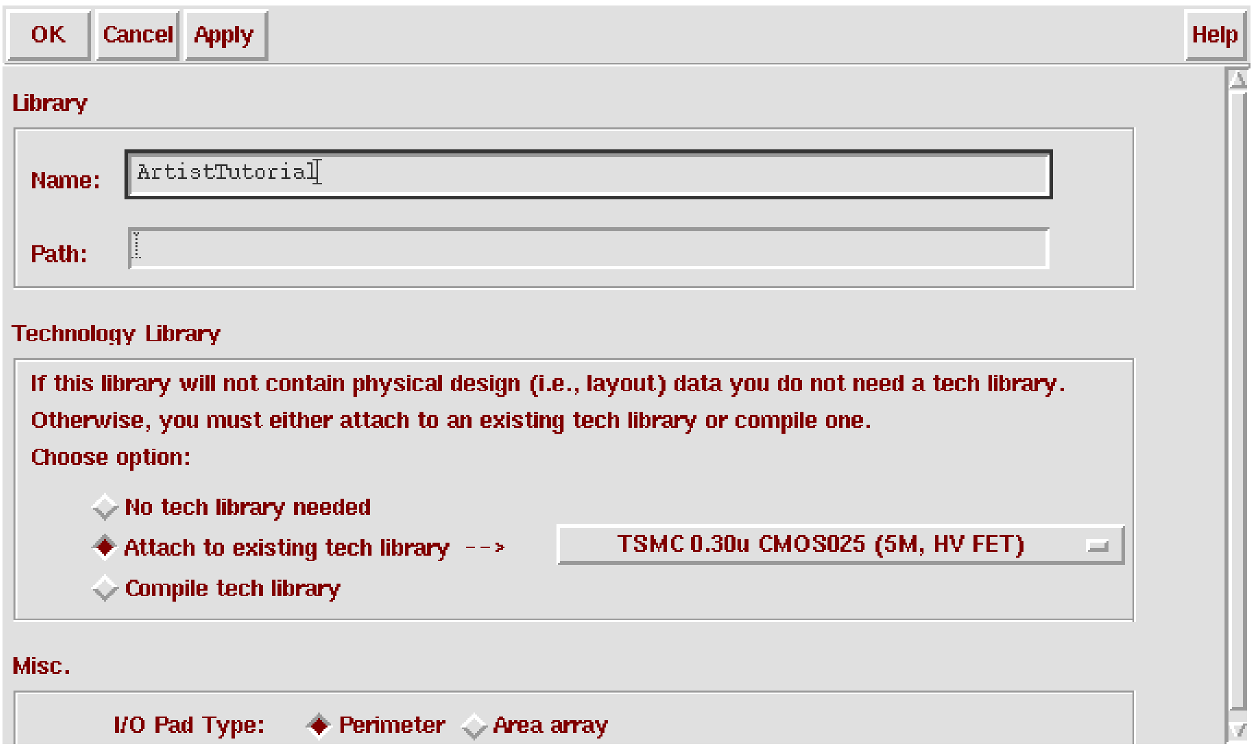
A few seconds later, you'll see **CIW** (Command Interpreter Window) and **Library Manager**


File Tools Options Technology File Help 1
Loading /ncsu/cadence/ic/tools/plot/.cdsplotinit
Loading layers.cxt
Loading NCSU SKILL routines...
END OF SITE CUSTOMIZATION
Loading NCSU SKILL routines...
mouse L:
M:
R:
>

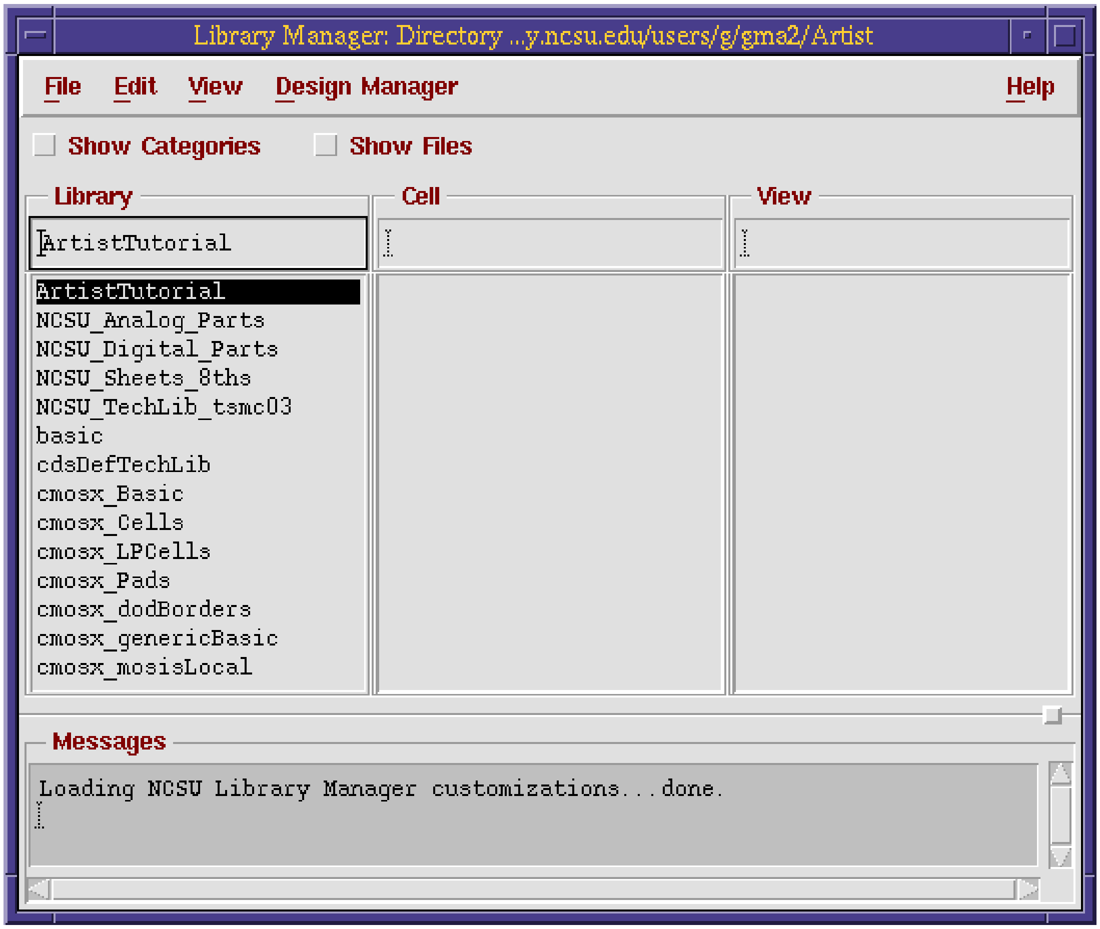

Library Manager: Directory ...y.ncsu.edu/users/g/gma2/Artist
File Edit View Design Manager Help
Show Categories
Show Files
Library
Cell
View
NCSU_Analog_Parts
NCSU_Digital_Parts
NCSU_Sheets_8ths
basic
cdsDefTechLib
cmosx_Basic
cmosx_Cells
cmosx_LPCells
cmosx_Pads
cmosx_dodBorders
cmosx_genericBasic
cmosx_mosisLocal
Messages
Loading NCSU Library Manager customizations...done.

2. Create a Design Library:

In **Library Manager**, Click **File -> New -> Library**
In the **Name** field, enter "**ArtistTutorial**"
In the **Technology Library** box, select
Attach to existing tech library -> TSMC 0.30u
Press **OK**

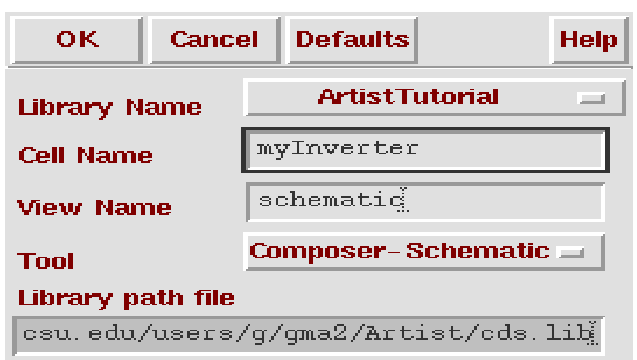


Then the Library Manager will refresh as follows:

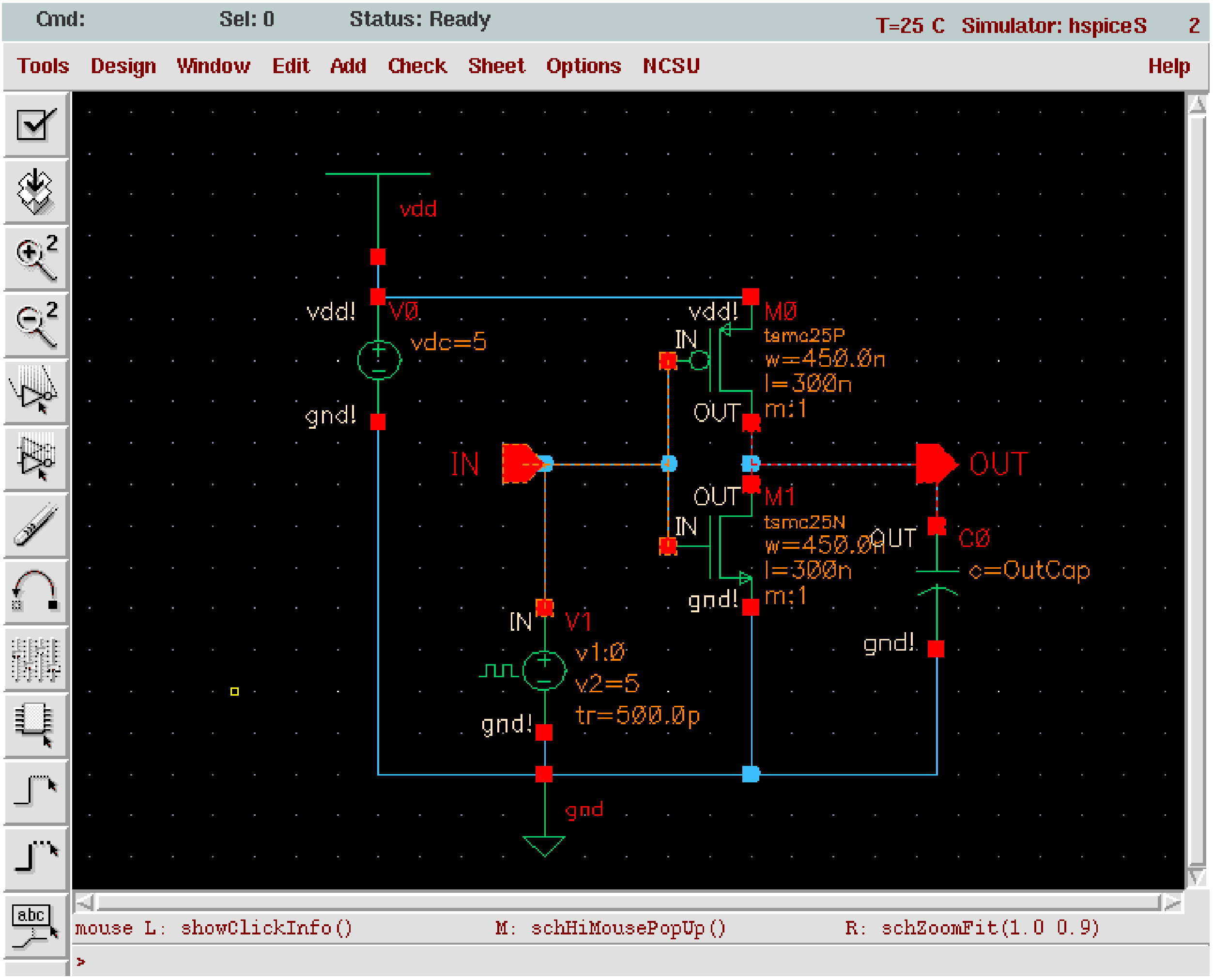


3. Create a Schematic:

In **Library Manager,** select **ArtistTutorial**
From the Menu Bar, select **File -> New -> CellView**
Fill the Form as follows, then click **OK**

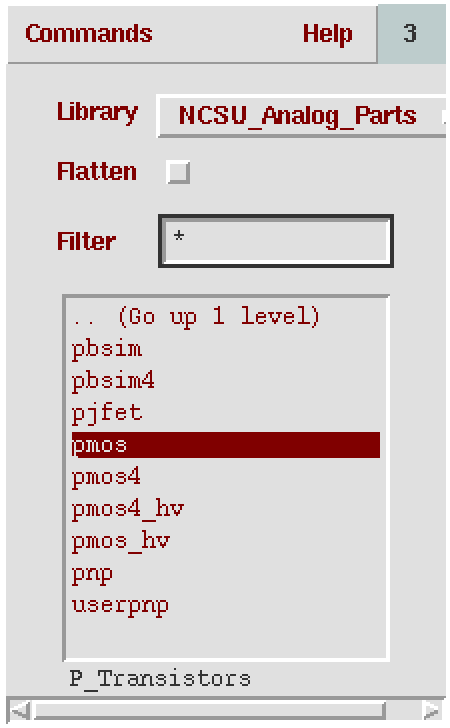


A blank Schematic window will then appear.
We need to generate a schematic as shown below:



To generate a schematic like this, you will need to go through the following steps:

From the **Schematic Window** menu, select **`Add -> instance`**
The **Component Browser**, will then pop up.



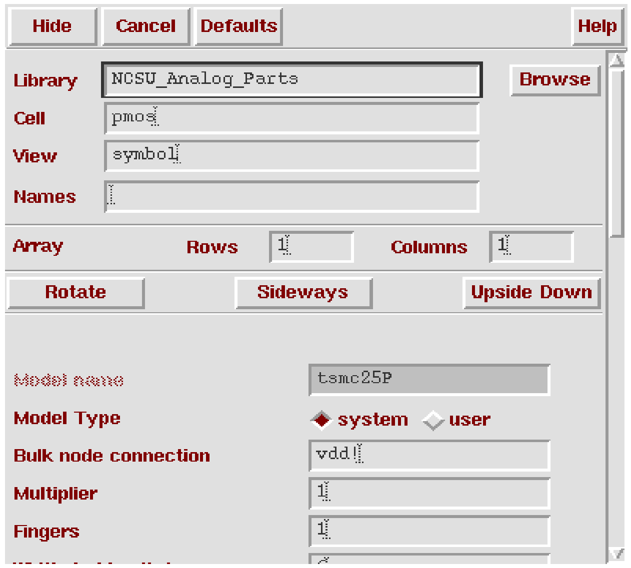
In the **Library** field, select **NCSU_Analog_Parts**
We will place the following instances in the **Schematic Window** from the **NCSU_Analog_Parts** library as instructed below:

N_Transistor	**:**	***nmos***
P_Transistor	**:**	***pmos***
Supply_Nets	**:**	***vdd , gnd***
Voltage_Sources	**:**	***vdc,vpulse***
R_L_C	**:**	***cap***

Note: pay attention to the parameters specified in *vdc, vpulse,* and *cap.* These parameters are very important in simulation

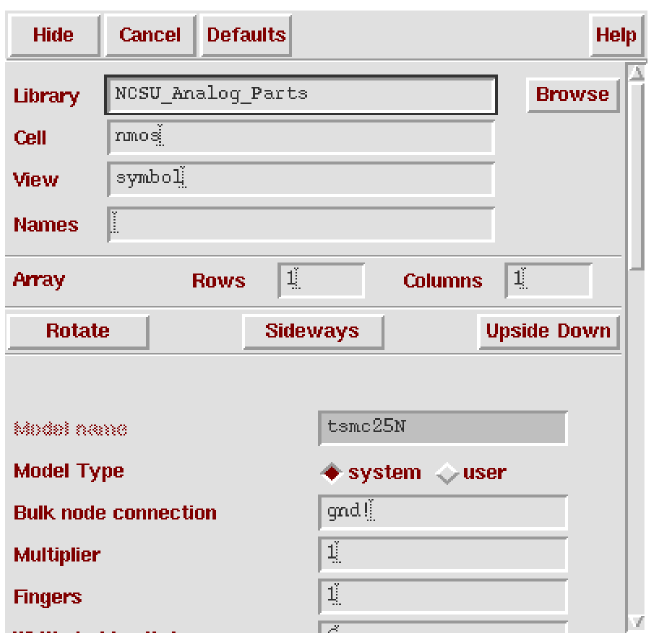
A. Place pmos instance:

In **Component Browser**, select `P_Transistor` and then `pmos`
Place it in the **Schematic Window**



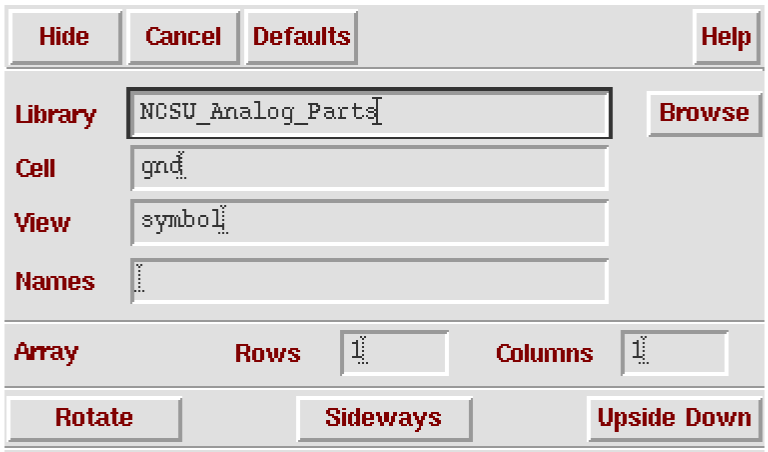
B. Place nmos instance:

In **Component Browser**, select `N_Transistor` and then `nmos`
Place it in the **Schematic Window**



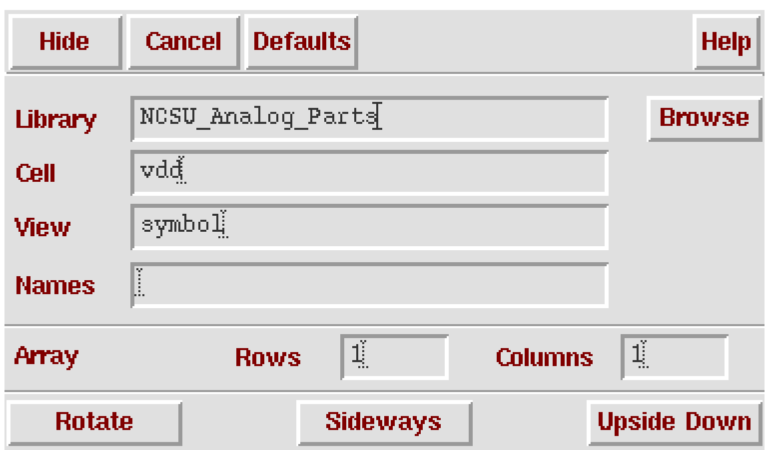
C. Place gnd instance:

In **Component Browser**, select **Supply_Nets** and then **gnd**
Place it in the **Schematic Window**



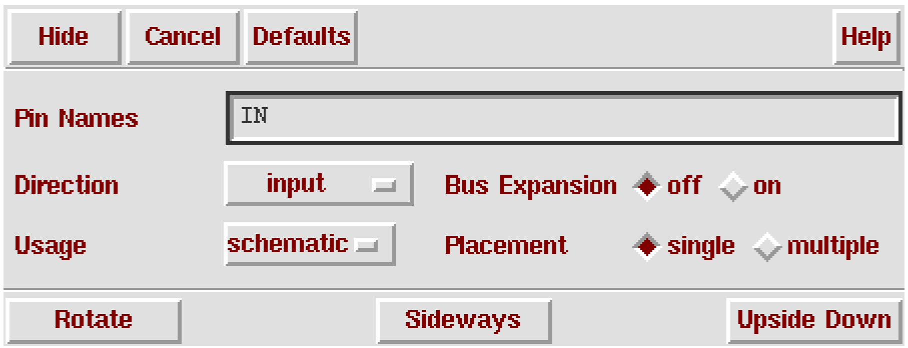
D. Place vdd instance:

In **Component Browser**, select **Supply_Nets** and then **vdd**
Place it in the **Schematic Window**



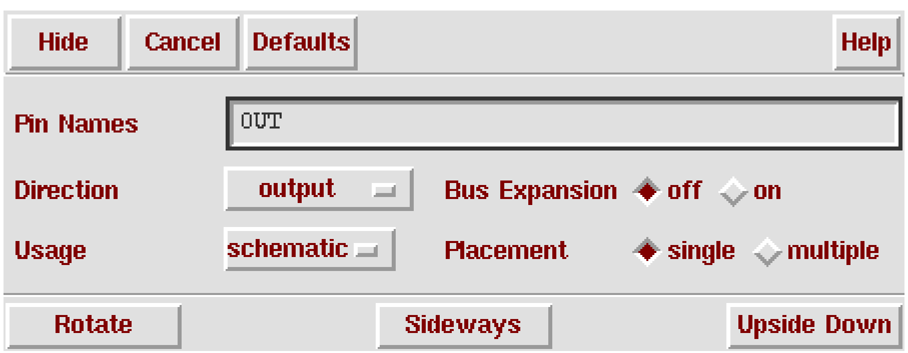
E. Place IN pin:

From the **Schematic Window** menu, select **`Add -> Pin...`**
In the Pin Name field , enter “**`IN`**”
In the Direction field, select **`input`**
Place it in the **Schematic Window**



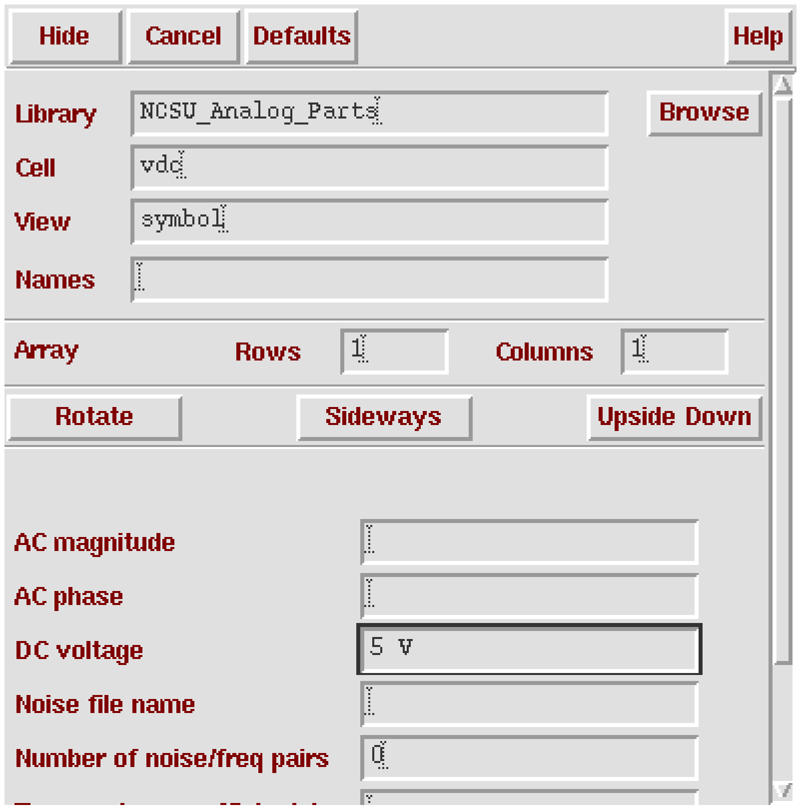
F. Place OUT pin:

From the **Schematic Window** menu, select **`Add -> Pin...`**
In the Pin Name field , enter “**`OUT`**”
In the Direction field, select **`output`**
Place it in the **Schematic Window**



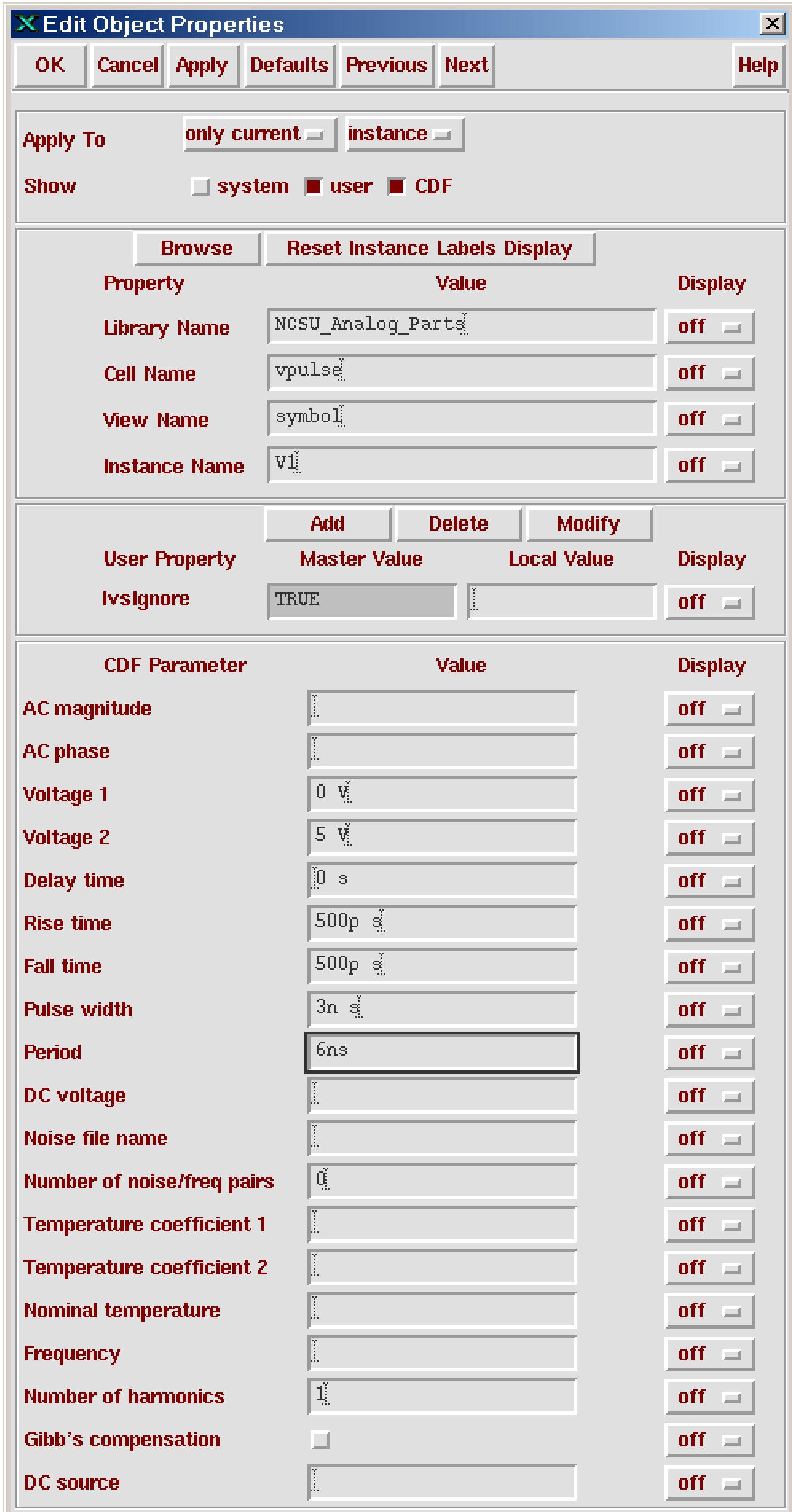
G. Place vdc instance

In **Component Browser**, select `Voltage Sources` and then `vdc`
In the DC voltage field, enter “`5 V`”
Place it in the **Schematic Window**



H. Place vpulse instance

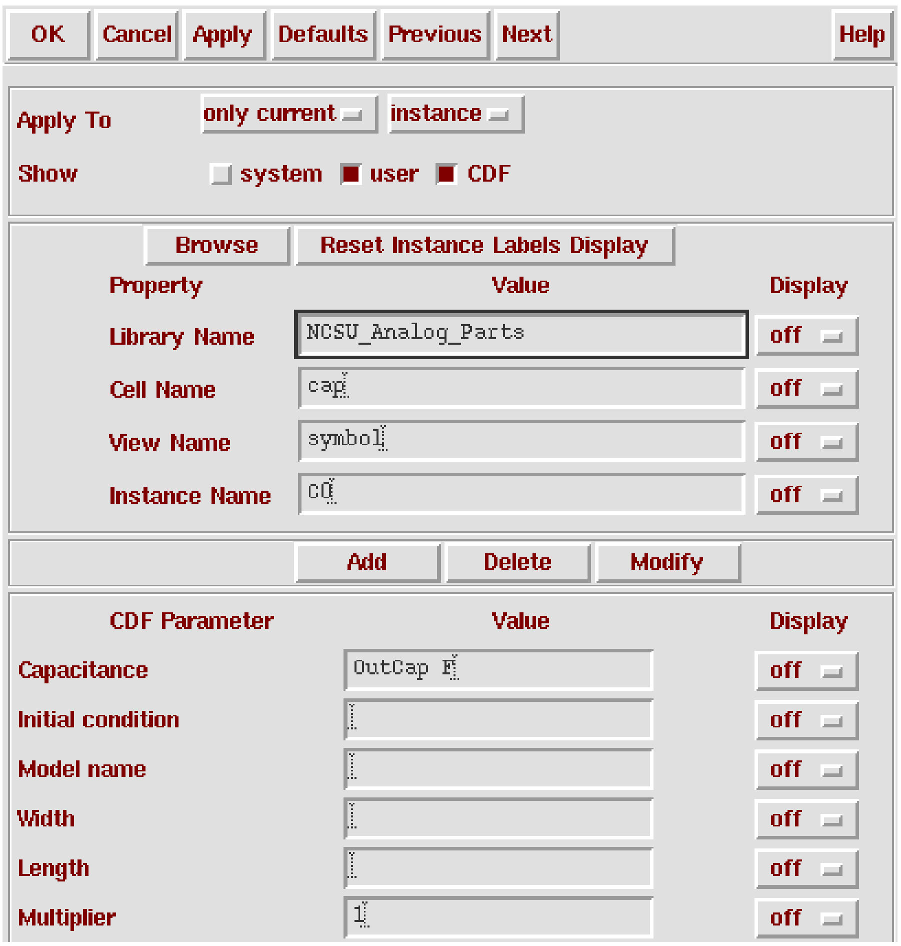
In **Component Browser**, select `Voltage_Sources` and then `vpulse`
Enter the values as shown in the following form (next page)
Place it in the **Schematic Window**


Edit Object Properties
OK
Cancel
Apply
Defaults
Previous
Next
Help
Apply To
only current
instance
Show
system
user
CDF
Browse
Reset Instance Labels Display
Property
Value
Display
Library Name
NCSU_Analog_Parts
Cell Name
vpulse
View Name
symbol
Instance Name
V1
Add
Delete
Modify
User Property
Master Value
Local Value
lvsIgnore
TRUE
CDF Parameter
AC magnitude
AC phase
Voltage 1
0 V
Voltage 2
5 V
Delay time
0 s
Rise time
500p s
Fall time
500p s
Pulse width
3n s
Period
6ns
DC voltage
Noise file name
Number of noise/freq pairs
0
Temperature coefficient 1
Temperature coefficient 2
Nominal temperature
Frequency
Number of harmonics
1
Gibb's compensation
DC source
off

I. Place cap instance

In **Component Browser**, select **R_L_C** and then **cap**
In the Capacitance field, enter "**OutCap F**"
(This **Design Variable** will be used in **Artist**.)

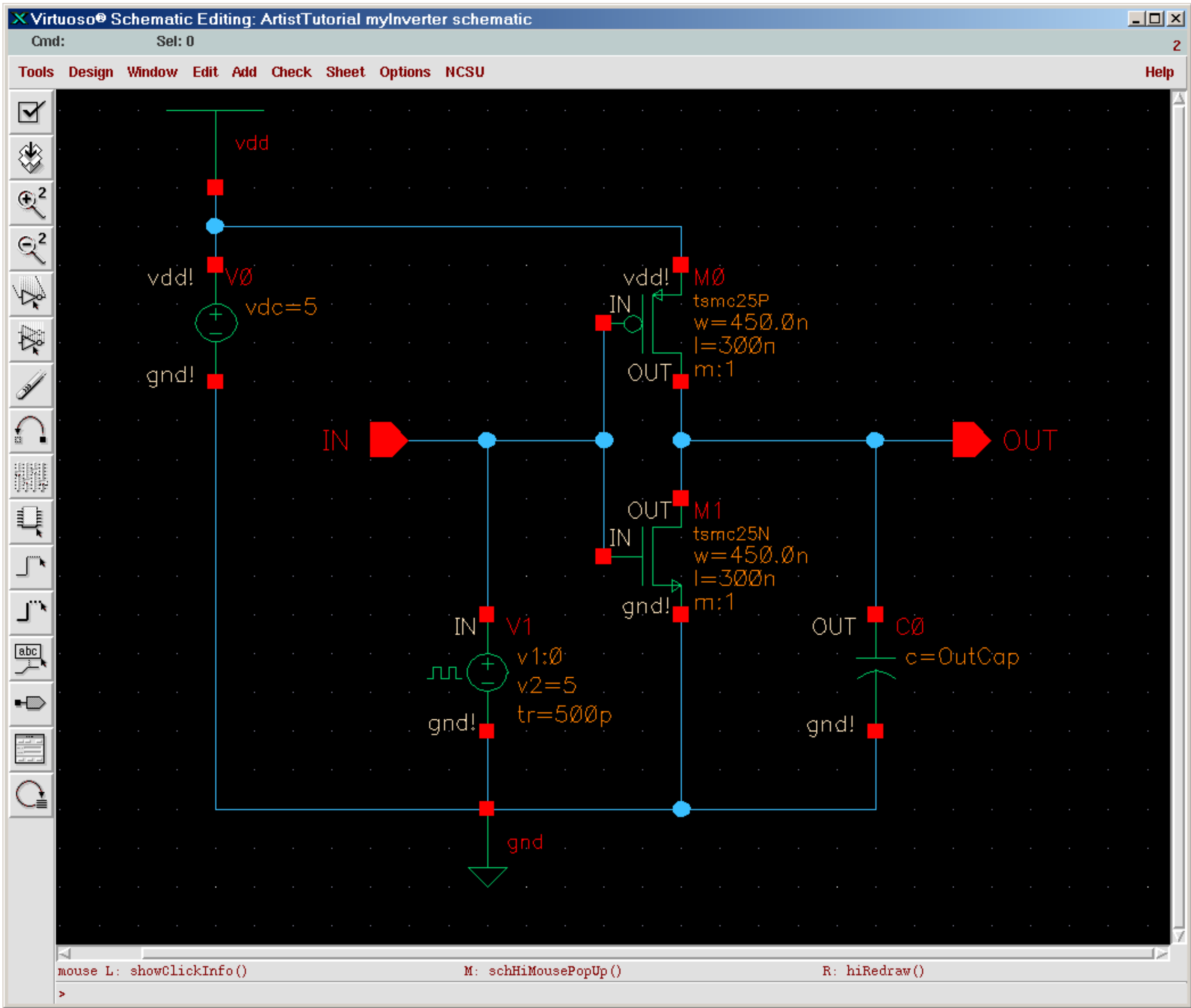
Place it in the **Schematic Window**



J. Place wires

In the **Schematic Window** menu, select **Add -> Wire (narrow)**
Place the wire to connect all the instances
Select **Design -> Check and Save**. CIW will report any errors.

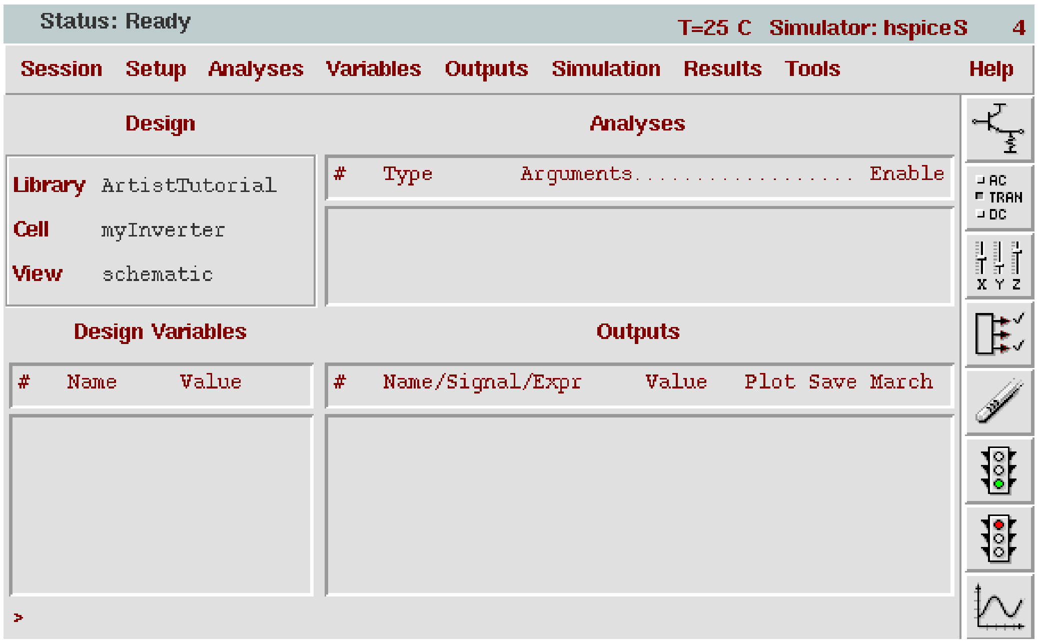
Your schematic should look like the one shown below.



4. Set up the Simulation Environment

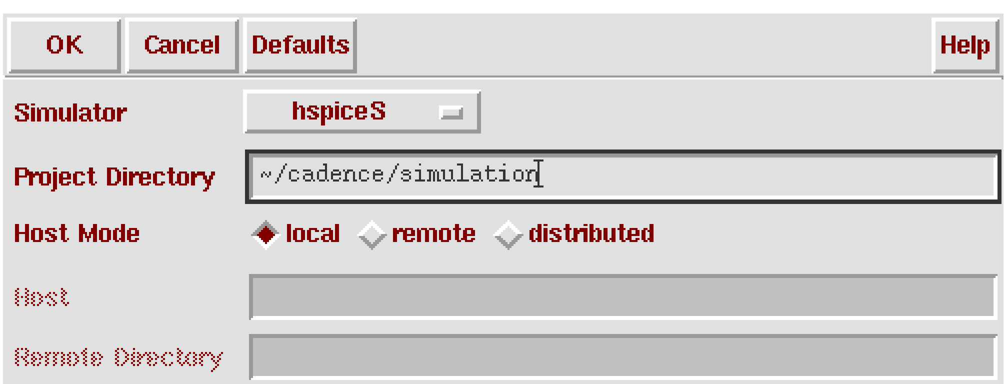
You are now prepared to simulate your circuit.

From the **Schematic Window** menu, select **Tools -> Analog Environment**
A window will pop-up. This window is the **Analog Artist Simulation Window**.



A. Choose a Simulator

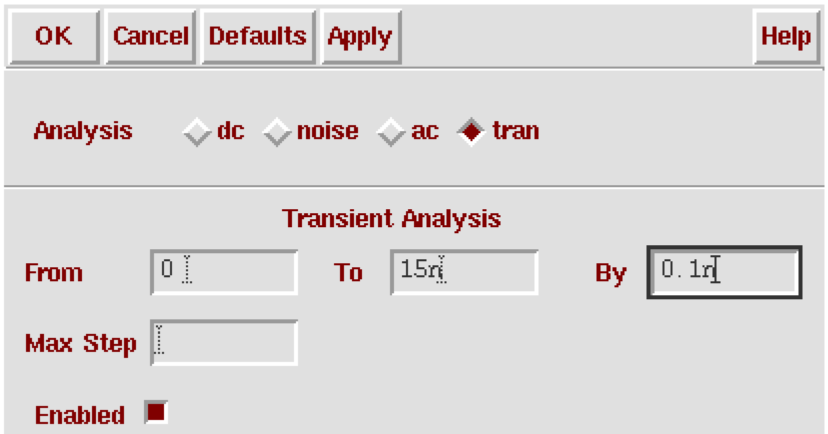
From the **Analog Artist** menu, select **Setup -> Simulator/Directory/Host**.
Enter the fields as shown below.
Choose **hspiceS** as your simulator.
Your simulation will run in the specified Project Directory.
You may choose any valid pathname and filename that you like.



B. Choose Analysis

We will do Transient Analysis on the circuit that we just produced.

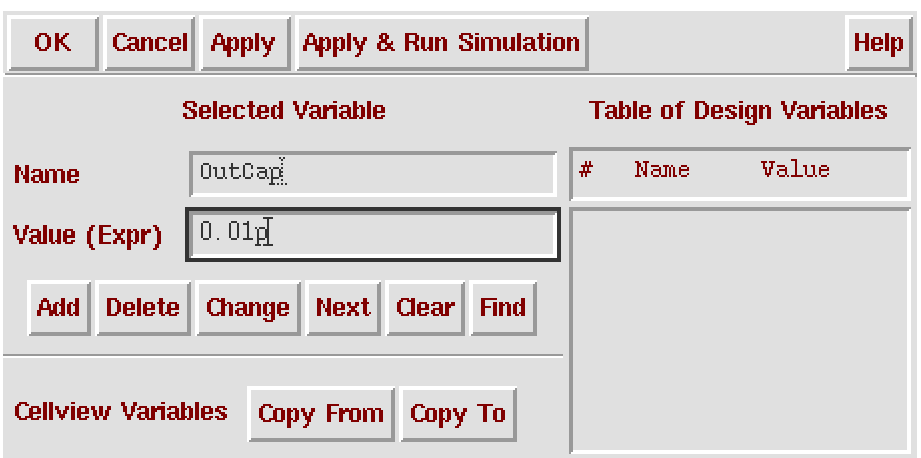
From the **Analog Artist** menu, select **Analyses -> Choose...**
Fill out the form as follows:



C. Add a Variable

From the **Analog Artist** menu, select **Variables -> Edit**
The **Editing Design Variables** form will appear.
Fill out the form as shown below, and then click **Add** to send this Variable to the Table of Design Variables.

(We entered the OutCap Design Variable in section 3.I.)



D. Setup Output

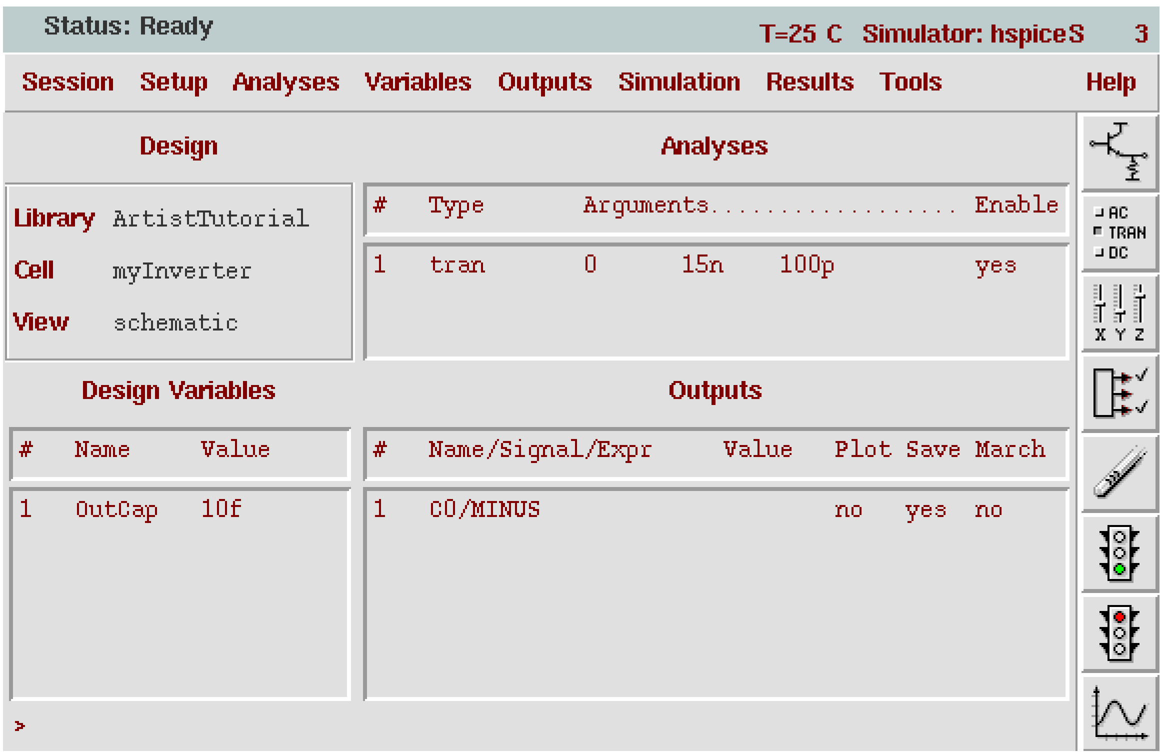
When using Transient Analysis, the transient voltage will be saved automatically.
We can save the current through capacitor C0 in the schematic by doing the following:

From the **Analog Artist** menu, select

`Outputs -> To be Saved -> Select On Schematic`

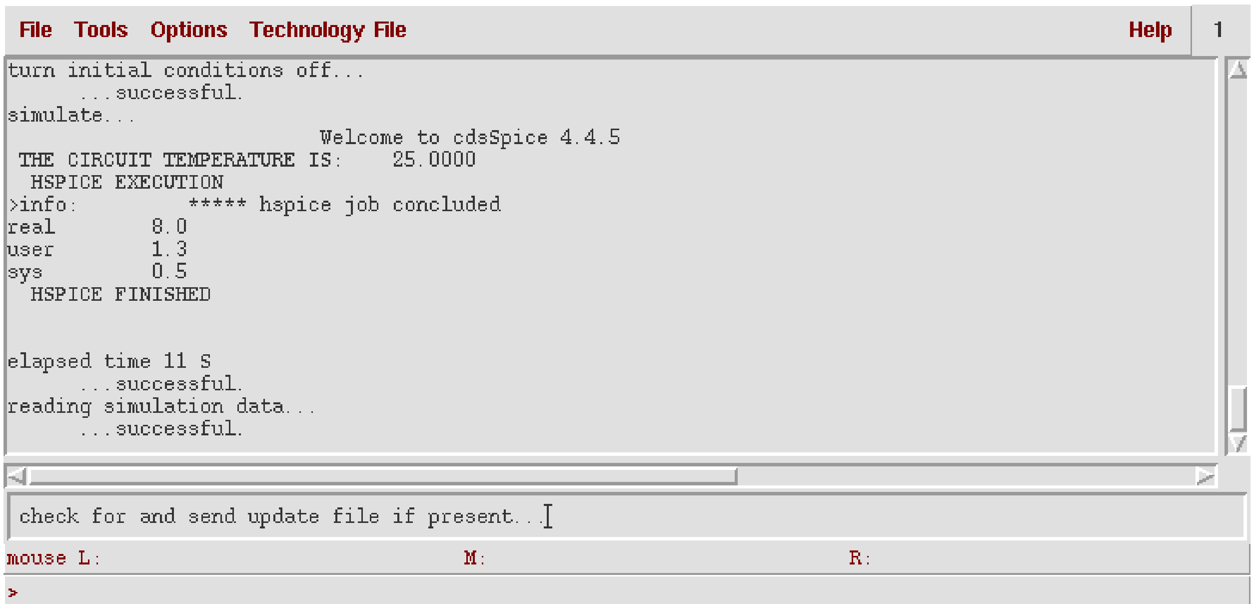
In the **Schematic Window**, click on the lower terminal (not the wire) of capacitor C0.

After you click on the terminal, the **Analog Artist Window** should look like this:



5. Run Simulation

From the **Analog Artist** menu, select **Simulation -> Run**,
Look at the echoing information in the **CIW** window.
If the simulation succeeds, the window will display "...successful."

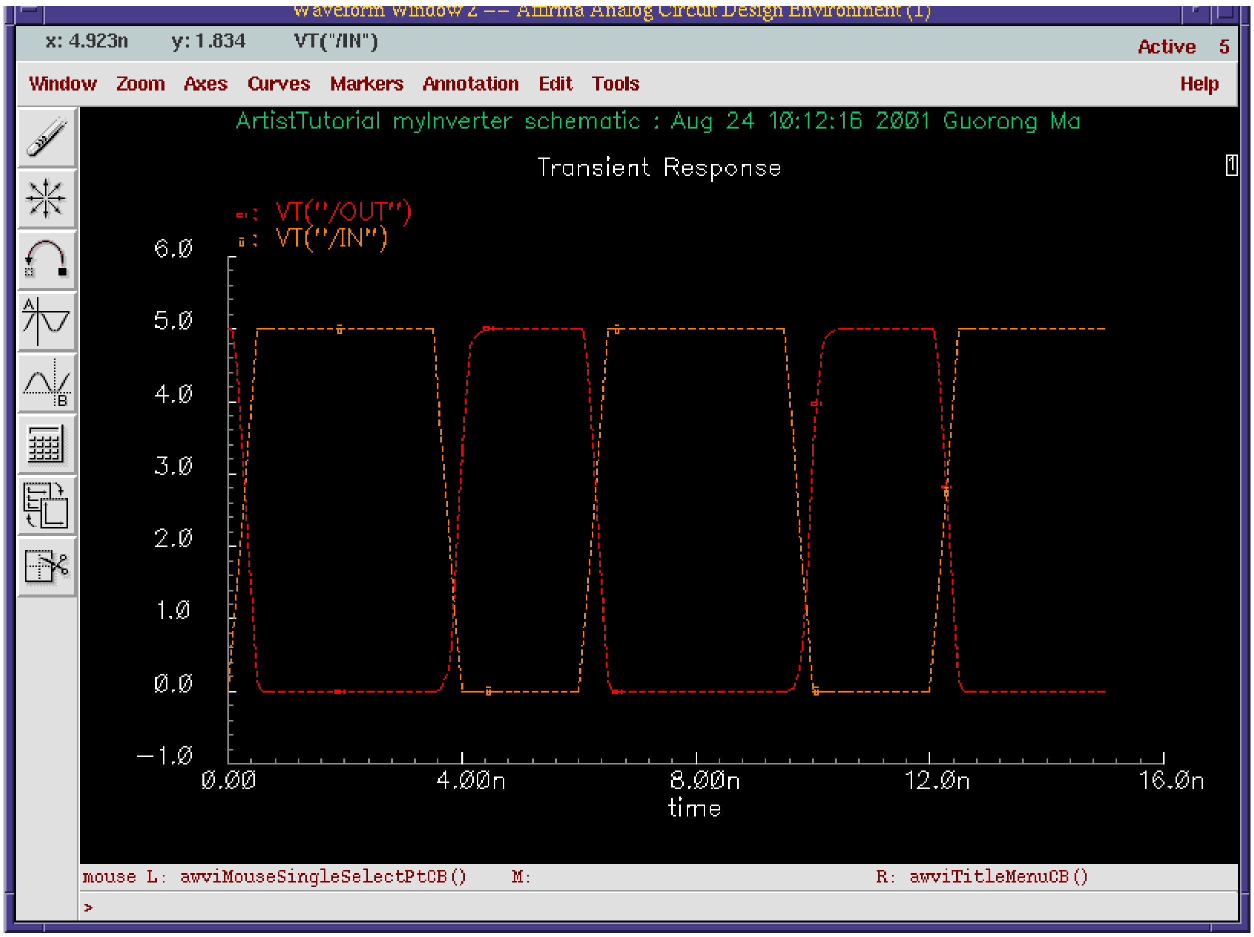


6. View Waveforms

From the **Analog Artist** menu, select
    Results -> Direct Plot -> Transient Signal
The **Waveform Window** will then pop up

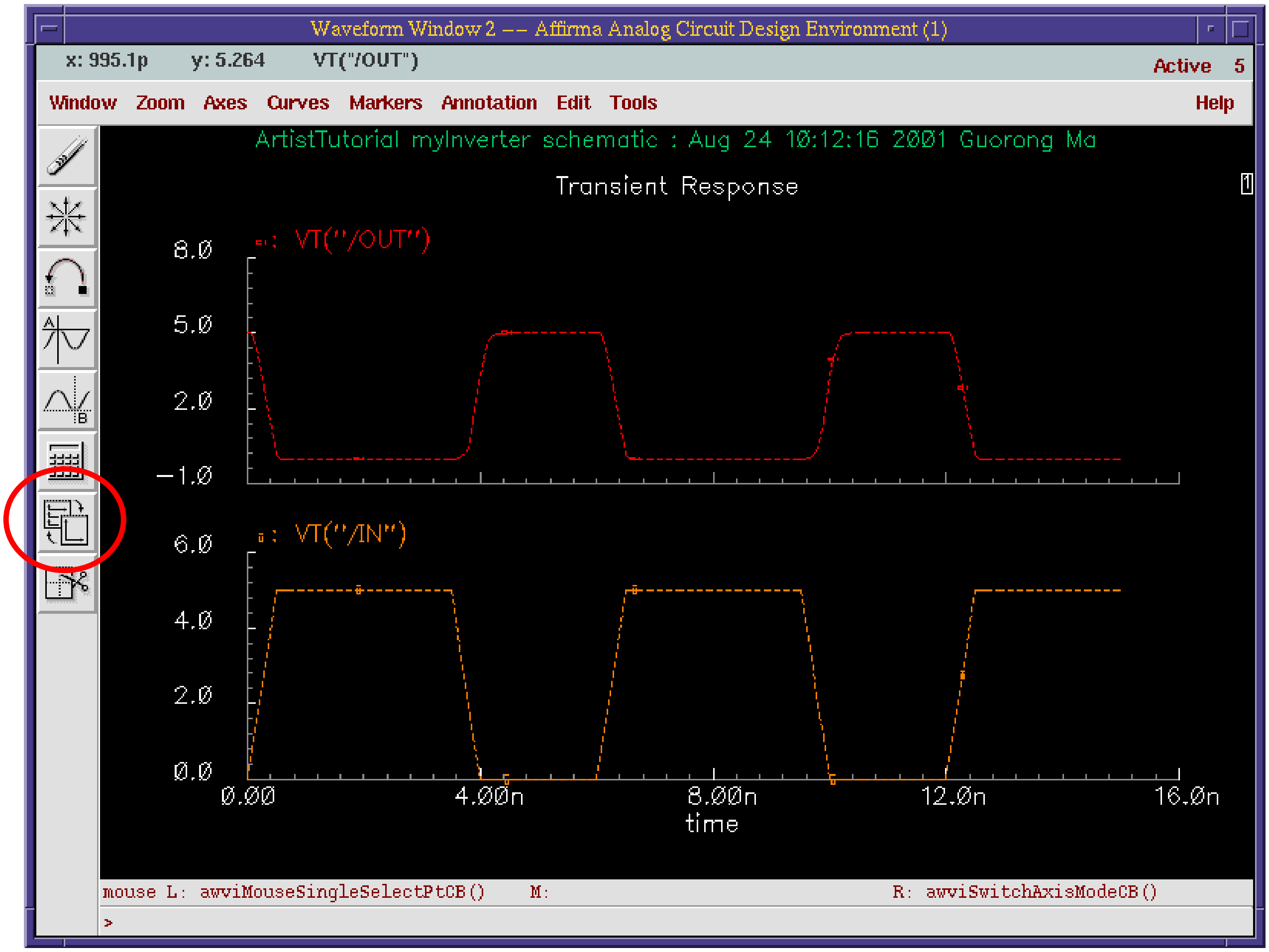
In the **Schematic Window**,
    Click on the IN wire and then **Click on the OUT wire**
Press **ESC** on your keyboard

The two curves (IN and OUT) will then be displayed in this window:



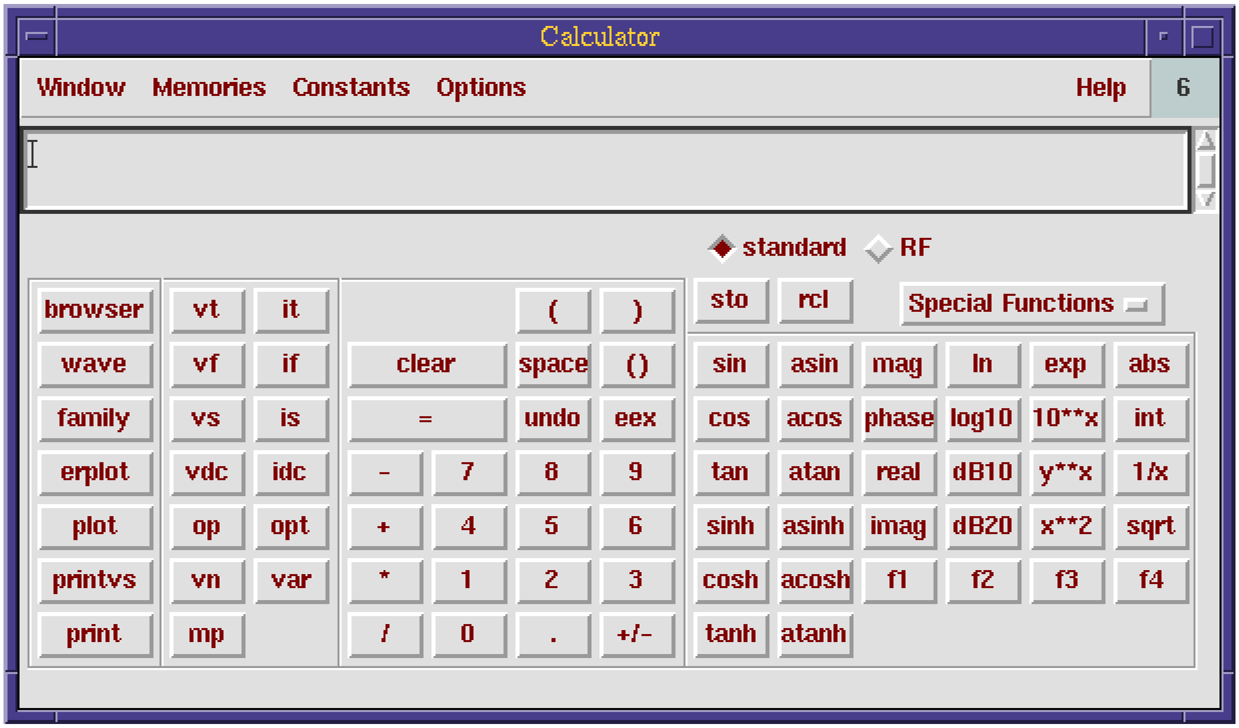
Press the **Switch Axis Mode** icon (circled in Red) on the left side of the **Waveform Window**

The waveforms will then be displayed separately as shown below:



7. Use Calculator

In **Artist Window**, go to **Tools -> Calculator**.
The **Calculator Window** will then pop up, as shown below:



In **Calculator Window**, go to **Options -> Set Algebraic**

We are going to use the calculator to plot both the current through the capacitor and the absolute value of the capacitor current.

In **Waveform Window**, select **Window -> Reset** to clear the input and output plots from the window.
In the **Calculator Window**, click on the **it** button (3rd column of buttons on the top).
In the **Schematic Window**, click on the lower terminal of the capacitor.
Returning to the **Calculator Window**, the text area at the top should like this:

In the **Calculator Window**, press the `plot` button to plot this waveform in the **Waveform Window.**

In the **Waveform Window**, press the `Add Subwindow` button (bottom button on left).

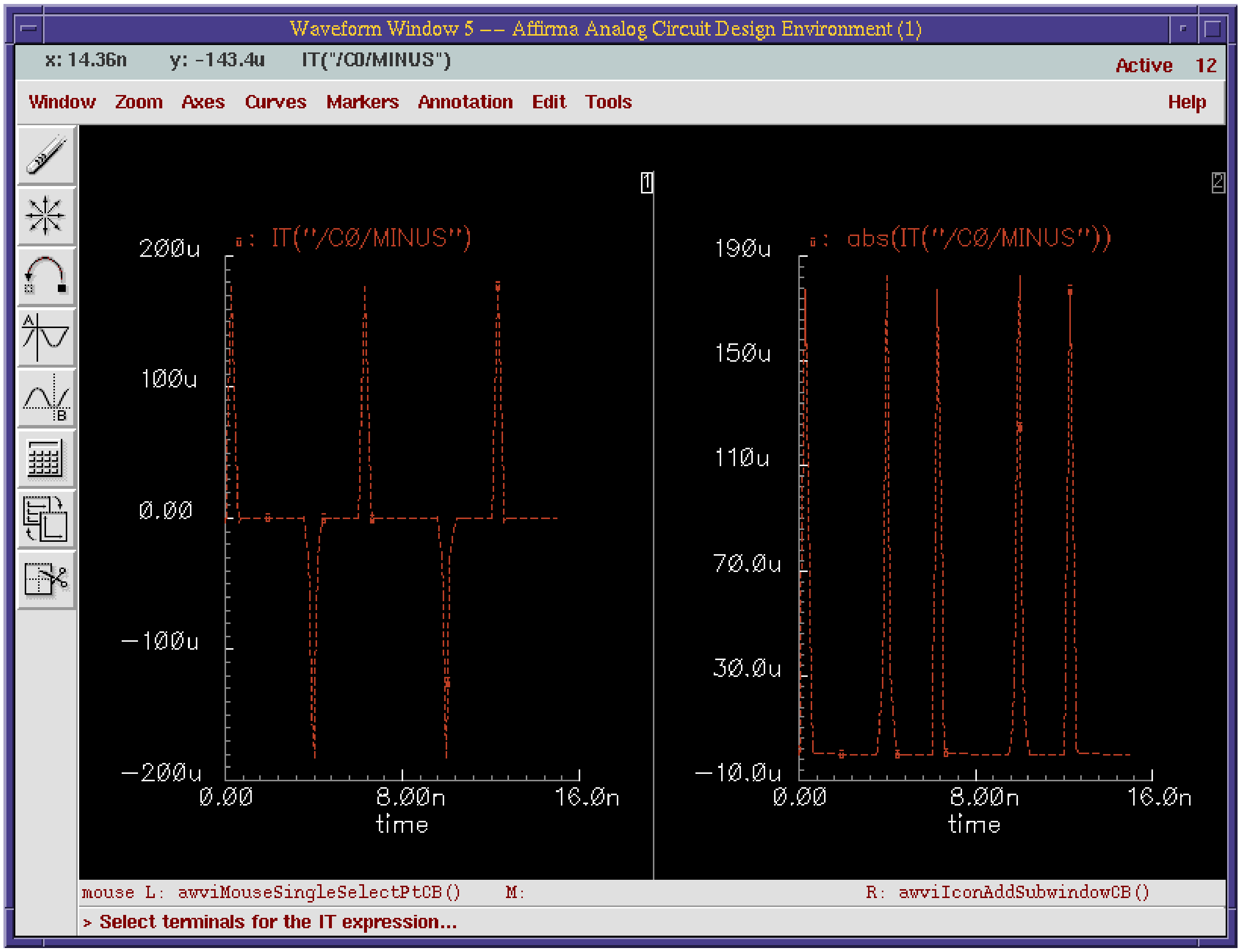
In the **Calculator Window**, press the `clear` button (4th Column, top) to erase the text area, press the `abs` button (last column, top), and press the `it` button.

In the **Schematic Window**, click on the lower terminal of the capacitor.

Returning to the **Calculator Window**, the text area at the top should like this:

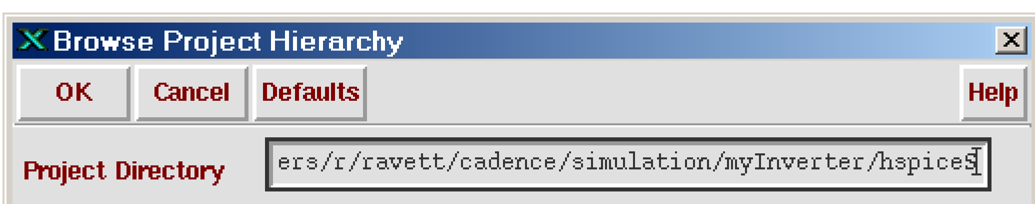
In the **Calculator Window**, press the `plot` button to plot this waveform in the **Waveform Window.**

Your **Waveform Window** should now look like this:

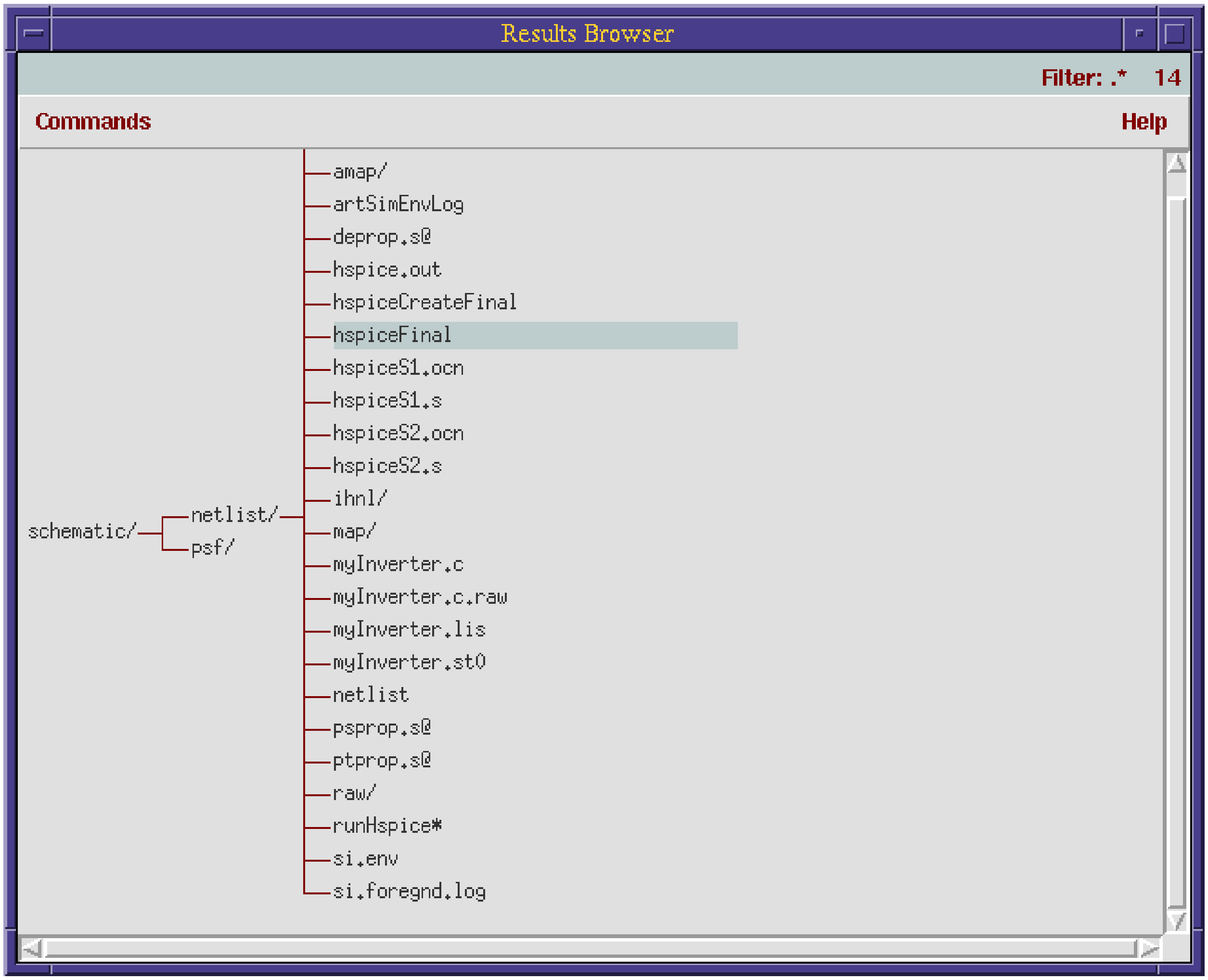


8. Use Results Browser

In **Artist Window** menu, select **Tools -> Result Browser**
In the pop-up window that appears, click **OK**



The **Results Browser Window** will then be displayed



In **Results Browser Window**, click `netlist/` and then click `hspiceFinal`

A text window will then show the hspice netlist file for your circuit.

/afs/unity.ncsu.edu/users/g/gma2/cadence/simulation/myInverter/hspiceS/schematic/netlist/hspiceFinal

File Help 16

```
* # FILE NAME: /AFS/UNITY.NCSU.EDU/USERS/G/GMA2/CADENCE/SIMULATION/
* myInverter/hspiceS/schematic/netlist/myInverter.c.raw
* Netlist output for hspiceS.
* Generated on Aug 24 10:12:22 2001
* global net definitions
.GLOBAL VDD!
* File name: ArtistTutorial_myInverter_schematic.S.
* Subcircuit for cell: myInverter.
* Generated for: hspiceS.
* Generated on Aug 24 10:12:22 2001.
V1 IN 0  PULSE 0.0 5.0 0.0 500E-12 500E-12 3E-9 6E-9
V0 VDD! 0  5.0
M1 OUT IN 0 0  TSMC25N  L=300E-9 W=450E-9 AD=337.5E-15 AS=337.5E-15 PD=2.4E-6
+PS=2.4E-6 M=1
M0 OUT IN VDD! VDD!  TSMC25P  L=300E-9 W=450E-9 AD=337.5E-15 AS=337.5E-15
+PD=2.4E-6 PS=2.4E-6 M=1
.lib "/ncsu/cadence/local/models/hspice/tsmc25/logic025.l" TT
.lib "/ncsu/cadence/local/models/hspice/tsmc25/logic025.l" PMOS
.lib "/ncsu/cadence/local/models/hspice/tsmc25/logic025.l" TT
.lib "/ncsu/cadence/local/models/hspice/tsmc25/logic025.l" NMOS
* Include files
* End of Netlist
C0 OUT 0  +1.00000000E-14 M=1.0
.PROBE TRAN
+ I(C0)
.TRAN  1.00000E-10 1.50000E-08 START=      0.
.TEMP    25.0000
.OP
.save
.OPTION  INGOLD=2 ARTIST=2 PSF=2
+        PROBE=0
```

This is the end of the tutorial. On the last few pages we've added an extra section on using a PWL (piece wise linear) voltage source instead of a pulse source, for your edification. Our thanks go to Guorong Ma (gma2@unity.ncsu.edu) for writing the original version of this tutorial, which we have edited to bring to you. If there are any questions, please email either one of us:

ravett@eos.ncsu.edu
mwbaker@eos.ncsu.edu

Thanks,

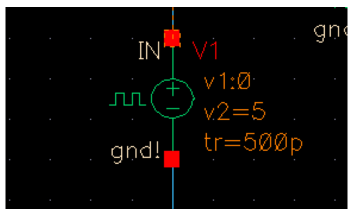
Ryan and Matt – Everyone's favorite ECE 746 TA's

Appendix:

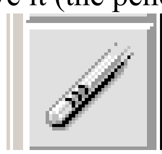
9. Using PWL voltage sources.

Assuming you have gone through the previous tutorial and have successfully built your inverter, we will now show you how to use a PWL voltage source instead of the pulse source that the tutorial source. A PWL voltage source is a source whose output voltage is dependant on a list of time and voltage pairs that is set by the designer. This list defines what the output voltage should be at the given times, with the voltage being linearly interpolated between these points. This allows a designer to simulate things like digital input streams.

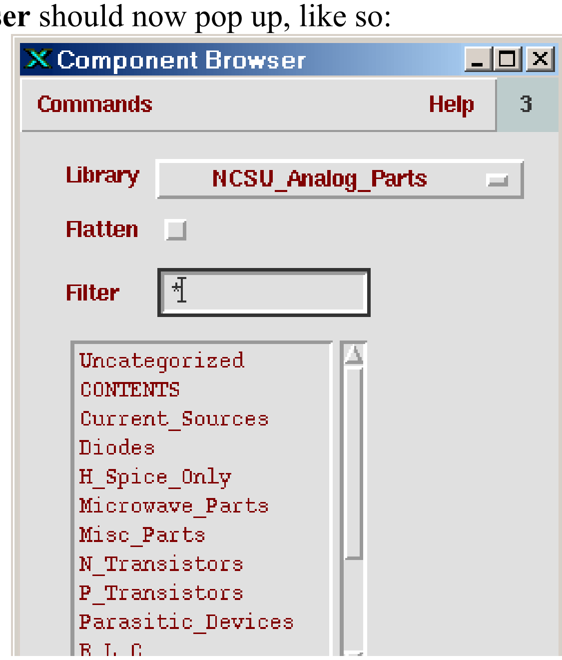
First, we must remove the old pulse source:
In the **Schematic Window**, click on the pulse source object



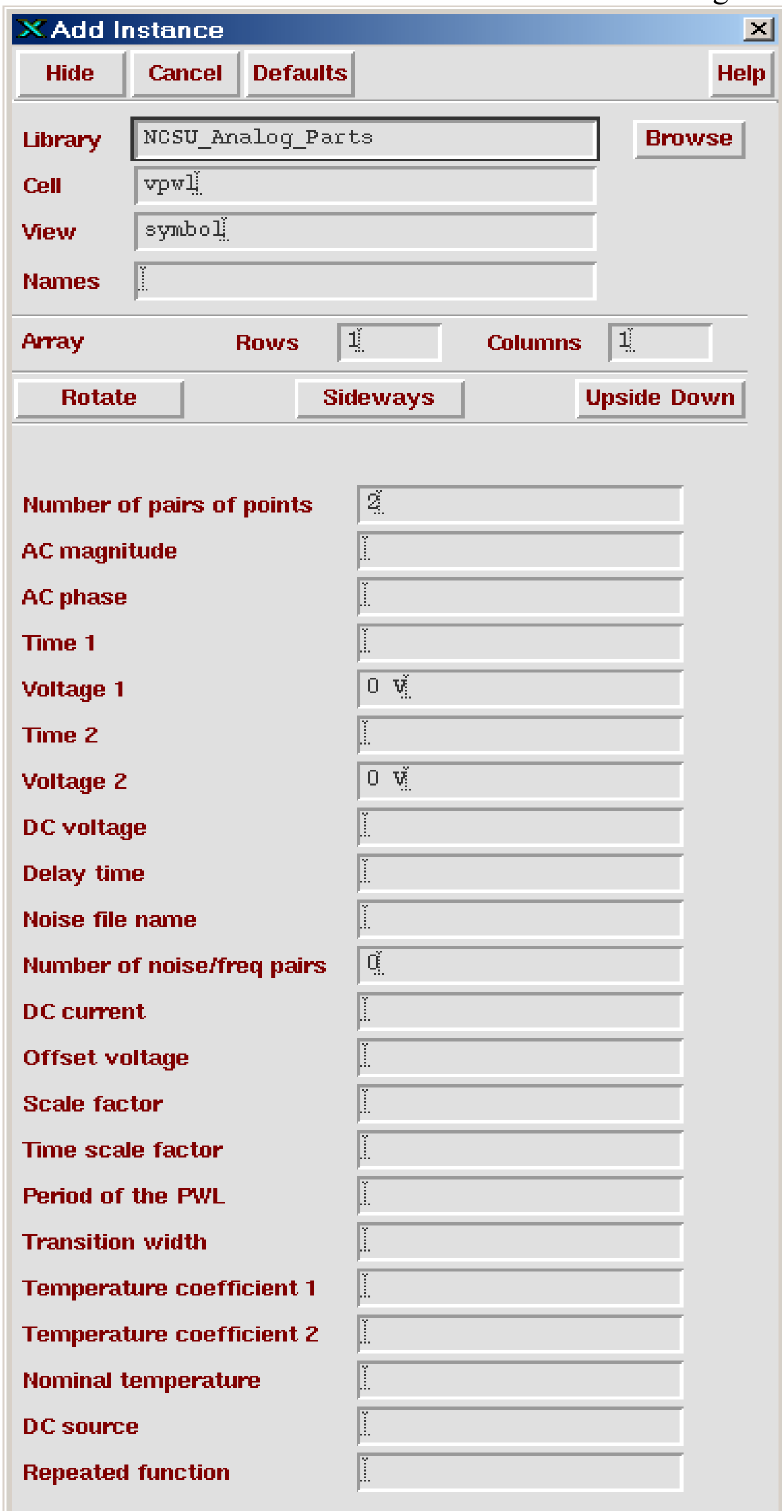
Then click on the delete button to remove it (the pencil eraser icon)



Now from the **Schematic Window** menu, select **Add -> Instance…**
The **Component Browser** should now pop up, like so:



In **Component Browser**, select `Voltage_Sources` and then `vpwl`.
The **Add Instance Window** should now look something like this:



While this option list looks very intimidating, we are really only concerned with a few of these many options.

The most important parts of this list are the “`Number of pairs of points`”, which specifies how many (time, voltage) pairs you will be defining for this source, and the “`Time X`” and “`Voltage X`” entries where you actually define the point list.

For this tutorial we will do a simple 10-point list:

In the **Add Instance Window**, fill in the “`Number of pairs of points`” entry box with “`10`”.

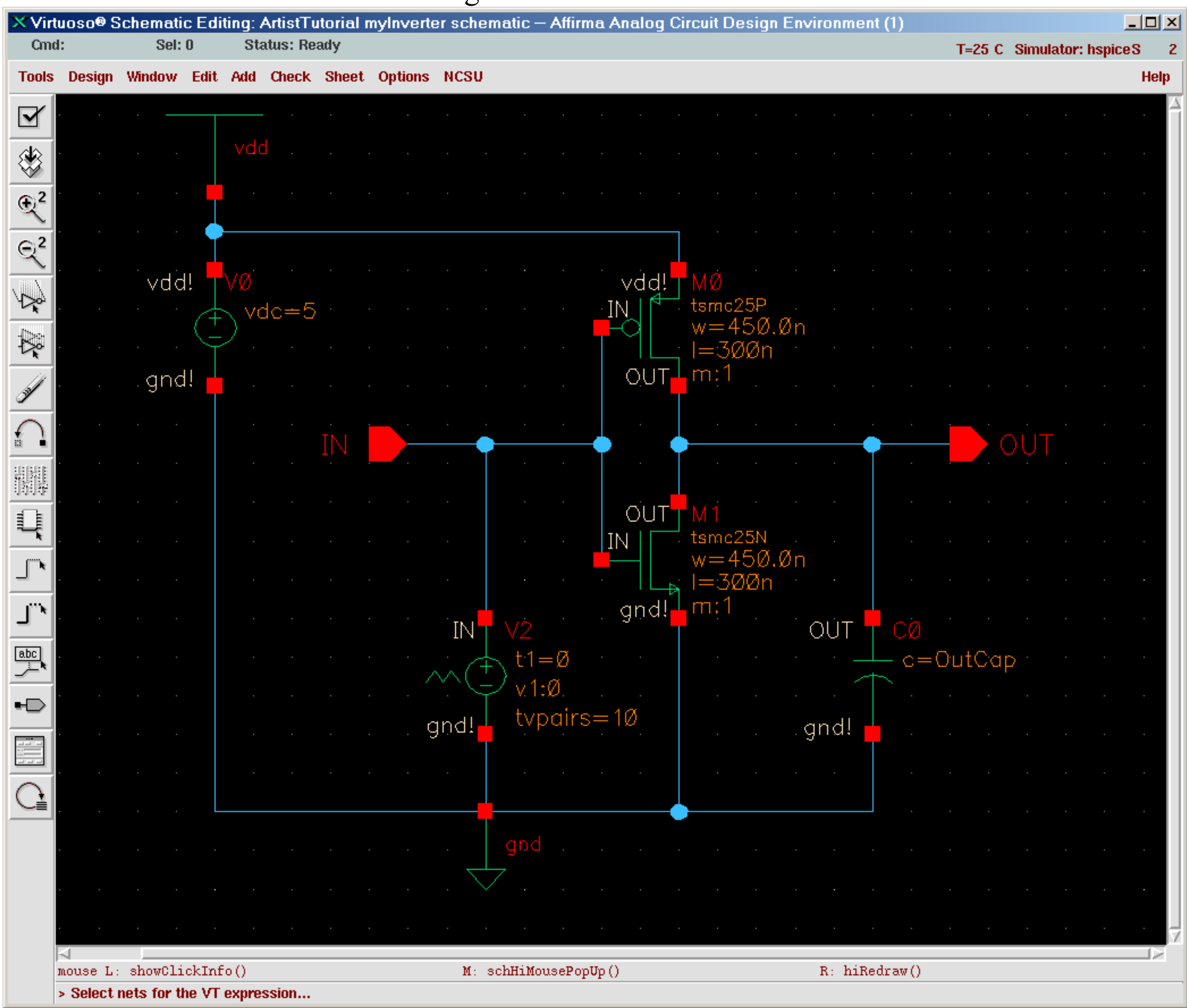
When the **Add Instance Window** finishes updating itself, fill in the time and voltage boxes with the following:

CDF Parameter	Value	Display
Number of pairs of points	10	off
AC magnitude		off
AC phase		off
Time 1	0 s	off
Voltage 1	0 V	off
Time 2	5n s	off
Voltage 2	0 V	off
Time 3	5.5n s	off
Voltage 3	5 V	off
Time 4	10n s	off
Voltage 4	5 V	off
Time 5	10.5n s	off
Voltage 5	0 V	off
Time 6	20n s	off
Voltage 6	0 V	off
Time 7	20.5n s	off
Voltage 7	5 V	off
Time 8	25n s	off
Voltage 8	5 V	off
Time 9	25.5n s	off
Voltage 9	0 V	off
Time 10	30n s	off
Voltage 10	0 V	off

In the **Schematic Window**, add the source instance in the vacant spot left from where we removed the pulse source.

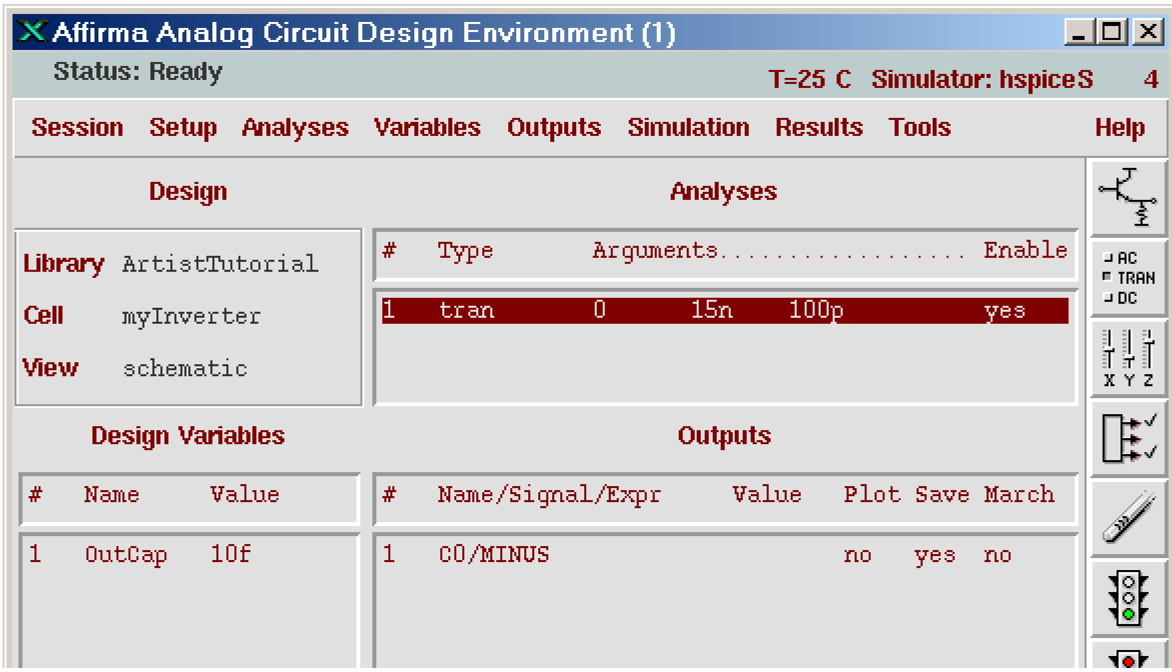
In the **Schematic Window**, click the Check and Save button, and fix any errors it highlights.

Your schematic should look something like this:

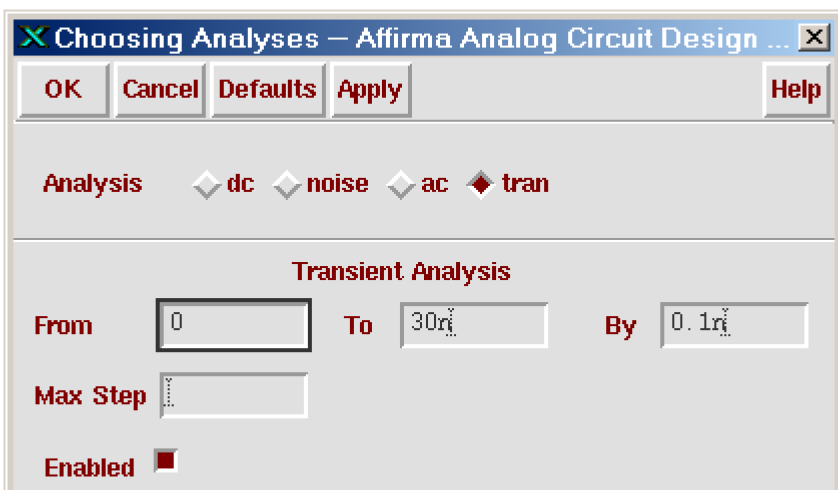


Now we need to test our new circuit to see the PWL source in action.

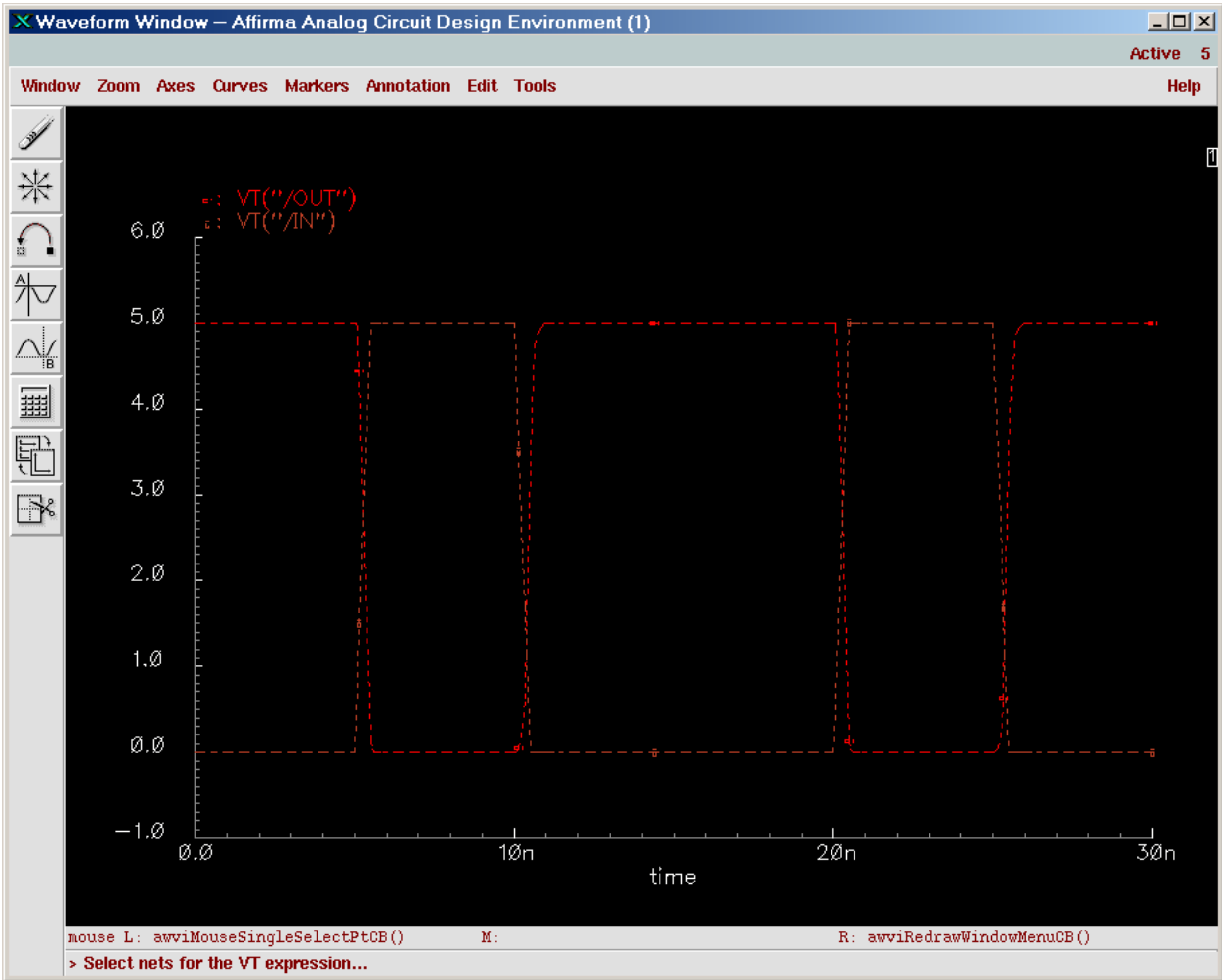
In **Analog Artist Window**, double-click on the entry highlighted below, which we set during the tutorial.



In the window that pops up, change the transient analysis so that it runs for 30 ns, like shown here:



Now, we can run the simulation just like we did in the tutorial. The plot in the **Waveform Window** should look like this:



Congratulations! You've just used a PWL voltage source.