A High-Performance CMOS 70-MHz Palette/DAC

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Introduction

• **Palette**: It is a combination of dual-ported RAM’s and three high-speed 8-bit DAC’s.

• The main application of palette is done in raster-scan graphic systems in CAD/CAM and in digital and high-definition television.

• The resolution of DAC’s makes it possible to produce over 16-million colors.

• The major limitations to DAC’s performance are threshold mismatch, variations between current-source cell, supply line resistance and power supply noise.

• In this paper author has implemented some modification to overcome these problems in DAC.
Fig. 1. Typical graphics system.
Palette/DAC Overview

• A medium-resolution monitor will have 640 horizontal by 350 vertical pixels for a total of 224000 pixels.
• For Black-White screen pixels will on or off so it would take a frame buffer of 224000 bits. But for color graphics a minimal system needs three bits per pixel (Each for red, green, blue).
• To produce more color more bit required. Typically for 16-million colors minimum 8 bit per color require. So total memory would require a 224000*24 bit or 672000 byte.
• Main function of Palette is to reduce the frame buffer memory requirement.
Functionality of Palette

- Basically Palette acts as a look-up table. The colors to be displayed on the screen are stored in the Palette by the system microprocessor; in this case 8 bit or 24 bit total per pixel.

- The data in the frame buffer choose which color from palette will be send for each pixel. The palette in this chip has 256 24-bit locations.

- The location of each pixel’s colour in the palette is stored in the frame buffer; therefore, there are 8 bits per pixel in the frame buffer. The 8 bits lookup the 24 bits that represent the colour to be sent to the screen.

- Using a palette reduces the frame buffer memory requirements from 672000 bytes down to 224000 bytes while maintaining 24 bits of colour information for each pixel.
Fig. 2. Simplified block diagram of the palette/DAC.
Architecture of Palette

• Pipeline resistors (PLR’s) are used to shorten the cycle time of the palette.

• The Digital signals to DAC’s come from three sources from RAM (circle path), 8-bit bypass source (triangle path), and a 16-bit source (triangle and square path). The data paths that do not flow through the palette are called bypass modes.

• In the bypass mode, the pixel data come directly from the frame buffers. The 8-bit bypass mode requires an 8-bit frame buffer. Each DAC receives the same 8 bits thereby producing 256 shades of grey.

• In contrast, the 16-bit bypass modes support 16-bit frame buffers. The 16 bits of data are augmented to 24 bits. With 16 bits of information, these bypass modes can produce 65536 different colours.
Fig. 4. DAC architecture.
DAC Architecture

• The DAC architecture is a 6–2 segmentation scheme.
• The palette/DAC has three 8-bit DAC’S to produce the primary colours. The architecture of one DAC is shown in Fig.
• The current-source matrix consists of 63 non-weighted current sources and two weighted ones. The LSB of the digital data controls the smallest weighted current source and the next bit controls the other weighted current source.
• The six MSB’S of the digital data decode the non-weighted current sources. The outputs of the current sources are summed to produce the final current value.
• A single cell in the DAC array is selected by row and column decoder signals. Current sources of a partially enabled row (row X+2) are selected by row and column signals as Shown in Fig.
• All rows that precede row X + 2 must be enabled. The last-row signal overrides the column decode signal for all preceding rows.
• PLR’s are located between the decoder logic and the current cells to equalize current switch transition times which removes glitches from the DAC output. The signals SW’ and SW- are well balanced for even switching.
Fig. 5. Reference current overview.
Reference current Distribution Scheme

• This scheme of busing a gate-to source voltage to the current sources is limited by
  1) threshold-voltage mismatch, 2) ground-line noise, and 3) ground-line resistance.

• The current in the current source cell as set by the bias voltage \( V_{\text{bias}} \) determined by the following equation:
  \[ I = K'(V_{\text{bias}} - V_{\text{gnd}} - V_{\text{th}})^2 \]
  where \( K' \) is the gain factor of an MOS device.

• Due to inherent mismatches in threshold voltages of the MOS devices forming the DAC current cells and noise on the internal ground buses at such high frequencies of operation, the reference voltage \( V_{\text{bias}} \), must be high enough to reduce the current mismatches in each cell to design tolerances.

• To overcome these limitations, a novel reference current distribution scheme was used.

• An overview of the scheme used in this chip is shown in Fig. 5. Three master currents are generated, one for each DAC. Current-to-voltage (I–V) and voltage-to-current (V–I) converters are used to accurately replicate the master current as local reference currents for each row of current source cells. The last step is to mirror the local reference current in each individual current source cell.
Fig. 6. Master current generation.
Master Current Generation

- The master current is set by the output of a bandgap voltage reference generator. The circuitry is shown in Fig. 6.
- The bandgap voltage $V_{bg}$ sets the appropriate gate bias of M1 to produce the current $I_{bg} = V_{bg}/R_{external}$.
- It is mirrored three times as the master currents.
- Devices M2–M9 provide bias voltages to the cascode devices. This biasing scheme keeps the current-source devices saturated and allows 4-V operation.
- Busing a current, instead of a voltage, eliminates coupling of noise from switching lines as well as ground bus potential drop across the chip.
Fig. 7. Bandgap reference generation.
Bandgap Reference generation

- The bandgap reference generator provides first-order temperature compensation. The output varies 100 ppm/°C over temperature, process, and power supply variations.
- The difference in emitter areas of Q1 and Q2 produces a voltage difference of \((kT/q) \ln(10)\) between nodes a and b.
- Nodes a and c are forced to be equal by the current mirrors formed by transistors MCo–MC7, thus generating a proportional-to-absolute-temperature (PTAT) voltage across R1. The PTAT current from R1 is mirrored in devices M10 and M11 and drawn through R2 to produce the compensation voltage.
- The bandgap voltage is referenced to Vdd and is given by
The bandgap reference circuit is stable when there is no current flowing in the current mirror devices. The circuit could remain in this state indefinitely and thereby not produce the voltage reference.

- Devices $M6-M9$ comprise a starter circuit. If $M9$ is turned off, node $d$ is pulled high through a small device $M8$. Devices $M6$ and $M7$ are turned on and start the flow of current in the mirrors.
- Once the current is established, node $d$ is pulled low by $M9$ and the starter circuit has no effect on the bandgap reference operation.

$$ V_{bg} = \frac{R_2}{R_1} \frac{kT}{q} \ln(10) + V_{be3}. $$
Slave Currents

• A master current is used to generate slave currents that are used locally in each DAC. The master current is converted to a local voltage reference in an I–V converter and the local voltage reference is used to generate slave currents in a V–I converter.
• The I–V and V–I converters are shown in Fig. 8. Empirical data show that the threshold voltages for two devices more than 300 pm apart can vary as much as 100 mV. The physical proximity of the devices in the converters reduces the threshold variation to approximately 5 mV.
• The relative error introduced by threshold variations can be seen with the following equation:

\[
\frac{I_1}{I_2} = \frac{(V_{gs} - V_{th1})^2}{(V_{gs} - V_{th2})^2}, \quad V_{gs} = 1.3 \text{ V.}
\]
DAC Current-Source Cell

• The current-source cell and the I-V converter that sets the current are shown in Fig. 9. The cascode device $M4$ increases the output impedance of the current-source cell.

• Its narrow width reduces the amount of stray capacitance on the output node which improves settling time.

• The output of the current-source cell with the cascode device is

$$Z_{out} = R_{d4}(1 - gm4* R_{d3}) + R_{d3}$$

• For this process and device sizes, the cascode device increase the output impedance of the current-source cell 141 times.

• The higher output impedance eliminates degradation of the line termination, thereby improving performance against reflections and noise.

• The increased output impedance also eliminates current-mirror inaccuracies due to fluctuations at node A.
Fig. 9. Current-source cell.

Fig. 11. Graphics-board emulator test setup.

Fig. 12. Full-scale step.
IC Implementation & Experimental Result

- The palette/DAC is implemented with a 1.2-pm, single-polysilicon, double-metal, P-well, CMOS process.
- The full-scale composite swing of the DAC is 0-1 V and it drives a 75 ohm doubly terminated line. At full scale each DAC sources 26.7 mA. The three DAC’S together consume 0.4 W.
- The digital section of the circuit has approximately 60000 transistors. To conserve power, only half of the RAM array is powered up at a time. Approximately 18000 devices switch each cycle and the average logic device gate area is 30 um2. At 70 MHz, using 170-nF/cm2 gate capacitance.
- The measured power consumption is 1.2 W. The part is packaged in a 44-pin PLCC package that has a temperature coefficient of 30°C/W. The operational temperature is 0–70° C and no heat sinks are required.
- High-speed performance was tested on a special video graphics board to emulate a real-world environment. A block diagram of the graphics board is shown in Fig. 11. A plot of the DAC output at 70 MHz is shown in Fig. 12. Characterization of the device was done on a VLSI tester based system. The results showed 0.48-LSB differential nonlinearity and an integral linearity of 0.6 LSB over process, supply, and temperature variations.
Conclusion

• A highly manufacturable, high-performance video palette/DAC has been integrated.
• A novel reference current distribution scheme was used to overcome the performance limitations of a bused reference voltage scheme.
• The current-source cell uses a cascode device to increase the DAC output impedance and to improve linearity.
• The part is fabricated on a CMOS double-metal process and can operate up to 70 MHz.
• The differential nonlinearity is 0.48 LSB and the integral nonlinearity is 0.6 LSB over process.
• Special modes have been included to bypass the palette so that the DAC’S can be driven directly.