A 12-Bit 3 GS/s Pipeline ADC With 0.4 mm$^2$ and 500 mW in 40 nm Digital CMOS

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Summarized by Kevin Phan
I. **Typical pipeline ADC**
- Offers the optimal tradeoff between conversion speed and resolution
- An n-bit quantization by cascading digitization stages
- Each stage: sampler, ADC, DAC, and amplifier
- DAC and amplifier are typically called the multiplying-DAC (MDAC)
II. A 12-bit 3GS/s Two-way time-interleaved pipeline ADC

- Time-interleaving technique to increase the conversion speed
- 2 interleaved ADCs running at half rate 1.5 GHz clk w/ opposite phases
- Each ADC uses a 2-2-2-6 architecture consisting of 3 MDAC stages and 1 6-bits flash ADC
- Taking full advantage of the maximum speed in each stage to achieve lowest power
III. Designing pipeline ADC

- Amplifiers used in SHA and MDAC stages consume the most power.
- The required minimum unity gain bandwidth $f_u$,

$$f_u = \frac{g_m}{2\pi C} = \alpha f_s$$

\(f_s\): sampling frequency
\(\alpha\): constant related to ADC resolution and stage feedback factor
\(C\): the output loading capacitance
\(g_m\): transconductance of the amplifier

$$g_m = \frac{2\eta I_D}{V_{DSAT}} = \frac{2\eta \cdot \text{Power}}{V_{DSAT} \cdot V_{DD}}$$

\(V_{DSAT}\): overdrive voltage
\(\eta\): factor of current efficiency depends on amplifier

- For high resolution pipeline ADCs, the required SNR,

$$\text{SNR} = \frac{V_s^2}{V_n^2} = \frac{V_s^2}{\lambda \frac{kT}{C}} = \frac{\beta^2 V_{DD}^2}{\lambda kT C}$$

\(V_s\): root-mean-square voltage of the signal swing
\(V_n\): total noise power
\(\beta\): voltage efficiency defined by ratio of \(V_{DD}\) and \(V_s\)
\(\lambda\): noise-excess factor, total amount of noise over the sampling noise (\(\lambda > 1\))

$$\frac{\text{Power}}{\text{SNR} \cdot f_s} = \frac{\pi \alpha \lambda kT}{\eta \beta^2} \cdot \left( \frac{V_{DSAT}}{V_{DD}} \right).$$
III. Designing pipeline ADC (Cont.)

- Keys to achieve high speed and high resolution: 2.5 V supply voltage and 40 nm thin-oxide CMOS transistors for $g_m$ devices and switches.

- 2.5 V Supply
  - Use 2.5 V supply maximizes peak-to-peak differential signal swing to 1.4 V and improves the SNR by more than 6dB compared to 1 V supply, based on eq. (4)

- Thin-oxide CMOS transistors
  - Offers sufficient $g_m$ with minimum $V_{DSAT}$ and small parasitic capacitance
  - Optimal wide bandwidth and good phase margin

- Enhances the amplifier speed, stability, and SNR performance
IV. Adaptive power/ground for CMOS switch and logic

- Fig. 3 shows the amplifier structure used in SHA and MDACs
- A single-stage amplifier structure is used to achieve wide bandwidth, good phase margin, and low noise
- 2.5 V supply gives large signal swing and improves power efficiency for SNR
- Thin-oxide transistors M1 to M6 are used to achieve high $g_m$, low $V_{DSAT}$ and low parasitic capacitance for wide bandwidth and fast settling time
- Thick-oxide transistors M7 and M8 to protect thin-oxide devices from 2.5 V supply

![Fully differential amplifier diagram]

Fig. 3. Fully differential amplifier.
IV. Adaptive power/ground for CMOS switch and logic (cont.)

- Fig. 4 shows the block diagram of the SHA circuit
- The amplifier output common-mode voltage $V_{cm1}$ and input common-mode voltage $V_{cm2}$ track over process, supply voltage, and temperature (PVT) variations for optimal operating points
- The switch that turns on and off the capacitors for signal sampling and charge transfer.

![Block diagram of sample-and-hold circuit](image-url)
IV. Adaptive power/ground for CMOS switch and logic (cont.)

- Fig. 5(a), a 2.5 V supply is used and output $V_{cm1}$ is 1.25 V
- S1, S2 and S3 are thick-oxide devices to avoid breakdown issues
- Slow and become the bottleneck of the ADC speed
- From Table I, shows the performance of a thin-oxide device under 1.0 V better than thick-oxide device under 2.5 V supply
- To maximize bandwidth using a thin-oxide device w/ minimum channel length as switching device
- Thin-oxide device operating w/ 1 V supply does not comply w/ 2.5 V amplifier design due to difference of common mode voltage

Fig. 5. Common-mode voltage of amplifier and switches.
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<th>Transient analysis</th>
<th>DC analysis</th>
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<td></td>
<td>Tr (ps)</td>
<td>P (µW)</td>
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<tr>
<td>1V thin-oxide inverter</td>
<td>6</td>
<td>16</td>
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<tr>
<td>2.5V thick-oxide inverter</td>
<td>170</td>
<td>160</td>
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IV. Adaptive power/ground for CMOS switch and logic (cont.)

- Have to level-shift up the power and ground of thin-oxide switches as shown in Fig. 5(b)
- The solution uses the adaptive power/ground technique
- $V_{dd1}$ and $V_{ss1}$ are generated internally using two low dropout regulators (LDO)
- Reference voltages LDOs are level-shifted up and down with a constant 0.5 V from amplifier output $V_{cm1}$
- The ADC clock is level-shifted up through AC coupling capacitor with a DC biased voltage of $V_{cm1}$ to $V_{dd1}$ / $V_{ss1}$ domain to drive thin-oxide drivers and switches
- The same amplifier and switch topology is used in all MDACs to achieve high-speed performance

Fig. 6. Block diagram of adaptive supply/ground for CMOS switch and logic.
V. Flash ADC design using reference voltage extrapolation

- Each MDAC has a 2.5b flash ADC and the final residual is digitized using a 1.5GS/s 6b flash ADC.
- Flash ADCs must digitize 1.4 Vpp voltage swing within a fraction of 1.5GHz clk, while presenting a low input capacitance to maximize the signal bandwidth.
- To minimize the input capacitance, the 6-bit Flash ADC uses averaging to relax the input matching requirement and interpolation to reduce the number of preamplifiers.
- Averaging requires over-ranging to compensate for the boundary effect.
- A reference voltage extrapolation method is employed to generate the extra reference voltage taps using the existing taps in the reference ladder as shown Fig. 7.
- Three-input dummy preamplifiers at the edges generate the over-ranging voltages from the inner taps of the reference ladder.
- This technique overcomes problem of the averaging and interpolation techniques and maximizes the input full-scale range, leading to higher SNR.
Fig. 7 Averaging/interpolation using reference voltage extrapolation
V. **Flash ADC design using reference voltage extrapolation (cont.)**

- Fig. 8 shows a three-input folded preamplifier where the input stage and output stage are biased and optimized independently.
- PMOS M5 and M6 have large area and large $V_{DSAT}$ to minimize the effect on the preamplifier offset.
- The folded preamplifiers are used in both 2.5b Flash ADCs inside the MDACs and the 6b Flash ADC.
- Designed to operate under multiple power/ground rails.
- $V_{dd1}$ and $V_{ss1}$ are generated from the same LDOs for switches.
- The latch is operated between $V_{dd1}$ and $V_{ss1}$ to control the MDAC switches.
- For 6b Flash ADC, high-speed level shifters convert latch output down for the encoder in the 1 V digital power main.
Fig. 8 Schematic of folded preamplifier under multiple power and ground rails
Fig. 9: SNR/SNDR versus input frequency with 3.0 GS/s sampling rate
Fig. 10: INL and DNL characteristic
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