A 16Ω Audio Amplifier with 93.8 mW Peak loadPower and 1.43 quiscent power consumption

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Abstract

• A class AB audio amplifier is used to drive a 16Ω headphone speaker load.

• With the use of fully differential internal stage and with CMFB and replica biasing circuit in output stage high power efficiency is achieved.

• Multiple compensation networks have been used here so as to attain high stability in the design while driving wide range of capacitive load.

• The power supply rejection ratio exceeds 63dB over the entire audio frequency range.
Introduction
• This 3 stage Class AB headphone driver incorporates all the desired features of an integrated audio amplifier.
• Apart from the output stage the proposed architecture is fully differential due to which there is low distortion even in low bias currents.
• Three Miller compensation networks are used so as to ensure stability.
• In addition to it the proposed architecture employs negative biasing of the substrate which further reduces the total harmonic distortion.
The first two stages are fully differential amplifiers whereas the last stage is a push pull common source amplifier.

**First Stage:**
- Its implemented with fully differential folded cascode amplifier using transistors M1-M12.
- M13-M20 along with the resistors form the CMFB.
- The gain of the first stage is given as $A_{v1} = gm1.R1$; where $gm1$ is the transconductance of M(3&4).

**Second Stage:**
- The second stage is implemented with a pair of fully differential amplifier.
- This architecture is used as to have symmetric gain and pole frequencies at the output.
• The output of the pmos differential amplifier is replicated to the output stage of the nmos common source amplifier $M_N$.

• The quiescent current through $M_N$ and $M_P$ is computed as 

$$I_{BN} = \left( \frac{W}{L} \right)_{M_{39}} I_B$$

$$I_{BP} = \left( \frac{W}{L} \right)_{M_{59}} I_B$$

• The design of the nmos differential amplifier is similar but the only difference is that the value of the resistors in the CMFB is changed to half of the value of that of pmos differential amplifier.

• This is done as in the output stage the input capacitance of the pmos is twice as that of nmos. Hence the value of resistors in CMFB are halved sized so as to obtain poles for both the transistors design on the same frequency.
Output Stage

• The output stage consists of pmos and nmos common source amplifier.
• As the amount of current required to drive the load is high and also the mobility of the electrons are twice as that of holes the width of the pmos transistor is made twice as that of nmos to attain equal strength for push pull action.
• The gate of transistor $M_P$ is biased at $V_{DD} - V_{SG,58}$ by the nmos differential amplifier in the second stage.
• Similarly the gate of transistor $M_N$ is biased at $V_{SS} + V_{GS,39}$.
• Since the threshold voltages are not the same in 0.5µm process we used negative substrate bias of 1.5V so that swing at the gates of $M_P$ and $M_N$ are same, and also it reduces harmonic distortion by 8dB.
Small Signal Model and Compensation Network
• Miller Compensation is used in this design to achieve the required stability.
• From the small signal model we can see that the resistor $R_{C1}$ and capacitor $C_{C1}$ are used between the output of the final stage and inverting output terminal of the first stage.
• This network determines the dominant pole of the amplifier.
• In order to achieve the same pole frequency at the output Miller capacitor $C_{C3}$ is used at the output of the noninverting terminal of second stage pmos differential amplifier and a Miller capacitor of $2.C_{C3}$ is used at the output of non inverting terminal of the second stage nmos differential amplifier.
Poles And Zeroes

- The low frequency gain of this audio amplifier is given by
  \[ A_v = g_m1 R_1 \cdot g_m2 R_2 \cdot g_m3 R_{out} \]
- The proposed amplifier has 4 poles and two zeroes.
- From the analysis it is shown that two poles have been cancelled out by the two zeroes hence the system is a two pole system.
- The low frequency gain of the system is 51.5dB and the phase margin is 72° and the unity gain frequency of the amplifier is 1.23MHz from the analysis shown below.
## Equations of Poles and Zeros with Estimated Values

<table>
<thead>
<tr>
<th>Poles</th>
<th>Pole frequency</th>
<th>Zeros</th>
<th>Zero frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\omega_{P1}$ [ \frac{2}{gm2 \cdot R1 \cdot R2 \cdot (2 \cdot Cc2 + 2 \cdot gm3 \cdot Rout \cdot Cc1 + 3 \cdot Cc3)} ]</td>
<td>6.72 kHz</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$\omega_{P2}$ [ \frac{2 \cdot Cc2 + 2 \cdot gm3 \cdot Rout \cdot Cc1 + 3 \cdot Cc3}{Cc1 \cdot (2 \cdot gm3 \cdot Rout \cdot R2 \cdot C2 + 2 \cdot R1 \cdot Cc2 + 3 \cdot R1 \cdot Cc3)} ]</td>
<td>74.5 kHz</td>
<td>$\omega_{Z1}$ [ \frac{2}{Cc1 \cdot R1 + 2 \cdot R2 \cdot C2} ]</td>
<td>55.8 kHz</td>
</tr>
<tr>
<td>$\omega_{P3}$ [ \frac{2 \cdot gm3 \cdot Rout \cdot R2 \cdot C2 + 2 \cdot R1 \cdot Cc2 + 3 \cdot R1 \cdot Cc3}{R1 \cdot R2 \cdot C2 \cdot (6 \cdot gm3 \cdot Rout \cdot Cc3 + 4 \cdot gm3 \cdot Rout \cdot Cc2 + 2 \cdot Cc2 + 3 \cdot Cc3)} ]</td>
<td>165 kHz</td>
<td>$\omega_{Z2}$ [ \frac{1}{R2 \cdot C2} + \frac{2}{Cc1 \cdot R1} ]</td>
<td>230 kHz</td>
</tr>
<tr>
<td>$\omega_{P4}$ [ \frac{gm2 \cdot (2 \cdot gm3 \cdot Rout + 1)}{Cout \cdot Rout \cdot gm2 + 2 \cdot C2} ]</td>
<td>2.77 MHz</td>
<td>$\omega_{Z3}$ [ - \frac{gm2}{2 \cdot Cc3} ]</td>
<td>83.0 MHz</td>
</tr>
</tbody>
</table>

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**Gain**: 51.5 dB  
**UGF**: 1.23 MHz  
**Phase-margin**: 72°
Experimental Results

- Input (mV)
  - Time (μS)

- Output (mV)
  - $C_L = 5 \text{ nF}$
  - $C_L = 500 \text{ pF}$
  - $C_L = 10 \text{ pF}$
  - Time (μS)

- Magnitude (dBV)
  - Frequency (kHz)
  - THD: $-77.89 \text{ dB}$
• The measured response of the audio amplifier to a 200mV_{PP} 50 kHz square wave is shown for various capacitive loads in the above fig.
• No ringing was observed for capacitive loads from 10pF to 5nF and I_{L} swinging from -25 to 25 mA.
• The slew rate is approximately 1.2 V/µs
• The quiescent current is measured 475µA for ± 1.5 V supply voltage.
• The above fig shows the output distortion for 1kHz sinusoidal input signal.
• As shown the harmonics are internally cancelled by fully differential first and second stage.
• The higher value of second harmonic distortion is due single ended output stage.
Power Supply Rejection Ratio

- The PSRR for $V_{DD}$ and $V_{SS}$ were also measured as shown in fig.
- Over entire audio freq range the PSRR from Vdd exceeds 63dB and for Vss it exceeds 66dB. As mentioned a high PSRR is a desirable feature in integrated amplifiers.
• **Conclusion:**

• A process called figure of merit (FOM) is used to signify the overall power efficiency of the audio amplifier and is given by

\[
\text{FOM} = \frac{P_p}{P_q}
\]

• Where \( P_p \) is the peak power delivered to the load and \( P_q \) is the quiescent power of the amplifier.

• For the proposed amplifier design the value of FOM is higher than some of the other design published.

• Hence this design exhibits the highest power efficiency of any comparable design.