OVERVIEW

- Array classification
- Non volatile memory Design and Layout
  - Read-Only Memory (ROM)
    - Pseudo nMOS and NAND ROMs
    - Programmable ROMS – PROMS, EPROMs, EEPROMs and Flash
  - Serial Access Memories
    - Shift Registers and Queues
- Content-Addressable Memory
- Programmable Logic Array
- Robust Memory Design
- Summary
Read Only Memory CLASSIFICATION

- **ROMs**
  - (i) *Mask Programmed ROMs* -
    - Data is written during chip fabrication using a photo mask
  - (ii) *Fused ROMs* -
    - Data is written by blowing the fuse electrically, hence cannot be modified later

- **Programmable Read Only Memories (PROMs)**
  - Data is written after chip fabrication
  - (i) *Erasable PROMs* -
    - Complete block is erased using UV light which is penetrated through glass window
  - (ii) *Electrically Erasable PROMs* -
    - 8 bit data is erased at a time, hence slower
  - (iii) *Flash* -
    - Programmed using high electrical voltage. Erases data in blocks hence faster
(A) Read-Only Memory – Mask ROM

- **Ex: Pseudo-nMOS NOR ROM**
  - Storing Bit information
    - Presence or absence of transistor
    - Selective placement of metal contacts according to customer requirement
    - Threshold implant by making the transistor permanently OFF
  - **Pseudo-nMOS ROM**
    - Static power and large contact area

- **Ex: Active High Word lines**
2:4 ROW DECODER and ROM LAYOUT

Inverters generating A[0-1] \_bar signals

**FIGURE 12.55** Row decoder layout on tight pitch
Pseudo-nMOS NAND ROMs

- **Ex:** Active low word lines
  - NMOS on non-selected word lines are **ON**

![Diagram](image)

**FIGURE 12.58** Pseudo-nMOS NAND ROM

**FIGURE 12.59** NAND ROM array layouts
Concept of Floating Gate

- Programming – Changing the threshold voltage [Fowler Nordheim Tunneling]
- Two threshold voltage - two states ‘0’ and ‘1’

**Figure 12.57** Cross-section of floating gate nMOS transistor
Programming Floating Gate

- **STORING STATES**
  - (i) **Positive threshold** [enhancement mode]
    - Electrons accumulated near the floating gate increases the threshold voltage
  - (ii) **Negative threshold** [depletion mode]
    - Electrons leave the floating gate decreasing the threshold voltage

![Diagram](image-url)
Flash Memory

- NAND Flash

  Name coined - blocks of memory were erased all at once “in a flash” [Masuoka84]

  Flash memory based on floating gate concept

  ssl - String select

  gsl - Ground select

  Page - no. of cells on a word line

**FIGURE 12.60** NAND Flash string
Flash - Read and Program Operations

- **Program**
  
  - $0v \rightarrow \text{logic0}$
  - $8v \rightarrow \text{logic1}$

- **Read**
  
  - $-Vt \rightarrow \text{bit line discharges}$
  - $+Vt \rightarrow \text{bit line remains the same}$

**Figure 12.60** NAND Flash string
Serial Access Memories - Shift Registers

- Look for **hold timing**!
  - No Logic between the registers
  - Min delay violation
- **How to avoid?**
  - Use - buffers
- **Variant**
  - Serial In Parallel Out [SIPO]
  - Parallel In Serial Out [PISO]
Shift Register - Variant

- 64 stage [0-63] Tapped Delay Line
- Multiplexer control the delay
- Delay blocks built from 32, 16, 8, 4, 2, 1-stage shift register
- In this Example [101010] – 42 stage Delay

**FIGURE 12.64** Tapped delay line
Serial Access Memories - Queues

- Queues supports different data read and write clock and data
- **FULL** and **EMPTY** flags
- Internally maintains separate read and write pointers

**FIGURE 12.66** Queue
Queues – FIFO/LIFO

- **First In First Out [FIFO]** – Buffers Data between two asynchronous data streams
  - On **WRITE** clk – The data is written in the Queue and asserts FULL flag when no more data can be written
  - On **READ** clk – This stored data is read until EMPTY flag is asserted

- **Last In First Out [LIFO]** – Subroutine stacks
  - Single pointer for read and write
  - **WRITE** – Increments pointer if last element $\text{FULL} = 1$
  - **READ** – decrements pointer if first element $\text{EMPTY} = 1$
Content-Addressable Memory [CAM]

- Data to be retrieved is with known binary keyword than known address
- Similar to SRAM cell with addition of a matched line
- APPLICATION
  - Translational Look Aside Buffer [TLB] in microprocessor supporting virtual memory
  - cache

**FIGURE 12.67** Content-addressable memory

**FIGURE 12.68** Translation Lookaside Buffer (TLB) using CAM
10T CAM Cell

Initial condition
Match line: Precharged

Match line discharges
Programmable Logic Arrays [PLAs]

- Flexible design approach
- Regular structure for implementing combinational logic in sum-of-products (SOP) form
- AND (products)-OR (sum) structure
- Both AND plane and OR plane is programmable

Implementation

- Pseudo-nMOS PLAs
- Dynamic PLAs
PLA - Full adder implementation

AND/OR Schematic

Pseudo-nMOS Schematic

FIGURE 12.75 AND/OR representation of PLA
Robust Memory Design

- Why do we need robust design?
  - Defects make chips useless
  - Yield loss

- How can we achieve it?
- Redundancy
  - In memory chips extra rows and columns can fix bad cells
  - Extra sub arrays can replace arrays that are beyond repair

- Supplement to Redundancy
  - Error Correcting Codes [ECC]
  - ECC – XOR actual data and corrupt data to detect flip bit

- Challenge in redundancy
  - Minimize the overhead of the replacement logic
Summary

- Array designs represents basic cell in 2D which enables regular structure and hence high density and careful layout is required
- **ROM** – 1T cell with the contents wired to a constant value
- **EPROM, EEPROM FLASH** – programmable memories
  - Used – store code with high storage density
- **CAM** – similar to SRAM with look up mode to identify a particular word presented
  - Used in – Translational look aside buffers
- **PLA** – AND-OR plane implementation with design flexibility
  - Used – implementation of quick combinational logic and use with synthesis tools logic can be simplified
Reference and Questions

- **Reference** – Neil H. E. Weste and David Money Harris, “Array Subsystems,” in *CMOS VLSI DESIGN A CIRCUITS AND SYSTEMS PERSPECTIVE*, Fourth ed. MA, USA, Ch. 12, sec 12.4-12.9, pp. 527-546