ECE 426/526: Digital Integrated Circuit Design II  
Summer 2011  
Syllabus (Updated 7/6/2011)

Course Objectives:

ECE 426/526 is the second section of the undergraduate/graduate sequence courses in digital integrated circuit design in ECE department at PSU. Only current CMOS technology will be used in this course. The objectives of this class are to cover the topics shown in the Class Coverage section and apply the knowledge learned from this class to design a small CMOS digital subsystem. Several lab works including design, simulation, and layout of CMOS digital circuits by using Cadence CAD tools are assigned.

Prerequisite: ECE 425/525 Digital IC Design I.

Textbook:


References:


Instructor: Dr. David H. Chiang  
E-mail: chiang@ece.pdx.edu
Office Location: WCC 314  
Office Hour: 6:00 pm – 8:00pm, Tuesday
Class Time: Monday & Wednesday: 7:00 pm – 9:20 pm,  
Classroom: WCC 312  
Telephone: 971-722-2580 (WCC 313 Office)
Class Website: www.ece.pdx.edu/~chiang
VLSI Design Lab (UNIX): FAB 60-19,  
Intel Lab (PC and Linux): FAB 55-17

Class Coverage:

(1) Introduction Combinational Circuit Design (1.5 Weeks)
(2) Sequential Circuit Design (2.0 Weeks)
(3) Data-path Subsystems (1.0 Week)
(4) Array Subsystems (1.0 Week)
(5) Special-Purpose Subsystems (0.5 Week)
(6) Design Methodology and Tools (0.5 Week)
(7) Testing, Debugging, and Verification (0.5 Week)
(8) Other Topics Related to CMOS Digital Circuit Design (if time permitted)
Grading Policy:

(1) Undergraduate: Homework: 20 %, mid-term exam: 20 %, Labs: 30 %, final exam: 30 %.
   A (100 – 90), A- (89 – 85) B+ (84 – 80) B (79 – 75) B- (74 – 70), C+ (69 - 65), C (64 – 60),
   C- (59 – 55), D+ (54 – 50), D (49 – 45), D- (44 - 40), F (Below 40).

(2) Graduate: Homework: 15 %, mid-term exam: 20 %, Labs: 25 %, Presentation: 10 %, final exam: 30 %.
   A (100 – 90), A- (89 – 85) B+ (84 – 80) B (79 – 75) B- (74 – 70), C+ (69 - 65), C (64 – 60), C- (59 – 55)
   F (Below 55).

Laboratory Assignments:

Three to four labs will be assigned this term. All labs are done individually.

Design Tools:

(1) Cadence IC Design Tools: Schematic Capture, Spectre, and Layout Virtuoso

Midterm Exam Schedule: 7:00 pm – 9:20 pm, Wednesday, 7/13/2011
Final Exam Schedule: 7:00 pm – 9:20 pm, Wednesday, 8/17/2011

Academic Honesty Policy:

If a student is caught for cheating on an exam, the student will receive zero point for that exam.

Class Policy:

The cellular phone must be turned it off during the class. During the lecture and presentation time, please do not use personal laptop computers in the classroom. No make-up exams will be given and no late homework and labs will be accepted unless a sincere excuse has been told in advance or an accident has happened during the homework/project due days or exam days. The student who asks for submitting a late homework or having a make-up exam needs to submit a valid document to the instructor to prove the excuse or accident. New homework problems will be assigned for the late homework submission if the solutions of the homework are released before the late homework due date. Different exam problems will be given for the make-up exam. Final exam and final lab report will not be returned to students. Only a scientific or a graphical calculator can be used during the exams.

Academic Honesty Policy:

If a student is caught for cheating on an exam, the student will receive zero point for that exam.

Disability:

If you are a student with a documented disability and are registered with the Disability Resource Center (DRC), please contact the instructor at the beginning of the course to set up appropriate academic accommodation or testing services.