A 1.9GHz Single-Chip CMOS PHS Cellphone

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Outline

• Introduction
• Architecture
• Circuit Implementation
• RF Loop Back and Digital Calibration
• Measurement Results
• Conclusion
Introduction - PHS

• Personal Handy-phone System (PHS)
  – First commercially launched in Japan in 1995
  – In 2008, China had 75 million subscribers where it can be used as a cellphone or cordless phone.

• PHS System
  – TDMA/TDD – Time Domain Multiple Access/Duplexing
  – $\pi/4$ QPSK modulation with 192kHz channel bandwidth
  – Signal transmission rate of 384kb/s with symbol rate of 192kb/s
  – RF receiver operates in a frequency band from 1880.15 to 1929.65MHz with channel spacing of 300kHz
  – Supports seamless handover = Fast channel switching
Introduction - SoC

- First radio system-on-chip (SoC) that incorporates all functions of PHS cellphone
- Implements all handset functions
- Fewer external components and smaller package pin count
- Low-cost
- Smaller form factor
- 0.18um CMOS process
- DSP and calibration to compensate for analog impairment easing analog and RF circuit requirements
Architecture – Block Diagram

- 1.9GHz direct conversion RF transceiver
- $\pi/4$ shift DQPSK PHS MODEM, ARM9 CPU and memory controller
- PHS TDMA controller
- Voice-band data converter
- Audio amplifiers for microphone, headphone and speaker
- Voice subsystem
- Low dropout voltage regulator and temperature sensing circuits
Architecture – Transceiver

- Direct conversion architecture to avoid issues with low IF architecture including image rejection and unwanted mixing products
- LO signals are generated from a sigma-delta fractional-N-synthesizer

Fig. 2. Block diagram of RF transceiver.
Frequency Synthesizer

- LO are generated from a sigma-delta fractional-N synthesizer
- Key challenge in the synthesizer design is to support seamless handover between cell base stations which require fast settling time.
- Wide bandwidth is preferred for fast settling. Bandwidth vs. phase noise tradeoff.
- Traditionally, two synthesizers interleaved -> area and power cost
- LO = 3.8GHz = 2x RF frequency. LO divided by 2 locally in receiver and transmitter to generate quadrature 1.9GHz LO. Local divide-by-2 suffers less I/Q mismatch and 3.8GHz inductor has higher Q and smaller size.

Fig. 3. Sigma-delta fractional-N synthesizer.
Voltage-Controlled Oscillator

- VCO based on NMOS and PMOS cross-coupled pair with LC tank circuit.
- To ensure tuning range covers PHS band, 7-bit switchable metal-metal cap array added in parallel to tank circuit.

Fig. 4. Simplified schematic of voltage-controlled oscillator.
Receiver

- Direct conversion = No image channels and no need for image reject filter
- RF amplified with on-chip LNA, two RF variable gain stages
- LNA has a cascaded diff pair with inductive degeneration and inductive load. LNA has attenuation mode to accommodate RF input signals as large as +5dBm.
- RF var gain has discrete gain and controlled by AGC.

Fig. 6. Direct conversion receiver.
Receiver

Passive IQ mixers convert RF to quadrature baseband signals
Baseband filtered by a 2nd order Butterworth low pass filter
Quantized by sigma-delta ADCs
AGC uses ADC outputs and envelope detectors to set receiver gain.
DC offset compensated at output of mixer by a pair of offset-cancellation DACs.

Fig. 6. Direct conversion receiver.
Passive I/Q mixers use NMOS native devices to down convert RF to baseband. Common mode voltage and amplitude of the LO IQ strongly influence gain of mixer.
• Digital baseband converted to I and Q baseband currents by two 9-bit current steering DACs. High sampling freq compared to signal BW -> no LP filter needed to remove DAC spectral images.
• Active mixers convert baseband currents directly to 1.9GHz.
• RF variable gain and programmable gain power amp compensate for gain variations.
• PA output power of 4dBm is sufficient to drive an external power amp.
• Local divide-by-2 LO buffer used to generate quadrature LO signals.
• Loopback path to calibrate analog imperfections.
Power Amplifier

Fig. 9. Segmentated power amplifier output stage.
RF Loop Back and Digital Calibration

- Single chip allows digital cal techniques to overcome analog impairments and ease requirement of analog and RF circuits which improves yield and reduces power and area.
- RF loop back allow for cal of receiver baseband filter variation, receiver DC offset, I/Q mismatch for both receiver and transmitter and transmitter carrier leak.
- To calibrate receiver DC offset, loop back path and receiver input are shutoff. DC offset quantized by ADC.
- Transmitter carrier leakage is caused by DC offset in transmitter baseband. To calibrate, preset digital sequence is transmitted and looped back into the receiver. Processor computes transmit offset.
- To calibrate receiver filter BW, in-band and out-of-band single tones are applied to the transmitter DACs. Baseband transmit signals are mixed to RF, looped back to receiver, down-converted to baseband and quantized by the ADCs. Filter response is then adjusted.

Fig. 10. RF loop back and digital calibration.
Measurement Results: Frequency Synthesizer

- 23MHz channel switching transient
- Important for seamless handover to a different channel without interruption of phone quality
Measurement Results: Frequency Synthesizer

- Critical phase noise at 600kHz offset (limits receiver blocker performance) is dominated by sigma-delta quantization noise and is sensitive to loop bandwidth.
- Phase noise is measured to be −118dBc/Hz meets PHS spec.
Measurement Results: Receiver

![Graph Showing Receiver Measurements]

**Fig. 13.** Measured receiver noise figure and sensitivity.
Measurement Results: Transmitter

![Graph showing transmit spectrum and occupied bandwidth]

PHS standard requires OBW < 288kHz
OBW = Occupied BW containing 99% signal power
Measured OBW < 250kHz for all channels

Fig. 16. Transmit spectrum and occupied bandwidth.
# Performance Summary

<table>
<thead>
<tr>
<th>Power Dissipation</th>
<th></th>
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<tbody>
<tr>
<td>RF Transmitter</td>
<td>29mA</td>
</tr>
<tr>
<td>RF Receiver</td>
<td>32mA</td>
</tr>
<tr>
<td>RF Synthesizer</td>
<td>25mA</td>
</tr>
<tr>
<td>Talk Mode (1/8 duty cycle Tx &amp; Rx)</td>
<td>81mA (including audio and digital)</td>
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<tr>
<td>Standby Mode</td>
<td>1mA (including audio and digital)</td>
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<tr>
<td>Phase Noise @ 1.9GHz</td>
<td>-118dBc/Hz @ 600kHz offset</td>
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<tr>
<td>Settling time to +/- 1kHz</td>
<td>15μs</td>
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<tr>
<td>Receive Sensitivity</td>
<td>-106dBm</td>
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<tr>
<td>Receiver Noise Figure</td>
<td>3.5dB</td>
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<tr>
<td>Transmit Power (EVM compliant)</td>
<td>+4 dBm</td>
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<tr>
<td>Transmit EVM @ +1dBm</td>
<td>4% rms</td>
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<tr>
<td>Technology</td>
<td>Standard 0.18μm CMOS</td>
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<table>
<thead>
<tr>
<th>Die Size:</th>
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<tbody>
<tr>
<td>Total</td>
<td>35 mm²</td>
</tr>
<tr>
<td>Radio and Analog</td>
<td>12 mm²</td>
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| Package   | 276-pin BGA |

Figure 26.8.7: Summary of measured performance.
Die Micrograph

Figure 26.6: Chip micrograph of the single-chip PHS cellphone.
Conclusion

• Fully integrated single-chip PHS cellphone SoC implemented in 0.18um CMOS process
• Single chip integration allows for RF loop back and extensive digital calibration to ease requirements of the analog circuits.
• SoC performance meets or exceeds all PHS specs.
• This work demonstrated feasibility of a single chip radio SoCs with fully integrated RF, analog and digital.
Questions