Advanced VLSI Packaging

AN INTENSIVE THREE-DAY COURSE
JANUARY 25-27, 1988 / SUNNYVALE, CALIFORNIA

CONTINUING EDUCATION IN ENGINEERING, UNIVERSITY EXTENSION,
AND THE COLLEGE OF ENGINEERING,
University of California, Berkeley
Advanced VLSI Packaging

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MONDAY THROUGH WEDNESDAY / JANUARY 25-27, 1988 / SUNNYVALE, CALIFORNIA

Overview
This course explains the physical, design, and economic considerations at the forefront of VLSI device packaging. Although the focus is on chip-level packaging, the subject is placed in the context of board and systems issues. The emphasis is on practical applications, and a comprehensive introduction to the literature is provided.

The topics on the first day are an overview of markets and economics, package families and their relation to the hierarchy of circuits and systems, generic chip-level assembly technologies, and printed circuit board assembly processes.

The second day continues with two special topics of increasing interest in advanced chip-level VLSI assembly technology: tape-automated bonding (TAB) and flip-chip technology. Finally, automation and manufacturing issues are discussed.

The remainder of the second day and most of the third are devoted to physical aspects of assembled packaged devices, including electrical, thermal, thermomechanical, and reliability issues. The final lecture looks at future developments.

Opportunities for discussion
Opportunities for discussion with the course staff are an important part of the program. A social hour at the end of the first day provides a relaxed atmosphere to encourage interaction between participants and staff. Discussion of specific issues of interest to the participants is provided by a panel discussion on the evening of the second day. Breaks and lunches offer further opportunities for informal interaction.

Location
Sunnyvale Hilton Inn, 1250 Lakeside Dr., Sunnyvale, California

Fee
$895, including course notes and lunch and refreshments each day. Enrollment is limited and advance enrollment is required.

Who should attend
Chip-level packaging engineers with specialized interests who want to broaden their understanding of the technology
VLSI system designers who require an appreciation of the current and future state of the art of chip packaging
Engineers in associated disciplines, such as circuit design and wafer processing, who require an appreciation of how their specialties relate to packaging technology
Engineers and managers from suppliers to the electronic packaging industry who need to understand technology trends

Program

**Monday, January 25**
7:30-8:15 am Registration / continental breakfast
8:15-8:30 Course overview / SHIRLEY
8:30-10 Markets and economics / JOHNSON
10-10:30 Break
10:30-12 Package families and assembly technologies I / GOlDA
12-1 pm Lunch
1-2:30 Package families and assembly technologies II / GOlDA
2:30-3 Break
3-4:30 Board-level assembly technology / KEAR
4:30-5:30 Social hour and discussion

**Tuesday, January 26**
8-8:30 am Continental breakfast
8:30-9:15 TAB technology / FISTER
9:15-9:30 Break
9:30-10:15 Flip-chip technology / TOTTA
10:15-10:30 Break
10:30-12 Assembly automation / KHADPE
12-1 pm Lunch
1:2-1:25 Reliability issues I / SHIRLEY
2:15-2:30 Break
2:30-3:30 Reliability issues II / SHIRLEY
3:30-3:45 Break
3:45-5:15 Thermal/thermomechanical issues I / MAHALINGAM
7-9 Panel discussion

**Wednesday, January 27**
8-8:30 am Continental breakfast
8:30-10 Thermal/thermomechanical issues II / MAHALINGAM
10:10:30 Break
10:30-12 Electrical issues I / HAMILTON
12-1 pm Lunch
1-2 Electrical issues II / HAMILTON
2-2:30 Break
2:30-4 Future trends / JOHNSON

Cover illustration: Pin-grid array. 
Drawn by Larry Pelchat, Intel Corporation.
CONTINUING EDUCATION IN ENGINEERING, UNIVERSITY EXTENSION, AND THE COLLEGE OF ENGINEERING,

University of California, Berkeley

Instructional staff
Course organizers
BARRY JOHNSON, Professor, Department of Electrical and Computer Engineering, University of Arizona, Tucson
GLENN SHIRLEY, Project Engineer, Intel Corporation, Chandler, Arizona

Lecturers
JULIUS FISTER, Manager, Product Development, Olin Corporation, New Haven, Connecticut
TOM GOIDA, Packaging and Assembly Engineer, Analog Devices Semiconductor, Wilmington, Massachusetts
DOUG HAMILTON, Professor, Department of Electrical and Computer Engineering, University of Arizona, Tucson
BARRY JOHNSON, Professor, Department of Electrical and Computer Engineering, University of Arizona, Tucson
FRED KEAR, Manager, Laboratory Support, Siemens Transmission Systems, Inc., Albuquerque, New Mexico
SUBASH KHADPE, President, Semiconductor Technology Center, Neffs, Pennsylvania
MALI MAHALINGAM, Member of Technical Staff, Motorola, Inc., Phoenix, Arizona
GLENN SHIRLEY, Project Engineer, Intel Corporation, Chandler, Arizona
PAUL TOTTA, IBM Fellow, IBM East Fishkill, Hopewell Junction, New York

Faculty adviser
HARI DHARAN, Associate Professor of Mechanical Engineering, University of California, Berkeley

Program coordinator
LINDA REID, Continuing Education in Engineering, University Extension, University of California, Berkeley

Enrollment information
Enrollment is limited and advance enrollment is required. Upon request, a place in the course will be reserved for individuals who require time to obtain authorization. To reserve a place call (415) 642-4151.

How to enroll
BY MAIL: Fill out and return the enrollment form provided.
BY PHONE: You may enroll by phone if you use Visa or MasterCard; call (415) 642-4111. Enrollments must be accompanied by the full fee or by purchase order authorization. You may pay by check or use Visa or MasterCard. Make checks payable to the UC Regents.

For efficient enrollment processing, we must have the Priority Code from this publication, whether or not it is addressed to you. This 5-digit code (3 numbers and 2 letters) appears on the mailing label above the addressee’s name. If there is no label on your copy, the code appears in a box in the middle of the address section.

Confirming your enrollment: If you enroll by mail and have not received an enrollment receipt five days prior to the scheduled date of the course, please call (415) 642-4151 to confirm that the course will convene as scheduled. Since UC Extension is self-supporting, it is necessary for us to establish a minimum enrollment. If the minimum is not met at least a week prior to the course date, the course may be canceled; if so, enrollees will be notified.

Refund policy: If you enroll and then cannot attend, a refund, less $20 processing charge, will be granted if requested before the beginning date of the course.

Further information
Housing: A group of rooms will be set aside at the Sunnyvale Hilton Inn, and reservation information will be sent to enrollees. Participants may reserve rooms in advance with the Hilton Inn reservation department, (408) 738-4888. Special rates will be available; participants in this course should identify themselves when requesting room reservations. Reservations must be made no later than December 24, 1987. After this date rooms will be available only on a space and rate availability basis.

Transportation and parking: Courtesy shuttle service is available between the hotel and the San Jose airport. Regularly scheduled commercial transportation or private limousine service is available between the hotel and the San Francisco and San Jose airports. There is ample free parking at the hotel.

If you have questions, call (415) 642-4151, or write to Continuing Education in Engineering, University Extension, University of California, 2223 Fulton St., Berkeley, CA 94720.

Forthcoming programs
This course is one of many planned for early 1988. Others include
The Berkeley Process and Device Technology Series, January-April, Palo Alto
Plasma Etching for VLSI, February 9-12, Palo Alto
MOS Devices for Advanced VLSI, February 9-12, Palo Alto
CMOS Process Integration and Engineering, February 9-12, Palo Alto
Burn-In and Reliability Testing of Semiconductors, March 2, Santa Clara
Barrier Metals for Semiconductor Fabrication, March, Sunnyvale
Polycrystalline Silicon, Metal Silicides, and CVD Metals for Integrated Circuit Applications, April 7-8, Palo Alto
Workshop on Metals and Silicides for VLSI Interconnect, May 9-12, San Juan Bautista

If you would like to receive detailed announcements of any of these courses, please telephone (415) 642-4151, or write to Continuing Education in Engineering, University Extension, University of California, 2233 Fulton St., Berkeley, CA 94720.