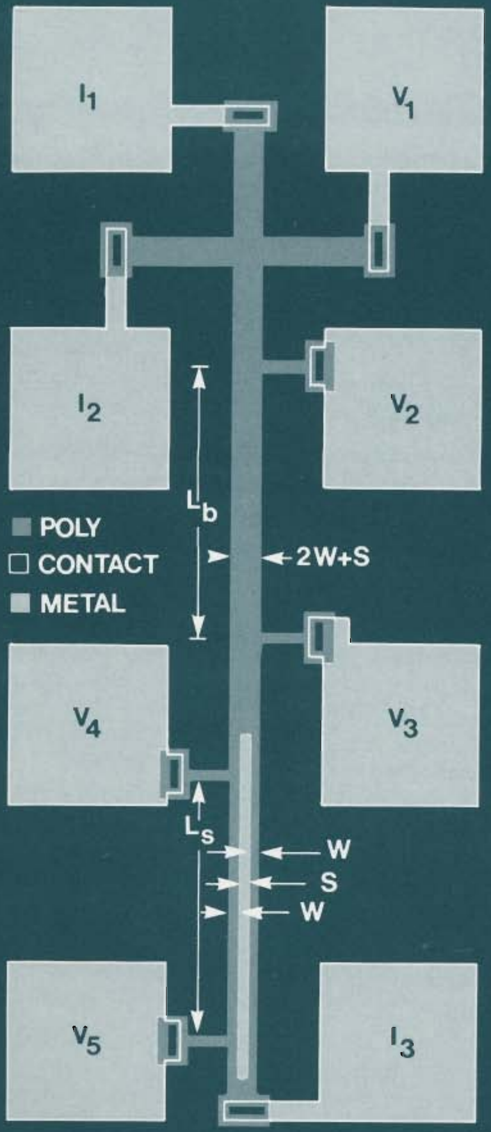
I1
V1
I2
V2
POLY
CONTACT
METAL
Lb
2W+S
V4
V3
Ls
W
S
W
V5
I3

Microelectronic Test Structures for VLSI Development and Manufacturing

An intensive two-day course
March 27-28, 1986
Palo Alto, California

Continuing Education in Engineering,
University Extension,
and the College of Engineering,
University of California, Berkeley

Microelectronic Test Structures for VLSI Development and Manufacturing

With the advent of very-large-scale integration (VLSI) and ultra-large-scale integration (ULSI), semiconductor processing, as well as packaging, is becoming increasingly complex. A process/package development/monitoring test die is used as the vehicle to move from the initial concept of a basic device to the reliable, reproducible, and economical manufacture of integrated circuits.

This course covers the issues involved in designing a microelectronic test chip. Participants will gain an in-depth understanding of how to design and utilize test structures to develop, define, or debug a new or existing VLSI process, from the basic concept of device structure to the final packaging considerations.

The course is intended for engineers, scientists, and managers interested in developing and maintaining processes and packages for VLSI devices and circuits. It will be of value to semiconductor process and packaging engineers as well as device and circuit designers.

After providing an overview of the field, the course focuses on recent techniques developed to meet the requirements of advanced processes and packages. The first day opens with a general introduction to semiconductor devices and technologies, followed by an examination of packaging considerations. Specific characterization needs, as well as the test structures required for characterization are discussed. Although the course emphasizes silicon integrated circuit applications, the treatment of the subject is useful to those working in other semiconductor fields.

The second day focuses on the design of the test chip for yield and reliability monitoring. Participants are assigned practical problems associated with design.

Time during the course is set aside for discussion and questions. Participants are encouraged to bring specific application problems that they would like to discuss.

Location: Hyatt Rickeys Hotel,
4219 El Camino Real, Palo Alto, California

Fee: $495, including course notes and refreshments and lunch each day. Enrollment is limited and advance enrollment is required. (EDP 323030)

Program

Thursday, March 27

7:45-8:15 am	Registration
8:15-8:30	**Introduction** / STRATHMAN
8:30-10	**Semiconductor technologies** / BHANDIA
10-10:30	Break
10:30-12	**Devices to circuits: performance benchmarks** / PERNER
12-1 pm	Lunch
1-3	**Device characterization** / BUEHLER
3-3:30	Break
3:30-5	**Packaging** / SHIRLEY & BOSE
5-6	Social hour

Friday, March 28

8-9 am	**Materials charcterization** / STRATHMAN
9-10	**Reliability in assembly** / SHIRLEY & BOSE
10-10:30	Break
10:30-12	**Yield monitors** / BUEHLER
12-1 pm	Lunch
1-2	**Problem sets**
2-3	**Discussion of problem sets**
3-4	**Panel discussion**

Continuing Education in Engineering,
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An intensive two-day course ■ Thursday-Friday, March 27-28, 1986 ■ Palo Alto, California

Course staff

Organizer

ALOKE BHANDIA, Staff Engineer, Hewlett-Packard Company, Santa Clara, California

Instructional staff

ALOKE BHANDIA, Staff Engineer, Hewlett-Packard Company, Santa Clara, California

SUBROTO BOSE, Reliability Engineer, Intel Corporation, Chandler, Arizona

MARTIN BUEHLER, Senior Manager, Technical Services, Jet Propulsion Laboratory, Pasadena, California

FRED PERNER, Manager, Technical Services, Hewlett-Packard Company, Palo Alto, California

GLEN SHIRLEY, Staff Reliability Engineer, Intel Corporation, Chandler, Arizona

MICHAEL STRATHMAN, Manager, RBS Services, Charles Evans & Associates, San Mateo, California

Faculty adviser

NATHAN CHEUNG, Associate Professor of Electrical Engineering and Computer Sciences, University of California, Berkeley

Industry adviser

MICHAEL STRATHMAN, Manager, RBS Services, Charles Evans & Associates, San Mateo, California

Program coordinator

LINDA REID, Continuing Education in Engineering University Extension, University of California, Berkeley

Enrollment information

Enrollment is limited and advance enrollment is required. Upon request, a place in the course will be reserved for individuals who require time to obtain authorization. To reserve a place call (415) 642-4151.

How to enroll

BY MAIL: Fill out and return the enrollment form provided.

BY PHONE: You may enroll by phone if you use Visa or MasterCard; call (415) 642-4111.

Enrollments must be accompanied by the full fee or by purchase order authorization. You may pay by check or use Visa or MasterCard. Make checks payable to the UC Regents.

For efficient processing, we must have your Priority Code, whether you enroll by phone, by mail, or in person. This 5-digit code (3 numbers and 2 letters) appears on the mailing label above the addressee's name. If there is no label on your copy, the code appears in a box in the middle of the address surface.

Confirming your enrollment: If you enroll by mail and have not received an enrollment receipt five days prior to the scheduled date of the course, please call (415) 642-4151 to confirm that the course will convene as scheduled. Since UC Extension is self-supporting, it is necessary for us to establish a minimum enrollment. If the minimum is not met at least a week prior to the course date, the course may be canceled; if so, enrollees will be notified.

Refund policy: If you enroll and then cannot attend, a refund, less $20 processing charge, will be granted if requested before the beginning date of the course.

Further information

Housing: A group of rooms will be set aside at the Hyatt Rickeys Hotel, and reservation information will be sent to enrollees. Participants may reserve rooms in advance with Hyatt Rickeys reservation department, (415) 493-8000. Special rates will be available; participants in this course should so identify themselves when requesting room reservations. Reservations must be made no later than February 26, 1986.

Transportation and parking: Regularly scheduled commercial transportation or private limousine service is available between the hotel and the San Francisco and San Jose airports. There is ample free parking at the hotel.

If you have questions, call (415) 642-4151, or write to Continuing Education in Engineering, University Extension, University of California, 2223 Fulton St., Berkeley, CA 94720.

Forthcoming programs

MOS Analog/Digital Interface Circuit Design for VLSI Digital Systems, January 13-15, 1986, San Francisco Airport

C Language Programming—An Intensive Course, February 13-15, 1986, Berkerley

The C Programming Language—An Introduction, February 20-21, 1986, San Francisco

Composite Materials Workshop, February 24-28, 1986, Berkeley

Workshop on Lisp, March 7-8, 1986, San Francisco

High-Resolution Lithography, March 9, 1986, Santa Clara

UNIX Shell Programming, April 17-19, 1986, Berkeley

Design and Application of Industrial Security Systems, May 6-8, 1986, Berkeley

Workshop on Refractory Metals and Silicides for VLSI IV, May 12-15, 1986, San Juan Bautista

III-V Semiconductor Materials & Devices, June 1986, Palo Alto

Telecommunications Signal Processing and ICs, June 1986, Palo Alto

Materials Characterization Techniques for Integrated Circuit Processing, June 16-19, Palo Alto

6th International Conference on Ion Implantation Technology, July 28-August 1, 1986, Berkeley

Packaging, August 1986, Palo Alto

Barrier Metals, August 1986, Palo Alto

Computer Security Technology, Summer 1986, Berkeley

International Conference on Semiconductor and Integrated Circuit Technology, October 19-26, 1986, Beijing, China

Design and Application of Industrial Security Sytems, December 2-4, 1986, Berkeley

If you would like to receive detailed announcements of any of these programs, please telephone (415) 642-4151, or write to Continuing Education in Engineering, University Extension, University of California, 2223 Fulton St., Berkeley, CA 94720.

Cover illustration: Split cross bridge resistor, courtesy Martin Buehler, Jet Propulsion Laboratory

APPLICATION OF TEST CHIPS IN PACKAGING AND ASSEMBLY

C. G. SHIRLEY, S. BOSE, R. C. BLISH II

INTEL CORPORATION
COMPONENTS ASSEMBLY/TEST
145 SOUTH 79TH ST.
CHANDLER, ARIZONA 85224

1. INTRODUCTION
2. OVERVIEW OF PACKAGING AND ASSEMBLY
3. DATA ANALYSIS SOFTWARE
4. SENSOR DESIGN
5. DESIGN GUIDELINES
6. CASE STUDIES
7. DESIGN SOLUTIONS
8. BIBLIOGRAPHY

1. INTRODUCTION

o WHAT IS AN "ASSEMBLY" TEST CHIP?

- IT SIMULATES THE MATERIALS AND PROCESSING OF REAL CHIPS, BUT NOT THE LOGICAL FUNCTION.
- IT GIVES ELECTRICAL READOUTS OF CONDITIONS, PAST AND PRESENT, INSIDE THE PACKAGE.

o TRADITIONALLY ASSEMBLY-RELATED TEST CHIPS HAVE BEEN

- USED TO MEASURE PACKAGE PARAMETERS SUCH AS STRESS, THERMAL IMPEDANCE, AND HUMIDITY.
- USED TO CHARACTERIZE A FEW TENS OF HAND-ASSEMBLED PIECES.
- ASSEMBLED BY A SKILLED PERSON.
- MEASURED USING DESKTOP INSTRUMENTS.

1. INTRODUCTION (CONTINUED)

o TO APPLY TEST CHIPS IN A MANUFACTURING ENVIRONMENT WE ADD THE FOLLOWING OBJECTIVES:

- USE THE TEST CHIPS TO CHARACTERIZE AND QUALIFY NEW WAFER AND ASSEMBLY PROCESSES.
- EXPERIMENTS WILL INVOLVE HUNDREDS OF PIECES TO GIVE A STATISTICAL CHARACTERIZATION OF PROCESSES.
- FACTORY (UNSKILLED) ASSEMBLY SHOULD BE EASY. DESIGN RULES SHOULD BE FOLLOWED.
- USE AN AUTOMATIC PARAMETRIC TESTER WITH SOFTWARE-CONTROLLED SWITCHING MATRIX.
- BUILD A QUALITY AND RELIABILITY DATA BASE BASED ON A FEW WELL-CHARACTERIZED SENSORS.

o BENEFITS OF THIS NEW ORIENTATION:

- ELIMINATES BOTTLENECKS IN THE SUPPLY OF NEW CHIPS.
- ELIMINATES BOTTLENECKS IN ACCESS TO TESTERS.
- CAN BUILD A DATA BASE FOUNDED ON A WELL-UNDERSTOOD SET OF SENSORS.
- CREATES A COMMON REFERENCE TO AID COMMUNICATION BETWEEN THE WAFER PROCESSING WORLD AND THE ASSEMBLY WORLD. DOES NOT INVOLVE PRODUCT DESIGNERS.

2. OVERVIEW OF PACKAGING AND ASSEMBLY

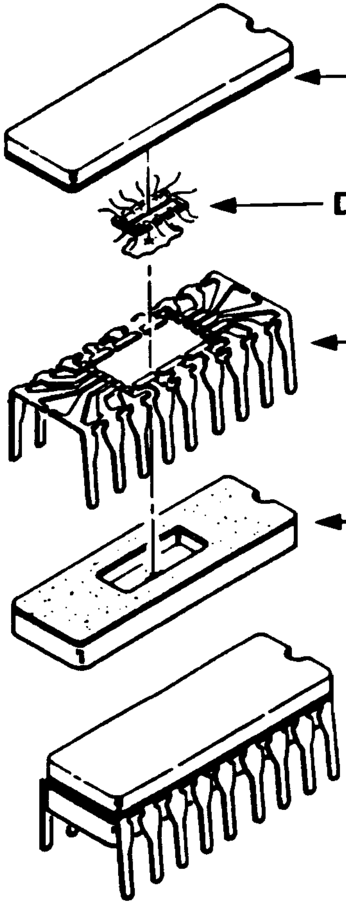
- PACKAGE FAMILIES AND TECHNOLOGIES
- ASSEMBLY PROCESS FLOW
- PACKAGE TESTING
- ASSEMBLY DEFECTS AND RELIABILITY JEOPARDIES

REFERENCE: INTEL QUALITY/RELIABILITY HANDBOOK (ORDER NUMBER 210997-001) INTEL LITERATURE DEPARTMENT, 3065 BOWERS AVE., SANTA CLARA, CA 95051, (800)538-1876, OR (800)672-1833 (CA ONLY). PRICE $15.

PACKAGE FAMILIES AND TECHNOLOGIES

	FAMILY AND LEAD COUNT		
TECHNOLOGY	DUAL-IN-LINE	CHIP CARRIER	PIN-GRID ARRAY
PRESSED CERAMIC "CERDIP"	YES, 16-40	NO	NO
LAMINATED CERAMIC "CERAMIC"	YES, 16-48	YES, 18-68	YES, 68-132
PLASTIC	YES, 16-48	YES, 18-68	UNDER DEVELPT

PRESSED CERAMIC PACKAGE



TOP WITH GLASS

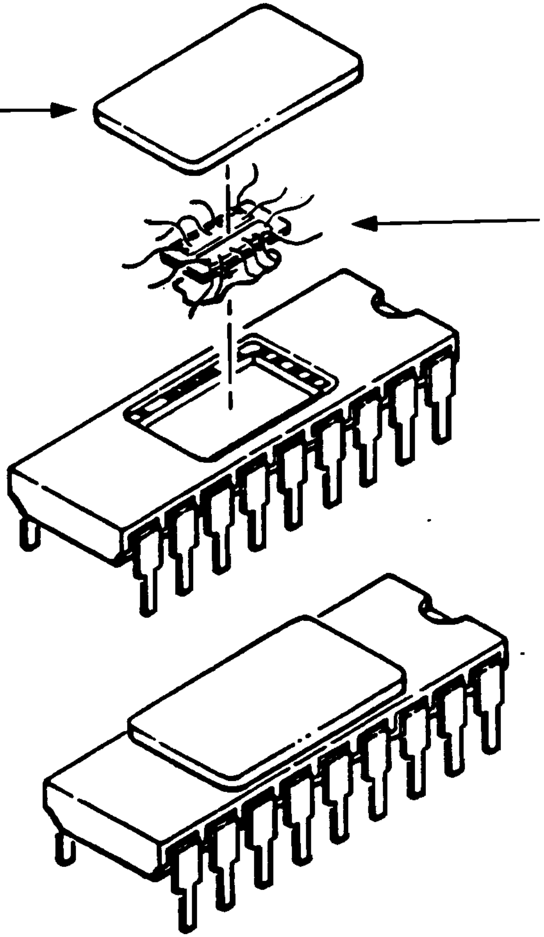
DIE (WIRE BOND AFTER DIE ATTACH)

LEAD FRAME

BASE WITH GLASS

FULLY ASSEMBLED

LAMINATED CERAMIC PACKAGE



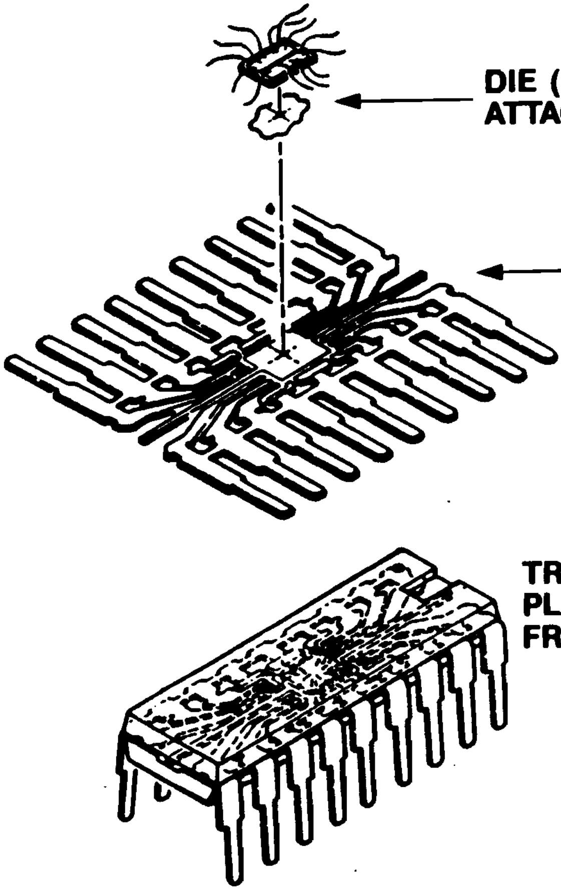
LID

DIE (WIRE
BOND AFTER
DIE ATTACH)

SIDEBRAZE
PACKAGE

ASSEMBLED

PLASTIC PACKAGE

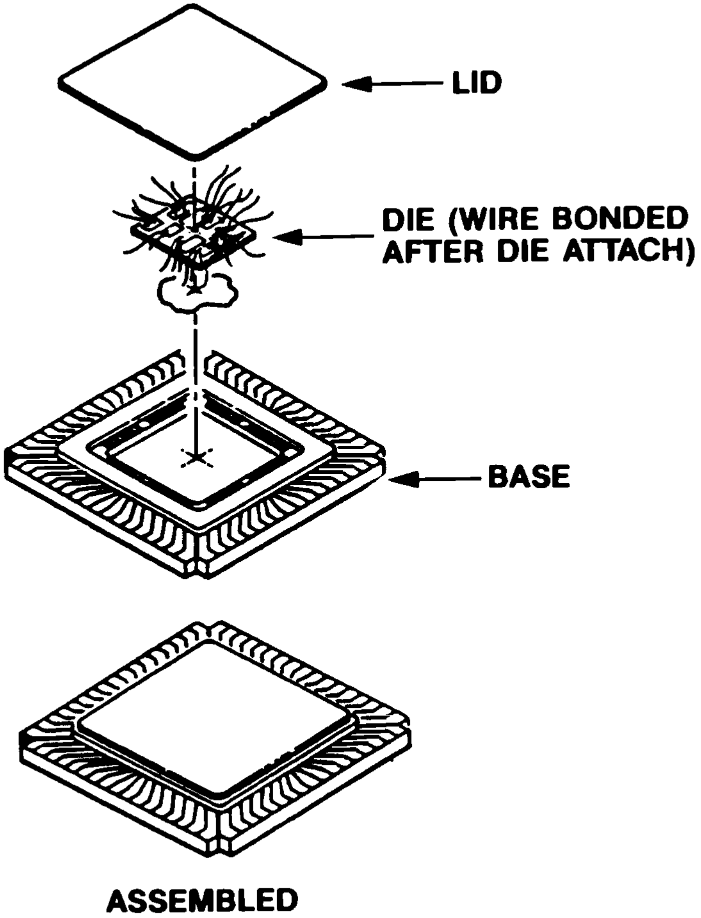


DIE (BONDED AFTER DIE ATTACH) ADHESIVE

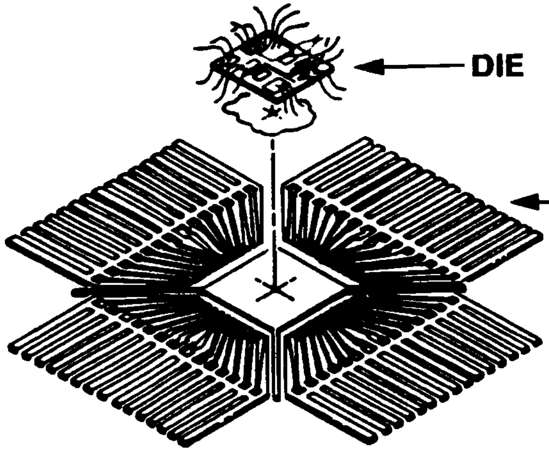
LEAD FRAME

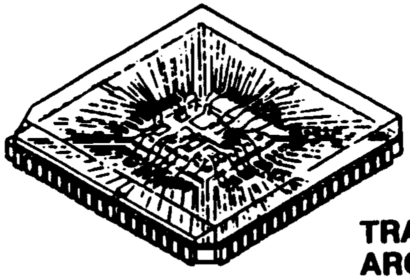
TRANSFER MOLD PLASTIC AROUND FRAME AND DIE

CERAMIC CHIP CARRIER


LID
DIE (WIRE BONDED AFTER DIE ATTACH)
BASE
ASSEMBLED

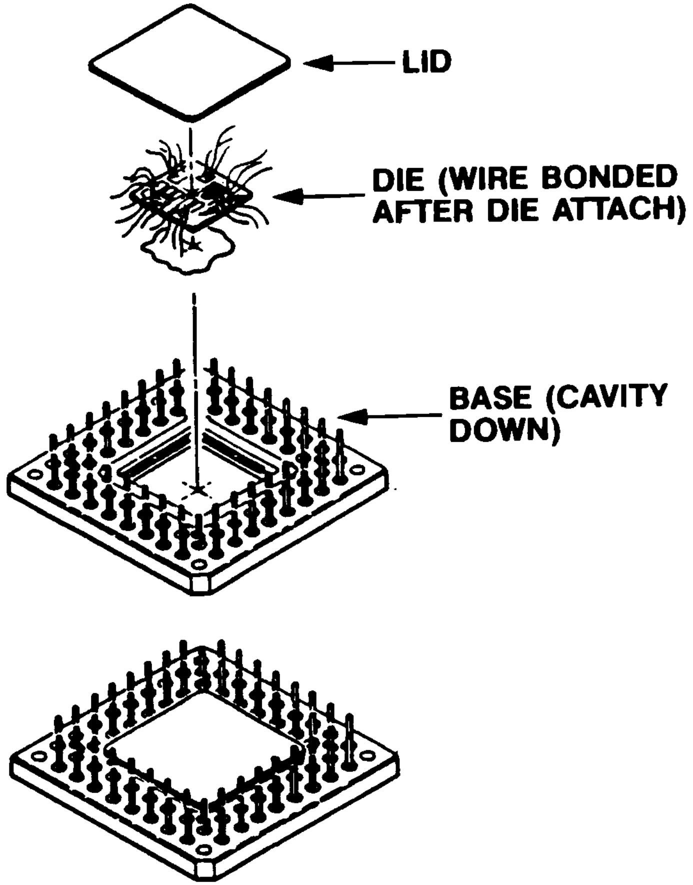
PLASTIC CHIP CARRIER


DIE
LEAD FRAME



TRANSFER MOLD PLASTIC AROUND LEAD FRAME AND CRIMP LEADS

PIN GRID ARRAY


LID
DIE (WIRE BONDED AFTER DIE ATTACH)
BASE (CAVITY DOWN)

ASSEMBLED

ASSEMBLY PROCESS FLOW VERSUS PACKAGE TECHNOLOGY

STEP	CERDIP	CERAMIC	PLASTIC
DIE PREP	SAW DI WASH	SAW DI WASH	SAW DI WASH
INSPECTION	DIE VISUAL	DIE VISUAL	DIE VISUAL
DIE ATTACH	FRAME ATTACH EUTECTIC 440 DEG C	EUTECTIC (440 DEG C)	EUTECTIC (440 DEG C) OR ADHESIVE (170 DEG C, EPOXY. 280 DEG C POLYIMIDE)
WIRE BOND	ALUMINUM (ULTRASONIC)	ALUMINUM (ULTRASONIC) OR GOLD (THERMOSONIC)	GOLD (THERMOSONIC)
INSPECTION	INTERNAL VISUAL GATE	INTERNAL VISUAL GATE	INTERNAL VISUAL GATE
ENCAPSULATION	OXYGEN ATMOS SEAL, 430 DEG 11 MIN	NEUTRAL OR REDUCING ATM 360 DEG C 45 MIN	MOLD AT 175 DEG 1-2 MIN, CURE 175 DEG C, 4 HR
LEAD FINISH	TIN PLATE, GOLD PLATE OR SOLDER TRIM	AS-RECEIVED GOLD PLATE TRIM	DEFLASH, TRIM AND FORM SOLDER SINGULATE
INSPECTION	EXTERNAL VISUAL GATE	EXTERNAL VISUAL GATE	EXTERNAL VISUAL GATE
OUTGOING Q.A. TESTS	HERMETICITY CENTRIFUGE LEAD FATIGUE DIE SHEAR BOND LIFT ACOUSTIC OPENS/SHORTS	HERMETICITY CENTRIFUGE LEAD FATIGUE DIE SHEAR BOND LIFT ACOUSTIC OPENS/SHORTS	LEAD FATIGUE BIAS PRESSURE POT OPENS/SHORTS

PACKAGE TESTING

TEST	MIL. STD 883	TEST COND	DURATION	END POINT	SAM. SIZE
HIGH T STORAGE	1008	200C D,C	168 HR	E	360
		200C P	48 HR	E	360
		200C P	48 HR	WIRE PULL	195
TEMP. CYCLE	1010C	-55C TO 125C C, D, P	1000 CYC	E V H	624
THERMAL SHOCK	1011C	-65C TO 150C C, D, P	200 CYC	E V H	624
STEAM		121C, 2 ATM C, D, P	288 HR	E V	624
HUMIDITY		85C, 85% RH C, D, P	2000 HR	E V	624
SALT ATM	1009A 2004B	35C C, D, P	24 HR	V, LEAD FATIGUE	440
SOLVENTS	2515C	CHEMICAL C, D, P	1 HR	V	88
MECH. SHOCK	2002B	1.5KG PEAK C, D	6 ORIENT	H, E	165
VIBRATION	2007	20 G PEAK C, D	3 ORIENT	H, E	165
CENTRIFUGE	2001D	20/30 KG C, D	Z ORIENT	H, E	504
ACOUSTIC/PIND	2020A	250 HZ C, D	Z ORIENT	H, E	165
DIE ADHERENCE	2019	DIE SHEAR C, D, P		TO DESTR FORCE	96
WIRE BOND	2011	WIRE PULL C, D, P		TO DESTR FORCE	1560
CAVITY MOISTURE	1018	100C BAKE C, D	1 CYCLE	RGA, PPM H2O	15
SEAL INTEGRITY	2024	TORQUE D		TO DEST FORCE	66

PACKAGE TESTING (CONTINUED)

TEST	MIL. STD 883	TEST COND	DURATION	END POINT	SAM. SIZE
LEAD STRENGTH	2004	BEND/FATIGUE C, D, P		TO DEST NO. BENDS	40
SOLDER-ABILITY	2025	BEND (C, D, P)		TO DESTR VIS	228
	2003	100C STEAM C, D, P	1 HR	VIS	
	-	200C BAKE C, D, P	5 HR	VIS	

KEY: C = CERAMIC, D = CERDIP, P = PLASTIC, E = ELECTRICAL MEASUREMENT, H = HERMETICITY TEST, V = VISUAL

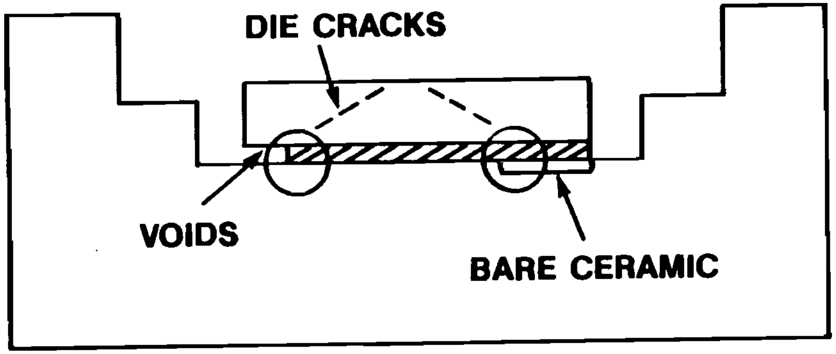
ASSEMBLY DEFECTS AND PACKAGE RELIABILITY JEOPARDIES

MODE	CAUSE	TEST	TECHNOLOGY
DIE CRACKING	DIE ATTACH DEFECT	T/C, T/S V, E (CONTINUITY, STRESS)	C, D, P
DIE OFF	DIE ATTACH DEFECT	V, E(CONTINUITY)	C, D
THIN FILM CRACKING	ASSEMBLY DEFECT	V, E(CONTINUITY)	P
CAVITY MOISTURE	LID SEAL DEFECT RESIDUAL GASSES	RGA, E(TRIPLE TRK)	D, C
DIE CORROSION	IONS FROM PROCESS IONS/MOIST FROM ENV. MOLD/FORM	THB, STEAM, V, E(TRIPLE TRK, CONTINUITY)	P, D
WIRES - ALUMINUM	MACHINE SETUP, MISHANDLING	BOND PULL VISUAL	D, C
- GOLD	CORROSION, IMPURITIES IN PLASTIC, SWEEP DUE TO MOLD, OVERHEAT (PURPLE PLAGUE)	BAKE + BOND PULL E(CONTINUITY, KELVIN)	P, C
PACKAGE CRACKS	MOLDING DEFECTS	T/S, T/C, V	P
	DESIGN (GEOMETRY)	T/S. T/C, V,H	D, C
SOLDERABILITY	OXIDATION, INTERDIFFUSION, IONIC RESIDUE, ETC.	BAKE + SOLDER STEAM + SOLDER	P, D, C

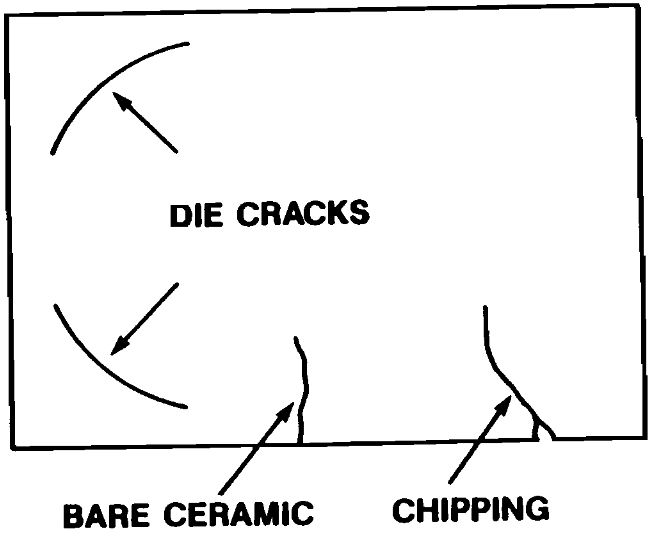
KEY: P = PLASTIC, D = CERDIP, C = CERAMIC, V = VISUAL, H = HERMETIC, E = ELECTRICAL

CRACKS IN CERAMIC PACKAGES

CROSS SECTION VIEW

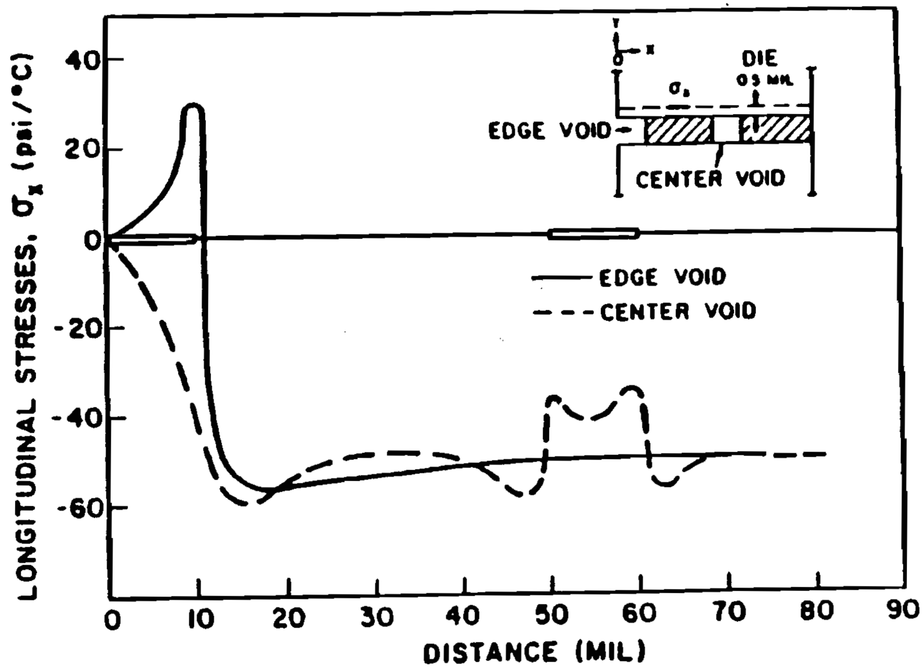

DIE CRACKS
VOIDS
BARE CERAMIC

DIE SURFACE


DIE CRACKS
BARE CERAMIC
CHIPPING

DIE CRACKING

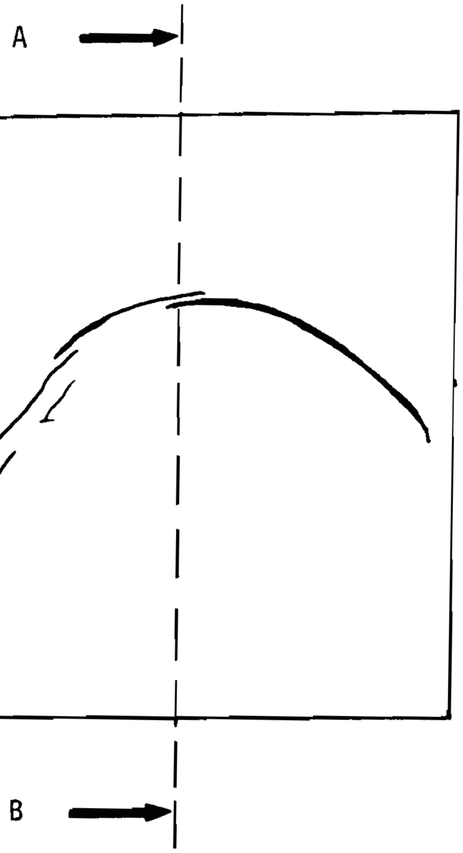
- EDGE VOIDS (NOT CENTER VOIDS) CAUSE HIGH TENSILE STRESS CONCENTRATION



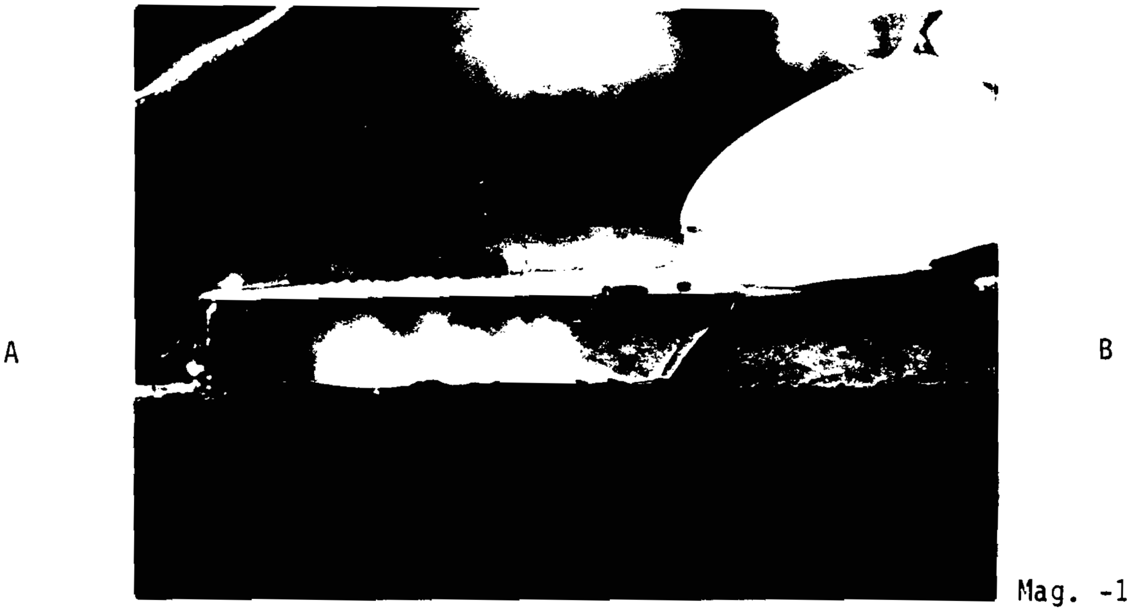
- FLAWS PRE-EXIST IN THE MATERIAL (BACKSIDE PREPARATION)
  - SWAM 1 ~ 10μm FLAWSIZE
  - DISCO .1 ~ 1μm FLAWSIZE
- SMOOTH BACKSIDE IS VERY IMPORTANT

8X

X-Ray Radiograph of unit (#5-6)



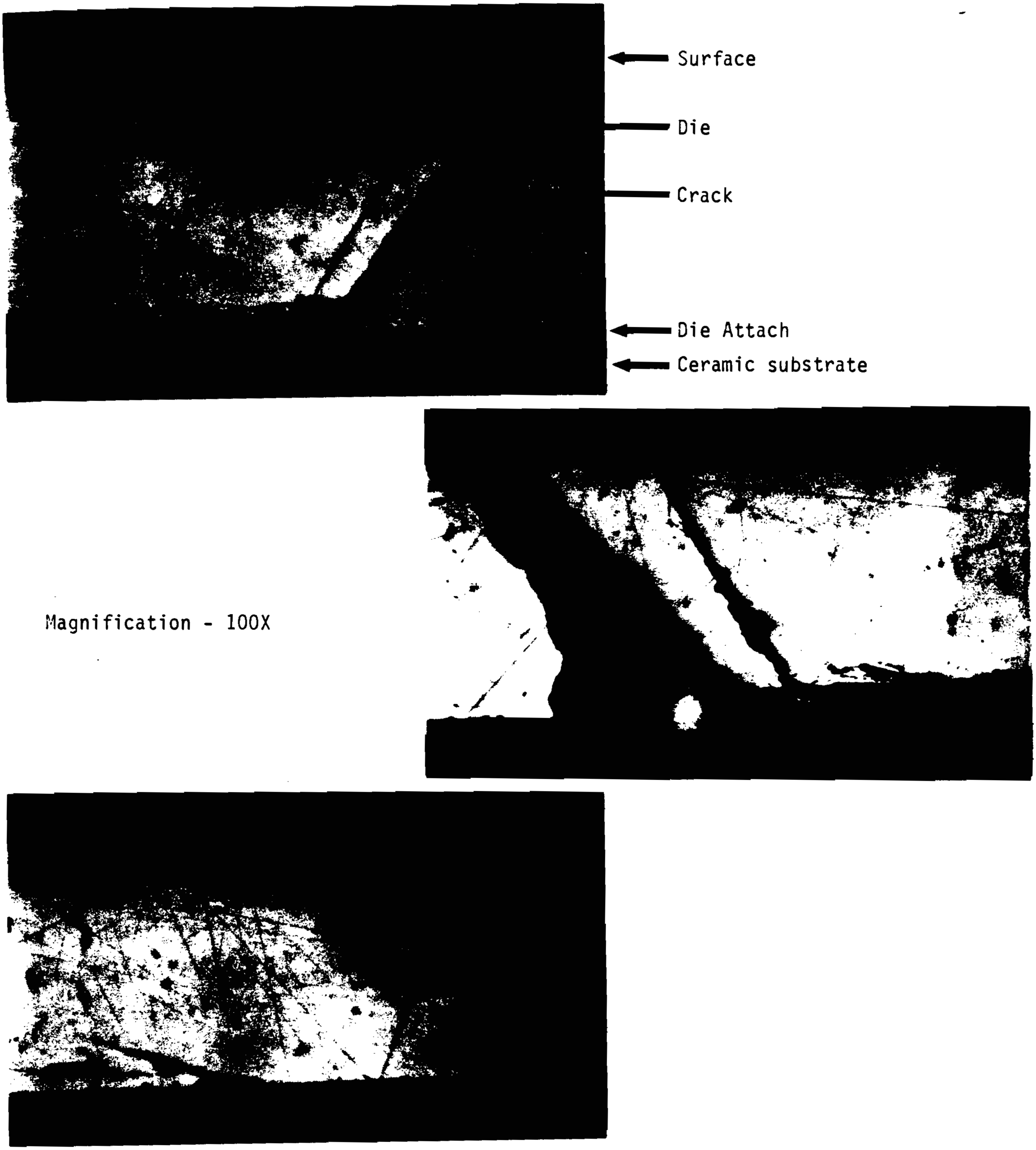
Schematic of cracks on the die surface. Arrows indicate the X-Section plane.



Mag. -16X

FIGURE 11) Die cross-section of unit #5-6 showing the initiation of the die crack at an edge void/separation.

COURTESY RAJEN DIAS, INTEL ASSEMBLY/TEST


Surface
Die
Crack
Die Attach
Ceramic substrate

Magnification - 100X

FIGURE 12) Die cross-section micrographs of unit #5-6 showing die crack initiation at edge voids and propagation to the die surface.

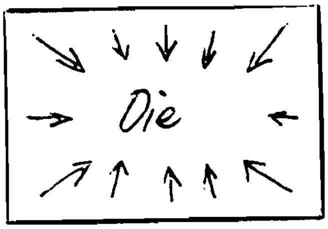
COURTESY RAJEN DIAS, INTEL ASSEMBLY/TEST

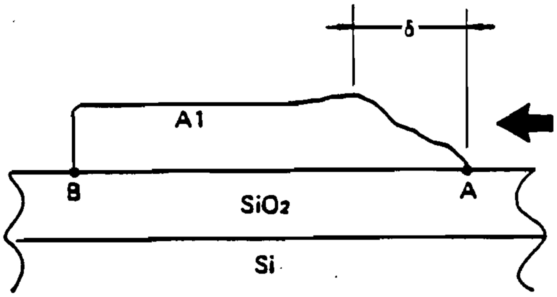
ASSEMBLY DEFECTS AND PACKAGE RELIABILITY JEOPARDIES

MODE	CAUSE	TEST	TECHNOLOGY
DIE CRACKING	DIE ATTACH DEFECT	T/C, T/S V, E (CONTINUITY, STRESS)	C, D, P
DIE OFF	DIE ATTACH DEFECT	V, E(CONTINUITY)	C, D
THIN FILM CRACKING	ASSEMBLY DEFECT	V, E(CONTINUITY)	P
CAVITY MOISTURE	LID SEAL DEFECT RESIDUAL GASSES	RGA, E(TRIPLE TRK)	D, C
DIE CORROSION	IONS FROM PROCESS IONS/MOIST FROM ENV. MOLD/FORM	THB, STEAM, V, E(TRIPLE TRK, CONTINUITY)	P, D
WIRES			
- ALUMINUM	MACHINE SETUP, MISHANDLING	BOND PULL VISUAL	D, C
- GOLD	CORROSION, IMPURITIES IN PLASTIC, SWEEP DUE TO MOLD, OVERHEAT (PURPLE PLAGUE)	BAKE + BOND PULL E(CONTINUITY, KELVIN)	P, C
PACKAGE CRACKS	MOLDING DEFECTS	T/S, T/C, V	P
	DESIGN (GEOMETRY)	T/S. T/C, V,H	D, C
SOLDERABILITY	OXIDATION, INTERDIFFUSION, IONIC RESIDUE, ETC.	BAKE + SOLDER STEAM + SOLDER	P, D, C

KEY: P = PLASTIC, D = CERDIP, C = CERAMIC, V = VISUAL, H = HERMETIC, E = ELECTRICAL

THIN FILM DEFORMATION IN PLASTIC PACKAGES, REF. 21.





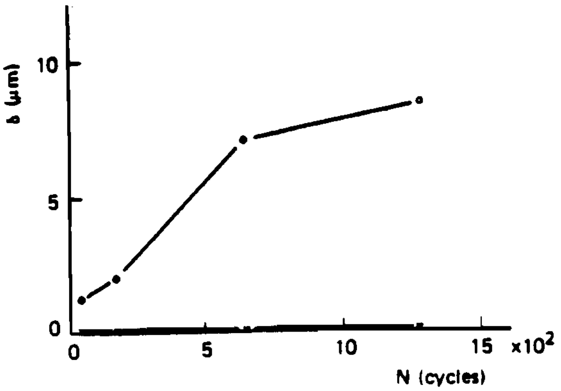


Fig. 4 The effect of molding resins for Al deformation length (δ) versus cycles (N) of thermal shock.

○ resin A
× resin B
r = 1.91 mm (Test No. 1)

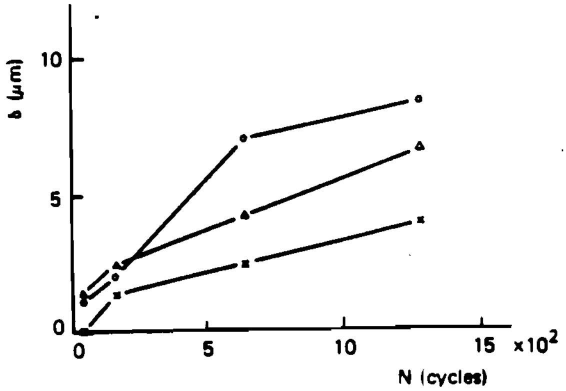


Fig. 5 The effect of chip sizes for δ versus N curves.

○ 2.2 mm x 3.1 mm (r = 1.91 mm)
△ 2.0 mm x 2.2 mm (r = 1.44 mm)
× 1.45 mm x 1.8 mm (r = 0.84 mm)
(Test No. 2)

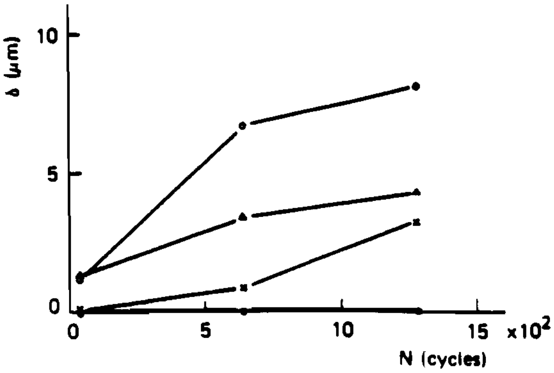


Fig. 6 The effect of the overcoatings for δ versus N curves.

○ none
△ SiO2
× polyimide resin
● JCR (= Junction Coating Resin, silicone varnish)
r = 1.91 mm (Test No. 3)

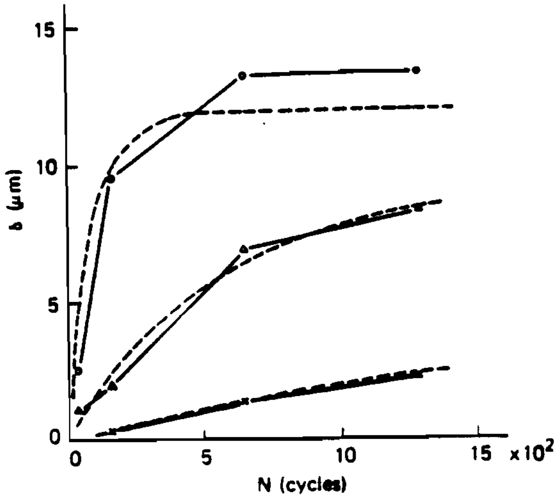


Fig. 7 The effect of the temperature differences of thermal shock for δ versus N curves.

○ –65°C⇄175°C
△ –55°C⇄150°C
× –40°C⇄125°C
r = 1.91 mm (Test No. 4)
Dotted line is the theoretical line due to equation (6).

ASSEMBLY DEFECTS AND PACKAGE RELIABILITY JEOPARDIES

MODE	CAUSE	TEST	TECHNOLOGY
DIE CRACKING	DIE ATTACH DEFECT	T/C, T/S V, E (CONTINUITY, STRESS)	C, D, P
DIE OFF	DIE ATTACH DEFECT	V, E(CONTINUITY)	C, D
THIN FILM CRACKING	ASSEMBLY DEFECT	V, E(CONTINUITY)	P
CAVITY MOISTURE	LID SEAL DEFECT RESIDUAL GASSES	RGA, E(TRIPLE TRK)	D, C
DIE CORROSION	IONS FROM PROCESS IONS/MOIST FROM ENV. MOLD/FORM	THB, STEAM, V, E(TRIPLE TRK, CONTINUITY)	P, D
WIRES - ALUMINUM	MACHINE SETUP, MISHANDLING	BOND PULL VISUAL	D, C
- GOLD	CORROSION, IMPURITIES IN PLASTIC, SWEEP DUE TO MOLD, OVERHEAT (PURPLE PLAGUE)	BAKE + BOND PULL E(CONTINUITY, KELVIN)	P, C
PACKAGE CRACKS	MOLDING DEFECTS	T/S, T/C, V	P
	DESIGN (GEOMETRY)	T/S. T/C, V,H	D, C
SOLDERABILITY	OXIDATION, INTERDIFFUSION, IONIC RESIDUE, ETC.	BAKE + SOLDER STEAM + SOLDER	P, D, C

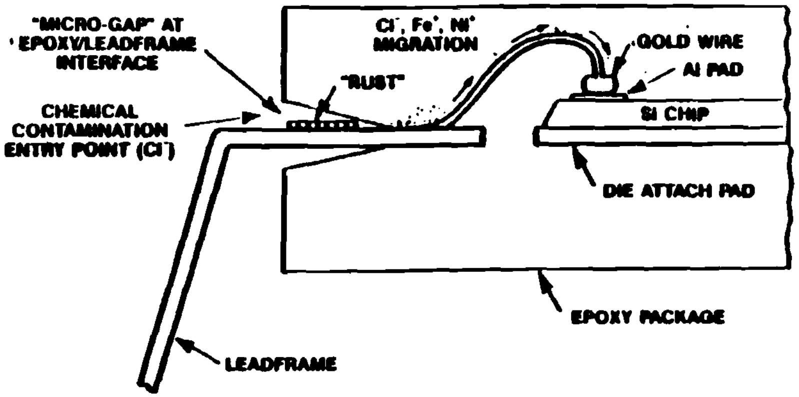
KEY: P = PLASTIC, D = CERDIP, C = CERAMIC, V = VISUAL, H = HERMETIC, E = ELECTRICAL

MODEL FOR BOND PAD CORROSION

CHEMICALS CONTAINING CHLORIDE IONS ENTER THE PACKAGE ALONG THE PLASTIC/LEAD FRAME INTERFACE DUE TO THE INHERENT POOR ADHESION BETWEEN THESE TWO.

DURING 85/81 TESTING, CI AND OTHER CONTAMINANTS MIGRATE ALONG THE LEAD FRAME/PLASTIC INTERFACE TO THE GOLD BOND WIRE, TRAVEL UP THE WIRE TO THE BOND PADS WHERE CORROSION PROCEEDS.

MOISTURE PERMEATION MAY PROCEED BY THE SAME MECHANISM OR THROUGH THE BULK EPOXY.


"MICRO-GAP" AT EPOXY/LEADFRAME INTERFACE
Cl^-, Fe^+, Ni^+ MIGRATION
GOLD WIRE
Al PAD
"RUST"
CHEMICAL CONTAMINATION ENTRY POINT (Cl^-)
Si CHIP
DIE ATTACH PAD
EPOXY PACKAGE
LEADFRAME

CONTAMINATION ENTRY AND MIGRATION PATH
FOR CHLORIDE IONS DURING ASSEMBLY AND THB STRESS

THE INFLUENCE OF PLASTIC ENCAPSULATION ON SURFACE CONDUCTIVITY, REF. 22.

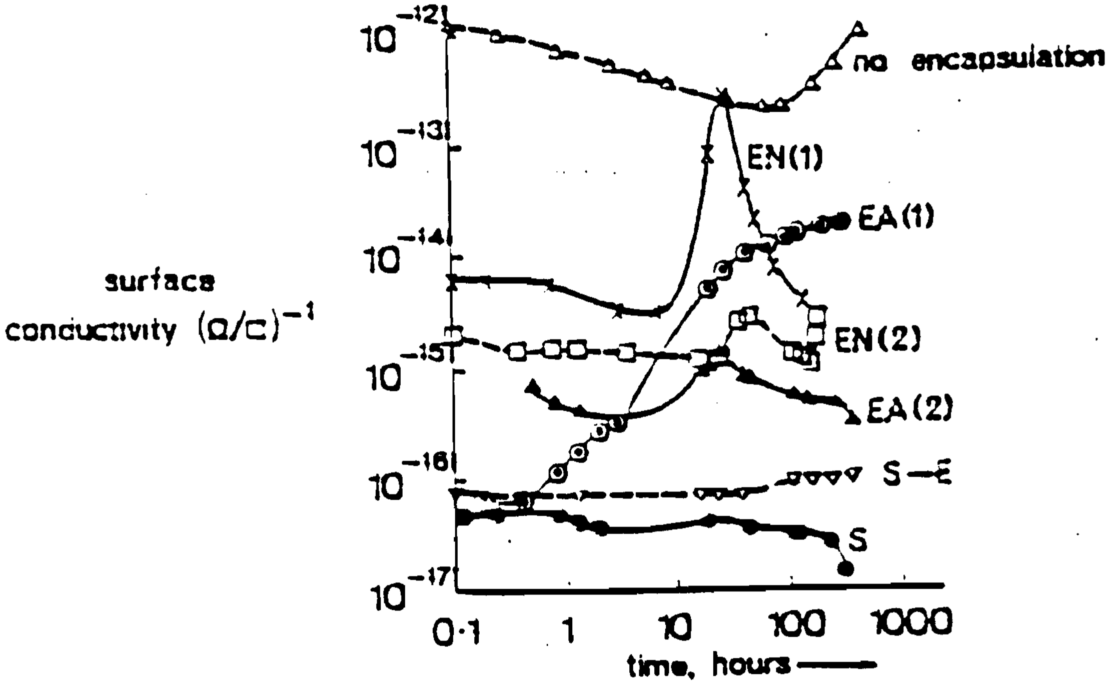


FIG 2 EFFECT OF PLASTIC ENCAPSULATION ON SURFACE CONDUCTIVITY, 110°C, 90% RH, 30V (see Table 1 for code identity)

TABLE I

Plastic Encapsulants Used in the Investigation

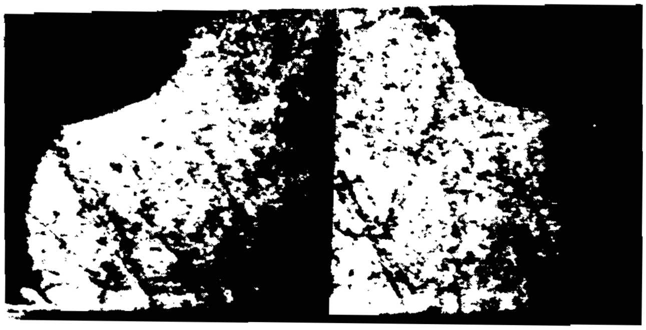
Plastic Encapsulant	Code	Aqueous Extract	
		Conductivity Sm^{-1}	pH
Epoxy novolac (1)	EN(1)	0.015	3.8
Epoxy novolac (2)	EN(2)	0.004	4.1
Epoxy anhydride (1)	EA(1)	0.035	5.4
Epoxy anhydride (2)	EA(2)	0.040	3.2
Silicone	S	0.006	4
Silicone-epoxy	S-E	0.005	4.2

ASSEMBLY DEFECTS AND PACKAGE RELIABILITY JEOPARDIES

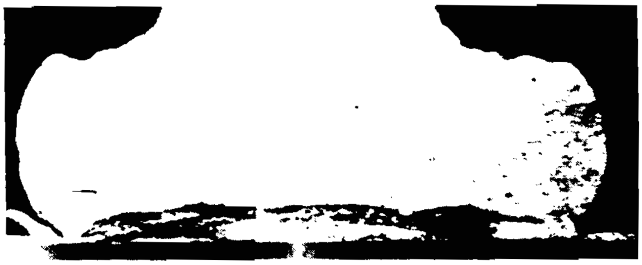
MODE	CAUSE	TEST	TECHNOLOGY
DIE CRACKING	DIE ATTACH DEFECT	T/C, T/S V, E (CONTINUITY, STRESS)	C, D, P
DIE OFF	DIE ATTACH DEFECT	V, E(CONTINUITY)	C, D
THIN FILM CRACKING	ASSEMBLY DEFECT	V, E(CONTINUITY)	P
CAVITY MOISTURE	LID SEAL DEFECT RESIDUAL GASSES	RGA, E(TRIPLE TRK)	D, C
DIE CORROSION	IONS FROM PROCESS IONS/MOIST FROM ENV. MOLD/FORM	THB, STEAM, V, E(TRIPLE TRK, CONTINUITY)	P, D
WIRES			
- ALUMINUM	MACHINE SETUP, MISHANDLING	BOND PULL VISUAL	D, C
- GOLD	CORROSION, IMPURITIES IN PLASTIC, SWEEP DUE TO MOLD, OVERHEAT (PURPLE PLAGUE)	BAKE + BOND PULL E(CONTINUITY, KELVIN)	P, C
PACKAGE CRACKS	MOLDING DEFECTS	T/S, T/C, V	P
	DESIGN (GEOMETRY)	T/S. T/C, V,H	D, C
SOLDERABILITY	OXIDATION, INTERDIFFUSION, IONIC RESIDUE, ETC.	BAKE + SOLDER STEAM + SOLDER	P, D, C

KEY: P = PLASTIC, D = CERDIP, C = CERAMIC, V = VISUAL, H = HERMETIC, E = ELECTRICAL

BOND PAD DEGRADATION, REFERENCE 12.

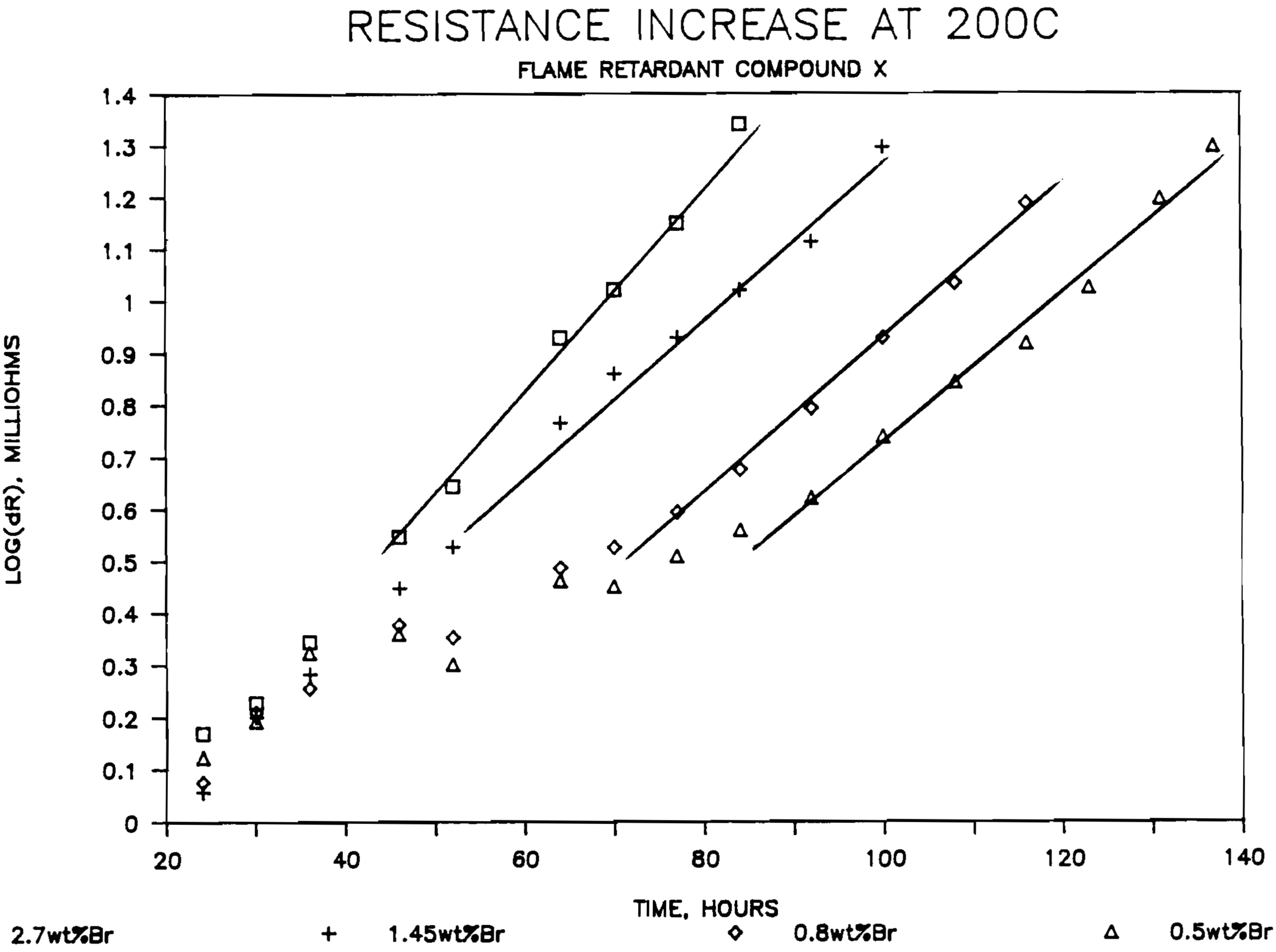


Sectioned Bond - As Encapsulated - R = 0
Figure 12



Sectioned Bond - Bake 200 Hrs at 200C - R = 63 mΩ
Figure 13

GOLD-ALUMINUM WIRBOND CONTACT RESISTANCE VERSUS TIME AT 200C AND AS A FUNCTION OF BROMINE CONTENT.



COURTESY SYED AHMAD, INTEL ASSEMBLY/TEST

ASSEMBLY DEFECTS AND PACKAGE RELIABILITY JEOPARDIES

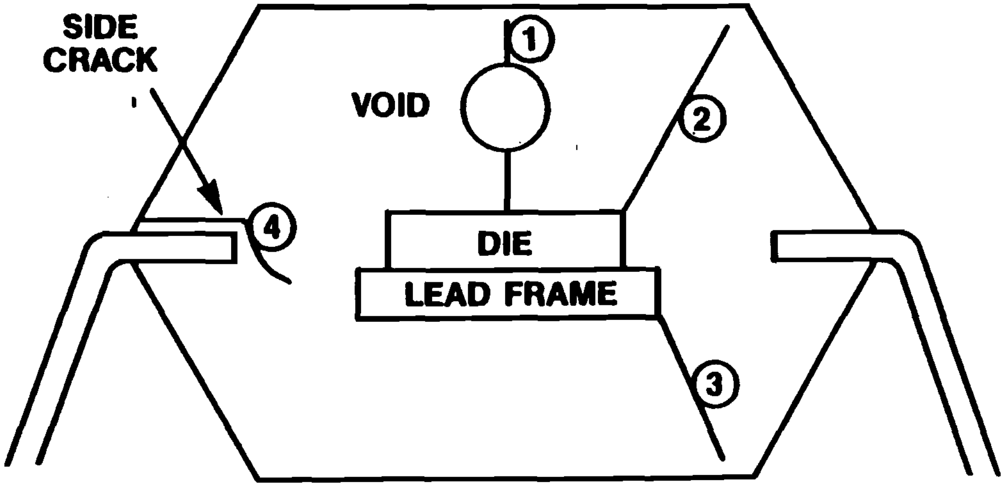
MODE	CAUSE	TEST	TECHNOLOGY
DIE CRACKING	DIE ATTACH DEFECT	T/C, T/S V, E (CONTINUITY, STRESS)	C, D, P
DIE OFF	DIE ATTACH DEFECT	V, E(CONTINUITY)	C, D
THIN FILM CRACKING	ASSEMBLY DEFECT	V, E(CONTINUITY)	P
CAVITY MOISTURE	LID SEAL DEFECT RESIDUAL GASSES	RGA, E(TRIPLE TRK)	D, C
DIE CORROSION	IONS FROM PROCESS IONS/MOIST FROM ENV. MOLD/FORM	THB, STEAM, V, E(TRIPLE TRK, CONTINUITY)	P, D
WIRES			
- ALUMINUM	MACHINE SETUP, MISHANDLING	BOND PULL VISUAL	D, C
- GOLD	CORROSION, IMPURITIES IN PLASTIC, SWEEP DUE TO MOLD, OVERHEAT (PURPLE PLAGUE)	BAKE + BOND PULL E(CONTINUITY, KELVIN)	P, C
PACKAGE CRACKS	MOLDING DEFECTS	T/S, T/C, V	P
	DESIGN (GEOMETRY)	T/S. T/C, V,H	D, C
SOLDERABILITY	OXIDATION, INTERDIFFUSION, IONIC RESIDUE, ETC.	BAKE + SOLDER STEAM + SOLDER	P, D, C

KEY: P = PLASTIC, D = CERDIP, C = CERAMIC, V = VISUAL, H = HERMETIC, E = ELECTRICAL

STRESS IN PLASTIC PACKAGES

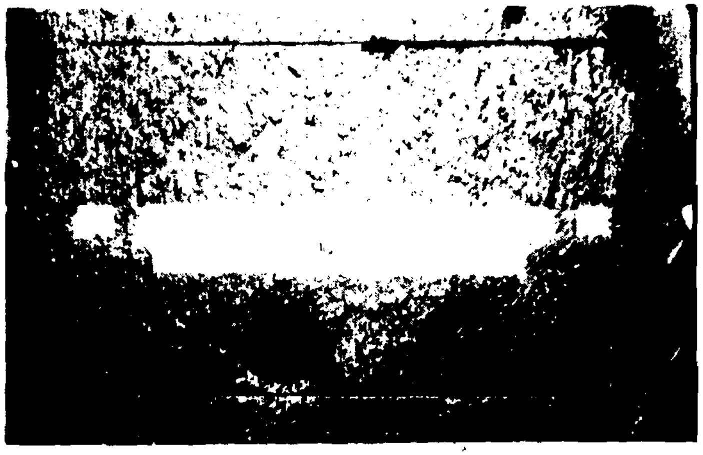
FAILURE MECHANISM DRIVEN BY STRESS CONCENTRATIONS

- VOID—STRESS CONCENTRATOR
- DIE/PAD CORNER—THERMAL MISMATCH
  —GEOMETRIC DISCONTINUITY
- SIDE CRACKS—POOR LEAD FRAME/MOLDING COMPOUND ADHESION
  —LEAD FRAME DESIGN
  —DTF OPERATION

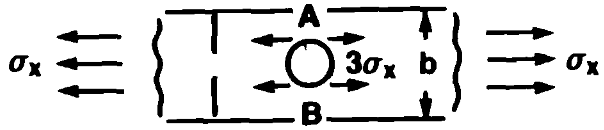

SIDE CRACK
VOID
①
②
③
④
DIE
LEAD FRAME

MOLDING VOIDS

- VOIDS CREATED DURING MOLDING OPERATION
- STRESS CONCENTRATIONS ARISE AROUND VOIDS DUE TO DISCONTINUITY
- TEMPERATURE CYCLING OF PLASTIC PACKAGES CAUSES CRACKS TO FORM AND PROPOGATE UP TO THE SURFACE AND *DOWN* TO THE DIE

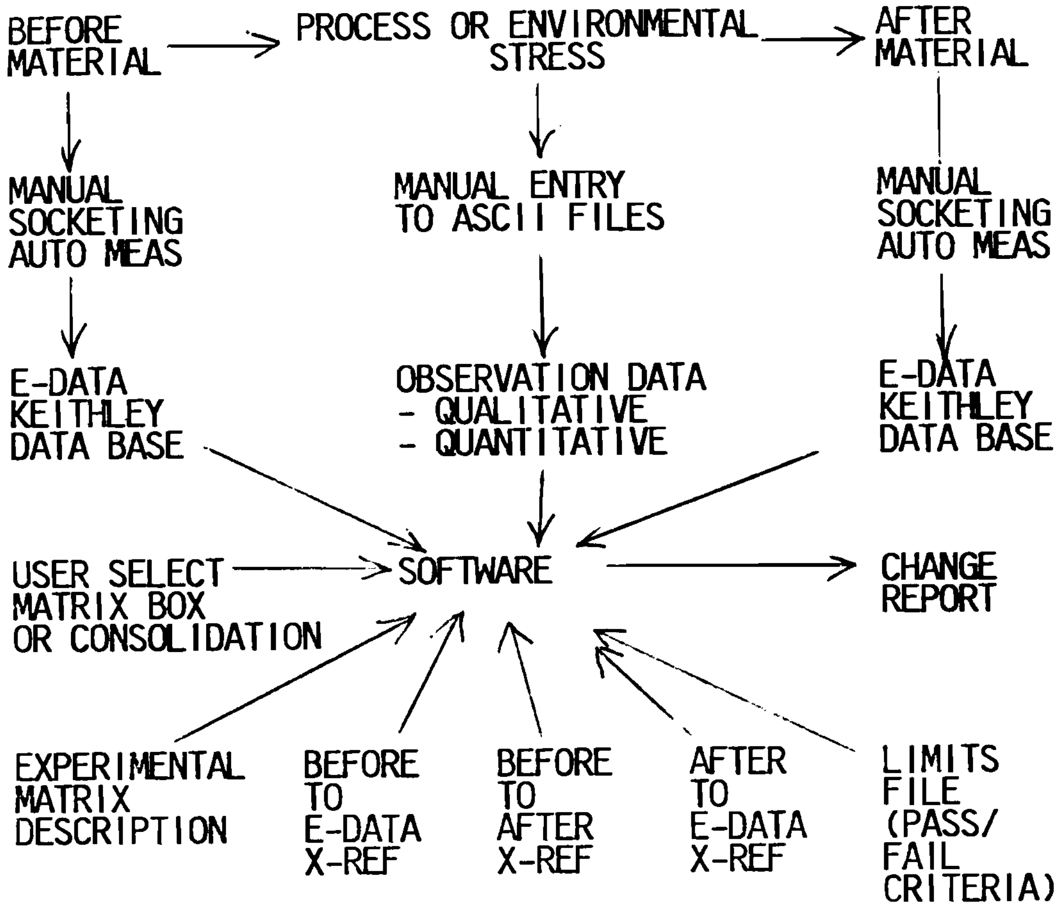


WHEN A VOID EXISTS INSIDE A PLATE UNDER A UNIFORM STRESS FIELD σ_x (a ≪ b)



THE STRESS AT POINT A AND B CAN BE AS HIGH AS 3 σ_x

3. DATA ANALYSIS SOFTWARE



BEFORE MATERIAL

PROCESS OR ENVIRONMENTAL STRESS

AFTER MATERIAL

MANUAL SOCKETING AUTO MEAS

MANUAL ENTRY TO ASCII FILES

MANUAL SOCKETING AUTO MEAS

E-DATA KEITHLEY DATA BASE

OBSERVATION DATA
- QUALITATIVE
- QUANTITATIVE

E-DATA KEITHLEY DATA BASE

USER SELECT MATRIX BOX OR CONSOLIDATION

SOFTWARE

CHANGE REPORT

EXPERIMENTAL MATRIX DESCRIPTION

BEFORE TO E-DATA X-REF

BEFORE TO AFTER X-REF

AFTER TO E-DATA X-REF

LIMITS FILE (PASS/FAIL CRITERIA)

4. SENSOR DESIGN

- THERMAL
- KELVIN
- CONTINUITY
- WIRE LOCATION
- STRAIN
- CORROSION AND/OR MOISTURE

THERMAL ELEMENT DESIGN

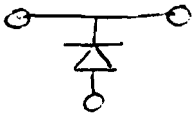
THEORY:

TO MEASURE THERMAL IMPEDANCE OF PACKAGE, DISSIPATE A KNOWN AMOUNT OF POWER, AND MEASURE THE CORRESPONDING TEMPERATURE RISE.

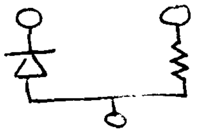
THERMAL IMPEDANCE = (TJ - TC)/P,

WHERE TJ IS THE JUNCTION TEMPERATURE AND TC IS THE CASE TEMPERATURE. TJ - TC IS DETERMINED BY USING A CONSTANT CURRENT TO FORWARD BIAS A DIODE (AT NEGLIGIBLE POWER) AND BY MONITORING THE VOLTAGE ACROSS IT. I=IS[EXP(V/KT)-1] BECOMES V=CONSTANT X T. THE CONSTANT IS DETERMINED BY CALIBRATION IN A THERMAL BATH. THE POWER, P, IS DETERMINED BY MEASURING THE CURRENT THROUGH AND VOLTAGE ACROSS A HEATER ELEMENT. THE HEATER AND THE DIODE CAN BE THE SAME, OR SEPARATE:

AC
(TEMPORAL RESTRICTIONS)
REF. 2



DC
(SPATIAL RESTRICTIONS)
REF. 3



SEE REF. 1 FOR REVIEW AND SEE REF. 4 FOR MEASUREMENT GUIDELINES.

DESIGN GUIDELINES:

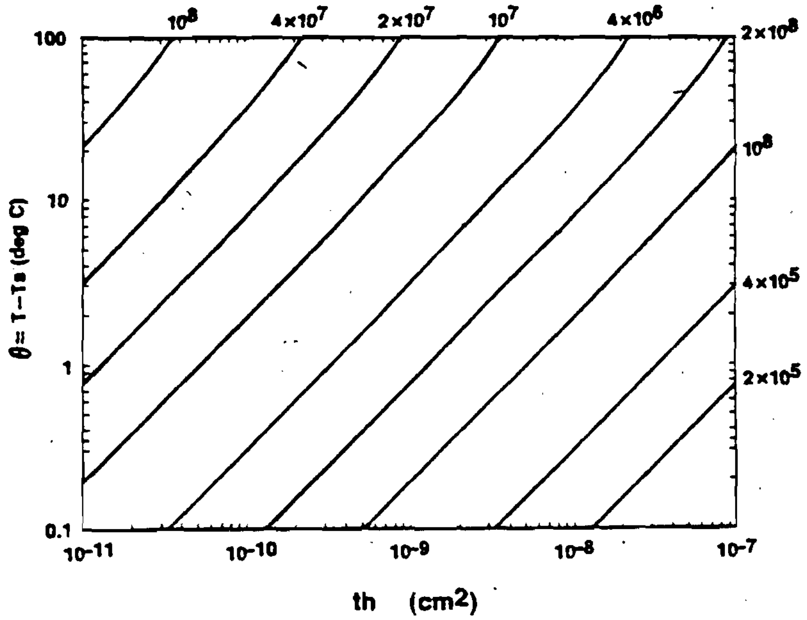
O CURRENT DENSITY IN AL LESS THAN 1XE5 AMP/CM2.

TWO REASONS: ELECTROMIGRATION, THROUGH-FILM TEMPERATURE PROFILES. REF. 5

T = METAL THICKNESS

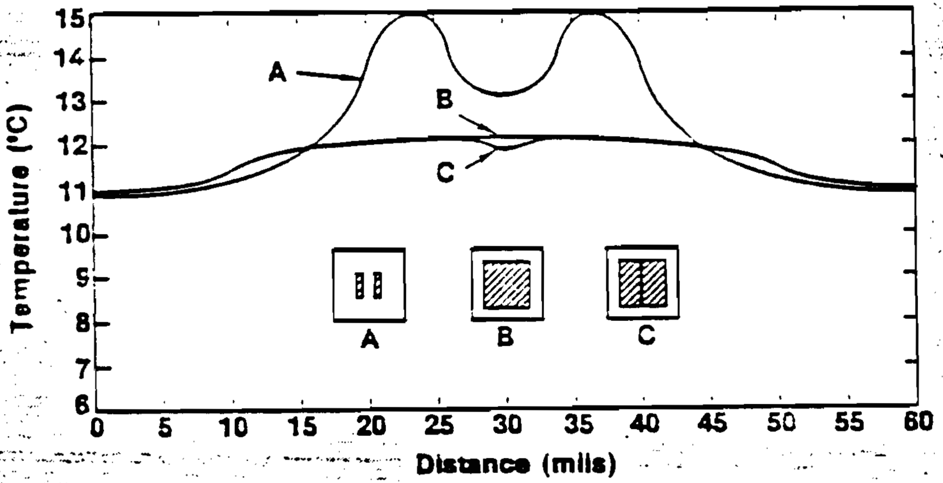
H = DIELECTRIC THICKNESS

DIELECTRIC = THERMAL SIO2



THERMAL ELEMENT DESIGN (CONTINUED)

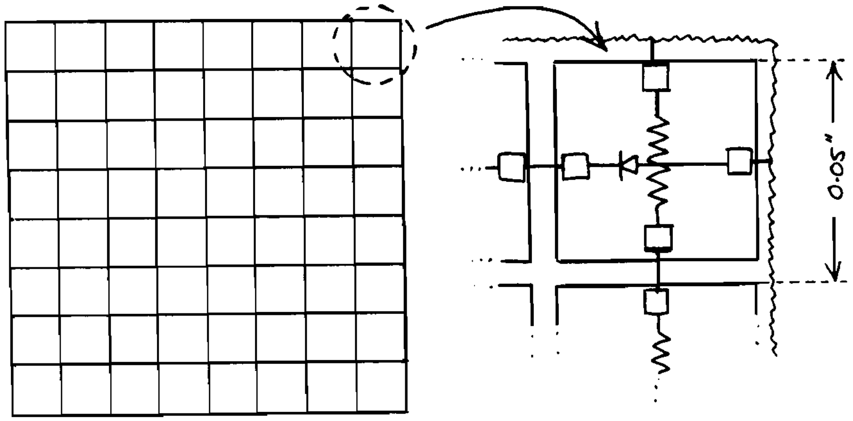
- CURRENT DENSITY IN AL CONTACTS LESS THAN 1XE5 AMP/CM^2.
- VOLTAGE LESS THAN 10 VOLTS BETWEEN PINS.
- CURRENT IN WIRES LESS THAN 100 MA/WIRE.
- CAPABILITY OF CAUSING A TEMPERATURE RISE OF 20 DEG C.
- MAXIMUM POWER DISSIPATION OF ABOUT 4 WATTS/CM2.
- USE SEPARATE HEATER AND SENSOR.
- USE POLYSILICON HEATER (NO JUNCTION PROBLEMS).
- KEEP RESISTANCE OF DIODE INTERCONNECTS NEGLIGIBLE.
- SEPARATION OF HEATER AND SENSOR LESS THAN 2 MILS (REF. 1).



THERMAL ELEMENT DESIGN (CONTINUED)

EXAMPLE:

SIMULATE A 400 MIL SQUARE CHIP DISSIPATING AT LEAST 4 WATTS. THE CHIP IS MADE OF IDENTICAL MODULES 50 MILS SQUARE. DESIGN A POLYSILICON HEATER.



DISSIPATION PER CELL > 4/64 = 0.0625 WATTS = PCELL

ONE WIRE IN, ONE OUT, SO IMAX = 100 MA

TOTAL VOLTAGE DROP ACROSS CHIP < 10 V, SO FOR MODULE, VMAX = 10/8 = 1.25 V

SO PCELL/IMAX^2 < R < VMAX^2/PCELL,

OR 6.25 OHMS < R < 25 OHMS.

POLYSILICON, OR DIFFUSIONS HAVE TYPICALLY 10 - 20 OHMS/SQUARE. SO MAKE THE HEATER ONE SQUARE OF POLYSILICON.

PROBLEM:

COULD ALUMINUM BE USED AS A HEATER?

PROBLEM:

COULD ALUMINUM BE USED AS A HEATER?

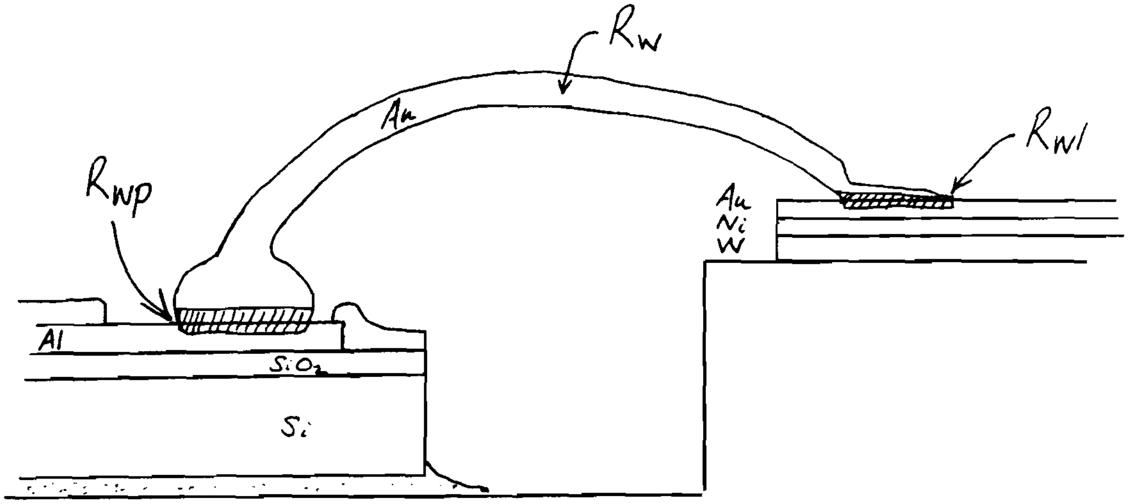
ANSWER:

ALUMINUM TYPICALLY HAS A SHEET RESISTANCE OF 0.05 OHMS/SQUARE (AND THICKNESS OF 1.2 MICRONS), SO WE'D NEED 125-500 SQUARES OF ALUMINUM. FOR 100MA AND 1.2 MICRONS OF ALUMINUM, THE MINIMUM LINEWIDTH IS ROUGHLY 85 MICRONS TO PREVENT ELECTROMIGRATION (1XE5 A/CM^2 CURRENT LIMIT), AND STEEP THROUGH-FILM TEMPERATURE VARIATIONS. THE TOTAL AREA OF ALUMINUM REQUIRED IS THEREFORE AT LEAST 125 X (85/25.4)2 = 1400 SQUARE MILS. THIS COMPARES WITH 2500 SQUARE MILS AVAILABLE ON THE MODULE.

KELVIN WIRE RESISTANCE MEASUREMENTS

THEORY:

THERE ARE THREE RESISTANCES OF INTEREST FOR ANY WIRE:



TYPICALLY, RWP OR RWL WILL INCREASE AS THE WIRE/PAD OR WIRE/LEAD FINGER INTERFACE DEGRADES UNDER ENVIRONMENTAL STRESS. IT IS DESIRABLE TO MEASURE CHANGES IN THESE INTERFACIAL RESISTANCES SEPARATELY.

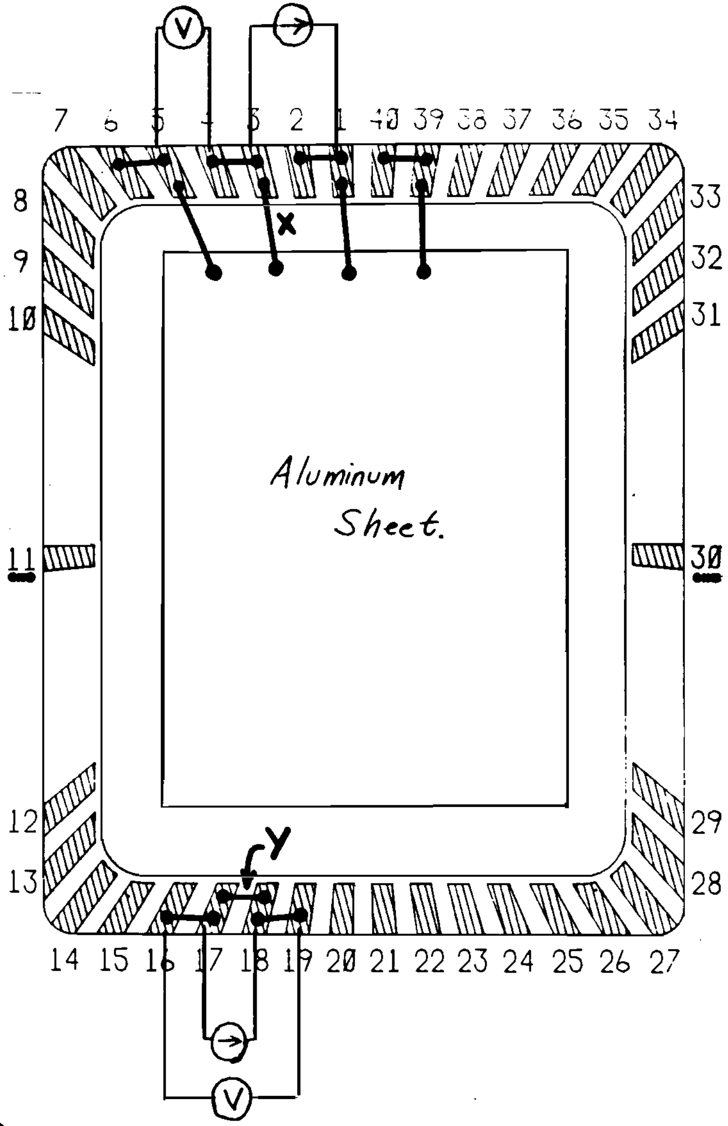
TO MEASURE CHANGES IN RWP OR RWL, WE NEED

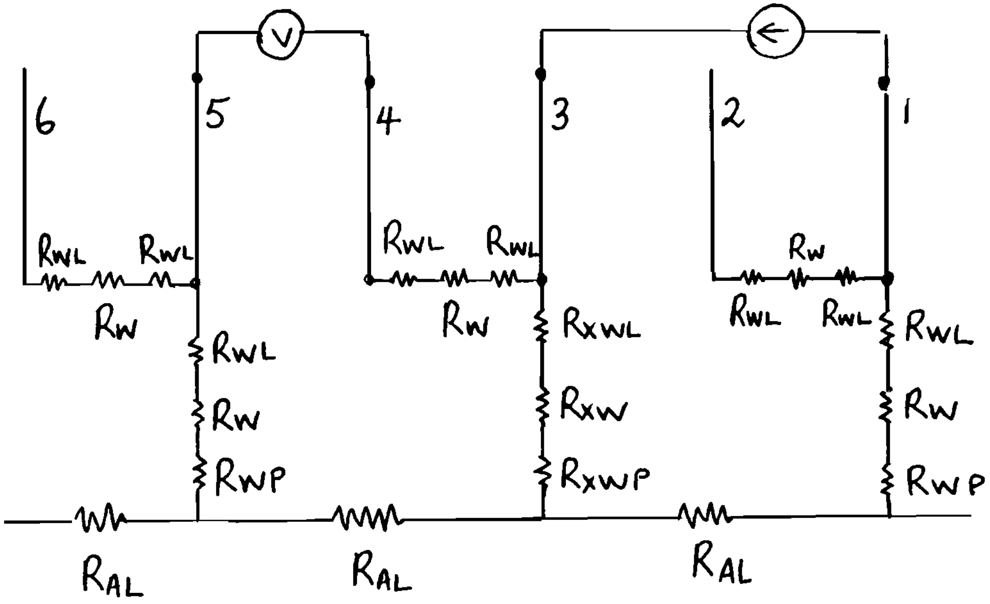
(I) A NUMBER OF BOND PADS SHORTED TOGETHER, OR A SHEET OF ALUMINUM.

(II) GROUPS OF LEAD FINGERS BONDED TO THE SHEET.

(III) AT LEAST 4 LEAD FINGERS BONDED TO EACH OTHER.

KELVIN WIRE RESISTANCE MEASUREMENTS (CONTINUED)


V
→
7 6 5 4 3 2 1 40 39 38 37 36 35 34
8
9
10
11
12
13
33
32
31
30
29
28
X
Aluminum Sheet.
Y
14 15 16 17 18 19 20 21 22 23 24 25 26 27
→
V


V
←
6
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4
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2
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RWL RWL
RW
RWL RWL
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RW
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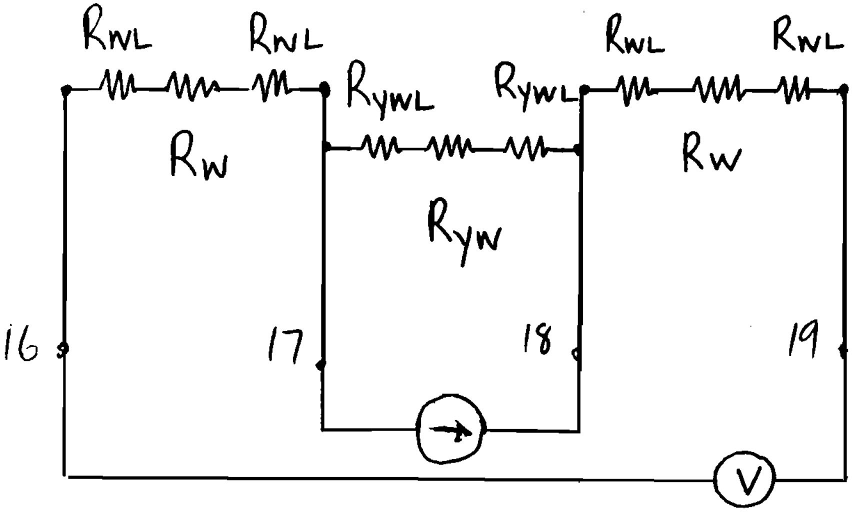

RWL RWL
RW
RYWL RYWL
RYW
RWL RWL
RW
16
17
18
19
→
V

KELVIN WIRE RESISTANCE MEASUREMENTS (CONTINUED)

FOR, EXAMPLE, FORCE CURRENT THROUGH PIN 1, WITHDRAW THROUGH PIN 3, AND MEASURE THE VOLTAGE BETWEEN PINS 4 AND 5. THIS GIVES THE RESISTANCE OF BOND X AS

$$RX = RXW + RXWL + RXWP$$

NOW FORCE CURRENT INTO PIN 18 AND WITHDRAW IT FROM PIN 17 AND MEASURE THE VOLTAGE BETWEEN PINS 16 AND 19. THIS GIVES THE RESISTANCE OF THE BOND Y AS

$$RY = RYW + 2RYWL.$$

COMPUTE R,

$$R = RX - RY/2 = RXW - RYW/2 + RXWP.$$

RXW AND RYW WILL CHANGE LITTLE WITH ENVIRONMENTAL STRESS, SO CHANGES IN R WILL BE A GOOD MEASURE OF CHANGES IN THE INTERFACIAL RESISTANCE RXWP. WE HAVE ASSUMED THAT RXWL = RYWL.

GOOD TECHNIQUE WOULD UTILIZE A HIGH-RESOLUTION DVM, AND A CONSTANT CURRENT SOURCE. TYPICAL RESISTANCES MEASURED WOULD BE 100 MILLIOHMS, AND RESOLUTION NEEDED IS 1 MILLIOHM. IF A CURRENT OF 100 MA IS FORCED, THE VOLTAGE RESOLUTION NEEDED IS 100 MICROVOLTS.

PROBLEMS:

HOW WOULD ONE MEASURE RWP DIRECTLY, WITHOUT HAVING TO CORRECT FOR RWL?

WHAT HAPPENS IF THE BOND PADS ARE CONNECTED BY INTERCONNECT OF APPRECIABLE RESISTANCE?

CONTINUITY SENSOR

PROBLEM:

HOW BIG A CRACK IN AN INTERCONNECT BEFORE THERE IS A DETECTABLE INCREASE IN RESISTANCE?

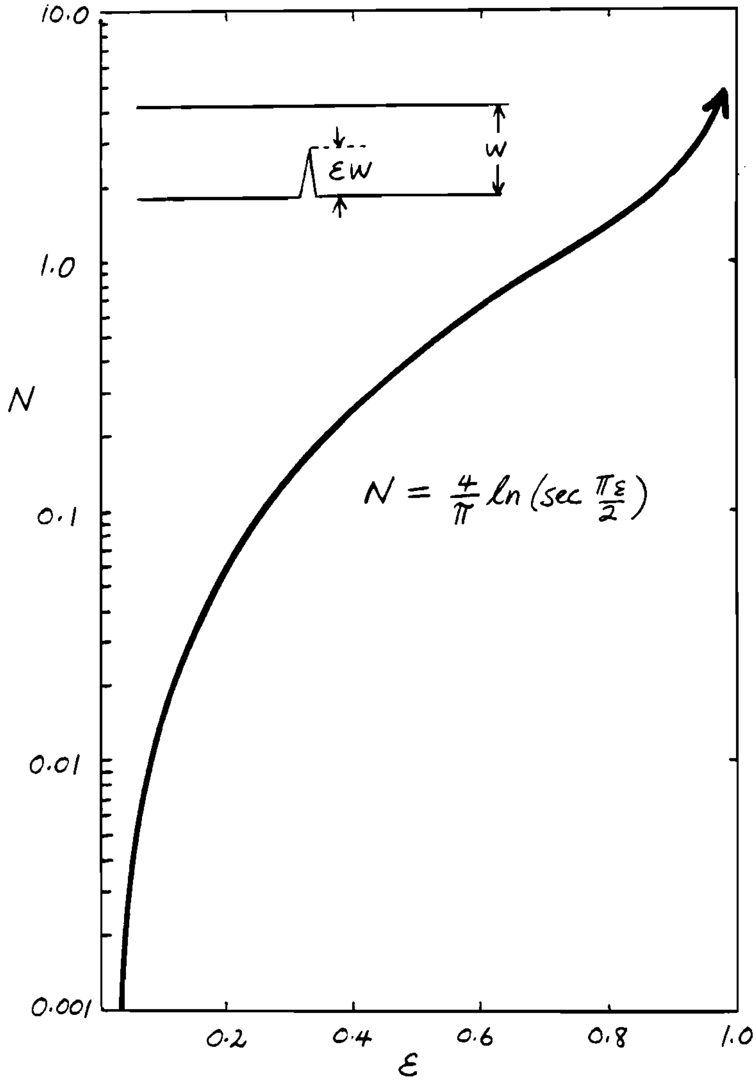
THEORY:

SOLVED BY CONFORMAL MAPPING BY P. M. HALL, REF. 13. THE NUMBER OF EXTRA SQUARES DUE TO A CRACK IS GIVEN BY

NUMBER OF EXTRA SQUARES = (4/PI)LN[SEC(PI*E/2)]

WHERE E IS THE CRACK LENGTH AS A FRACTION OF THE LINEWIDTH. A GOOD RULE OF THUMB: 70% CRACKED GIVES ONE EXTRA SQUARE.

LONG, NARROW SENSORS ARE ONLY DETECTED AS GOOD, OR OPEN.



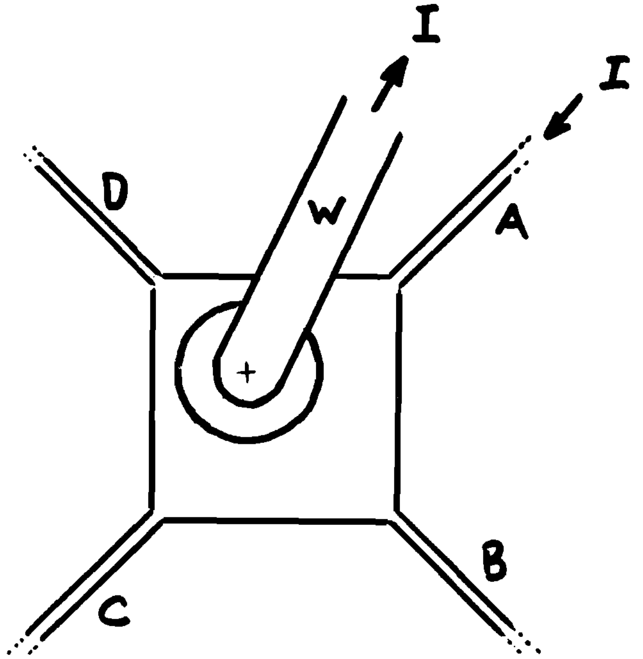
WIRE BOND POSITION SENSOR

MOTIVATION:

VISUAL MEASUREMENTS OF WIRE-BOND LOCATION ON BOND PADS ARE TEDIOUS. ELECTRICAL TECHNIQUE IS MORE CONVENIENT, ESPECIALLY IF LARGE NUMBERS OF WIRE-BOND LOCATIONS ARE TO BE DETERMINED.

METHOD:

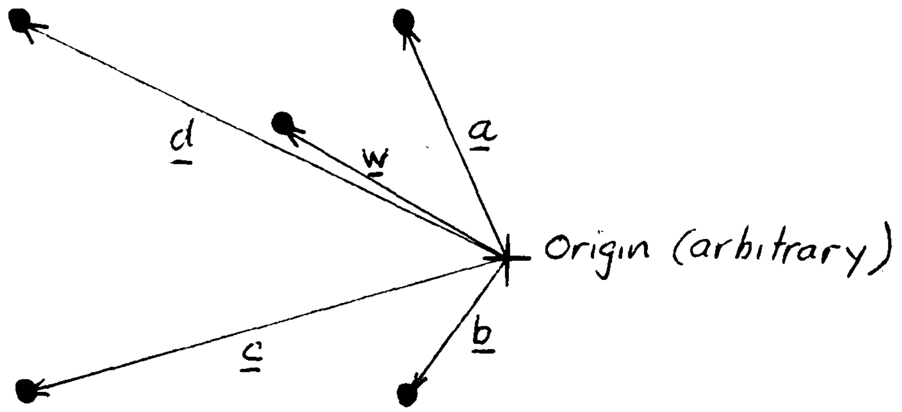
A POSITION-SENSITIVE PAD HAS ELECTRICAL CONNECTION TO EACH OF ITS CORNERS AS SHOWN:



CURRENT IS FORCED INTO CORNER A, AND WITHDRAWN THROUGH THE WIRE, W. THE POTENTIAL DIFFERENCE IS MEASURED BETWEEN CORNERS B AND D. NOW REPEAT, BY CYCLIC PERMUTATION OF A, B, C AND D. THE RESULTING FOUR RESISTANCES (OVER-) DETERMINE THE LOCATION OF THE BALL.

WIRE BOND POSITION SENSOR (CONTINUED)

THEORY:



THE THEORY IS STRAIGHT-FORWARD FOR THE CASE OF AN INFINITE SHEET OF ALUMINUM WITH CONTACTS ARRANGED IN A SQUARE (AT POSITIONS A, B, C, AND D) AND WITH THE CENTROID OF THE BALL AT W. ELEMENTARY THEORY GIVES THE POTENTIAL DIFFERENCE (EXPRESSED AS RESISTANCE) BETWEEN B AND D DUE TO THE SOURCE AT A AS

RBD(A) = (RHO/2*PI)*LN(|B-A|/|D-A|) = 0

WHEREAS THE POTENTIAL DIFFERENCE DUE TO THE SINK AT THE WIRE IS

RBD(W) = -(RHO/2*PI)*LN(|B-W|/|D-W|).

SO THE TOTAL POTENTIAL DIFFERENCE IS RBD = RBD(W)+RBD(A) = RBD(W). DEFINE

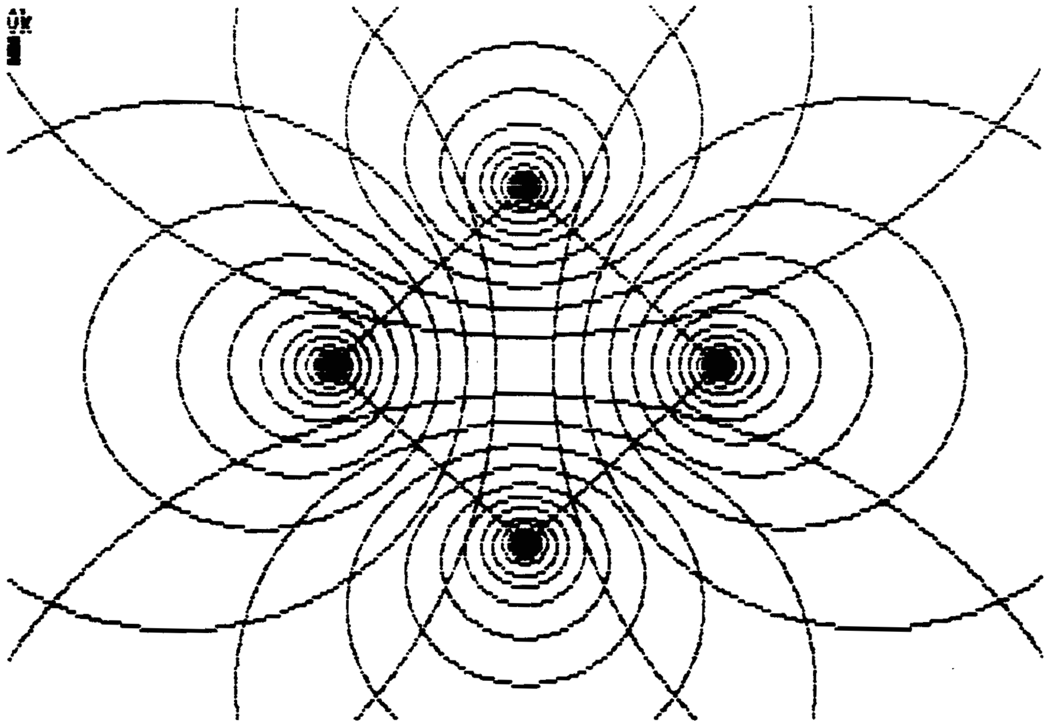
KBD = EXP(4*PI*RBD/RHO)

THEN THE LOCUS OF W CORRESPONDING TO A CONSTANT VALUE OF RBD IS GIVEN BY

|D-W|/|B-W| = SQRT(KBD)

THIS LOCUS IS A SET OF CIRCLES OF RADIUS 2*SQRT(K)/|K-1| AND CENTER (K+1/K-1,0), REFERRED TO THE COORDINATES SHOWN ABOVE. A SIMILAR SET OF LOCI CAN BE DRAWN FOR EACH OF THE OTHER 3 MEASUREMENTS. WHEN THESE ARE SUPERIMPOSED WE PRODUCE A SET OF COORDINATES BY WHICH THE BALL CAN BE LOCATED.

WIRE BOND POSITION SENSOR (CONTINUED)



PROBLEMS:

DERIVE THE FOUR-POINT PROBE FORMULA FOR AN INFINITE SHEET.

DERIVE THE LOCUS SHOWN ABOVE.

SKETCH HOW THE "EQUIPOTENTIALS" WILL BE CHANGED IF THE BOND PAD IS FINITE; IF THE BALL IS NOT A POINT SOURCE/SINK.

WHAT INSTRUMENTS ETC. (RESOLUTION, AMOUNT OF CURRENT ETC.) IS NECESSARY TO MAKE THIS MEASUREMENT.

WHAT IS THE EFFECT OF THE WIRE RESISTANCE, THE RESISTANCES OF THE CONTACTS TO THE CORNERS OF THE BOND PADS?

STRAIN GAUGE DESIGN

PURPOSE:

STRAINS ARE INTRODUCED INTO CHIPS THROUGHOUT THE PROCESSING CYCLE, BUT THE LARGEST STRAINS ARE INTRODUCED DURING ASSEMBLY. THE MAIN SOURCES OF STATIC STRAIN ARE INTRODUCED AT DIE-ATTACH DUE TO THERMAL COEFFICIENT MISMATCH BETWEEN SUBSTRATE AND DIE, AND AT SEAL DUE TO ENCAPSULATION IN PLASTIC PACKAGES. DYNAMIC STRAINS ALSO OCCUR DURING THE THERMAL CYCLING AND SHOCK NEEDED TO QUALIFY PACKAGES. THE PIEZORESISTANCE PHENOMENON IN SILICON PROVIDES AN OPPORTUNITY TO MEASURE THESE STRAINS.

THEORY:

THE PIEZORESISTANCE PHENOMENON COUPLES THE FRACTIONAL CHANGE IN RESISTANCE IN THE I DIRECTION TO THE NORMAL σ AND SHEAR τ IMPOSED STRESSES FOR CUBIC CRYSTALS SUCH AS SILICON VIA THREE FUNDAMENTAL PIEZORESISTANCE COEFFICIENTS, π_{11}, π_{12}, π_{44} :

$$\left.\frac{\Delta R}{R}\right|_i = \pi_{i1}\sigma_1 + \pi_{i2}\sigma_2 + \pi_{i3}\sigma_3 + \pi_{i4}\tau_{23} + \pi_{i5}\tau_{13} + \pi_{i6}\tau_{12} \qquad (1)$$

WHERE I = 1,2,3. NOTE THAT THE PIEZORESISTANCE COEFFICIENTS HAVE THE FOLLOWING PROPERTIES WHEN 1, 2, AND 3 ARE THE CUBIC AXES:

$$\pi_{11} = \pi_{22} = \pi_{33}, \quad \pi_{12} = \pi_{13} = \pi_{23}, \quad \pi_{ij} = \pi_{ji},$$
$$\pi_{44} = \pi_{55} = \pi_{66}, \quad \pi_{56} = \pi_{45} = \pi_{46} = 0.$$

IT IS USEFUL TO HAVE A FEEL FOR THE WAY IN WHICH VARIES WITH COMPOSITION AND TEMPERATURE. THEORY SHOWS (SEE, EG. REF.14.) THAT

$$\pi_{ij} = Q_{ij}\,P(N,T) \qquad (2)$$

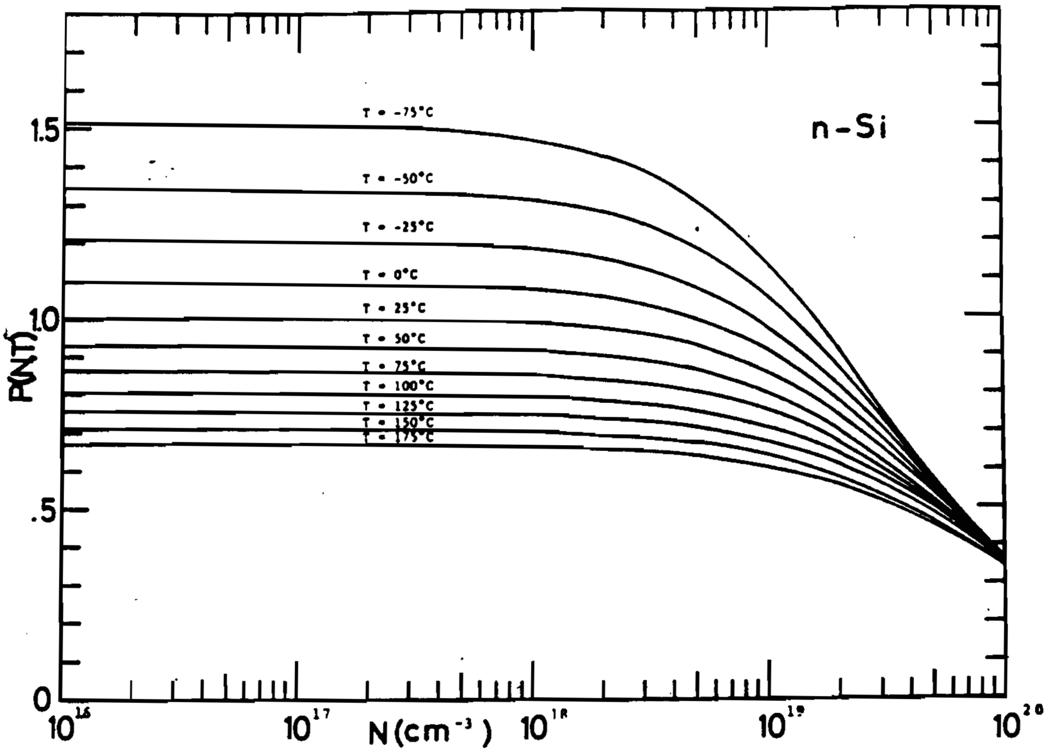


Fig. 8. Piezoresistance factor $P(N, T)$ as a function of impurity concentration and temperature for n-Si.

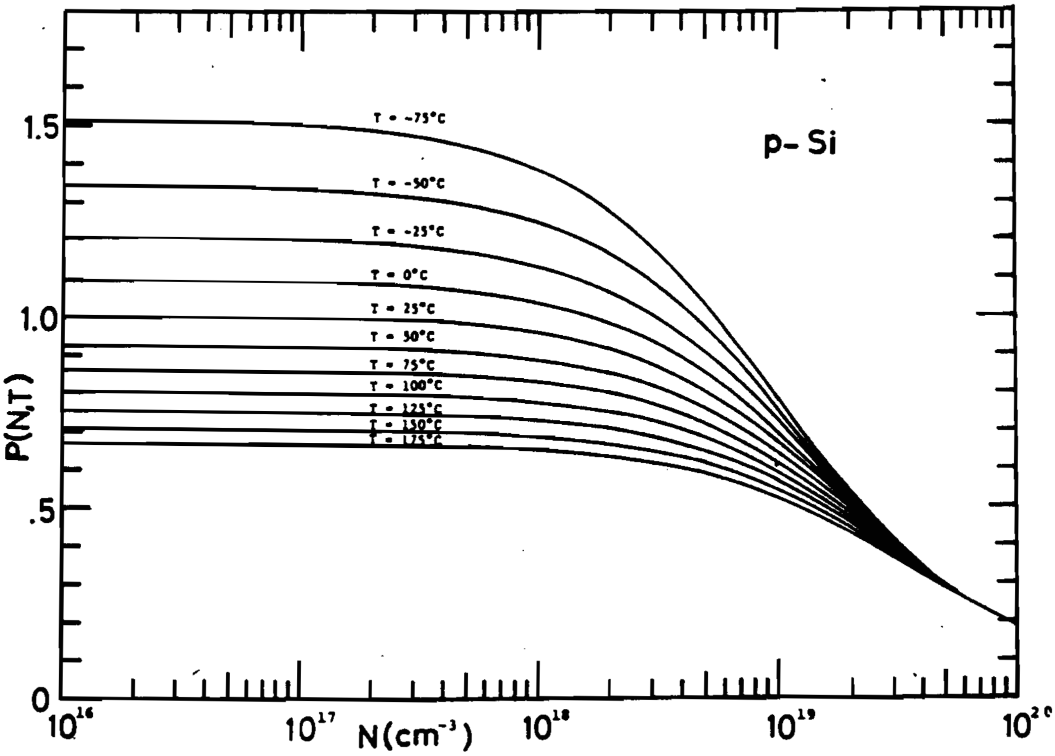


Fig. 9. Piezoresistance factor $P(N, T)$ as a function of impurity concentration and temperature for p-Si.

STRAIN GAUGE DESIGN (CONTINUED)

NOTICE THAT

(I) THE TEMPERATURE EFFECT BECOMES LESS WITH INCREASING DOPING, BUT IS STILL SIGNIFICANT (ABOUT 0.2 % PER DEGREE C) AT CONCENTRATIONS OF INTEREST (1xE19 TO 1xE20 /CM^3).

(II) π_{ij} BECOMES LESS WITH INCREASING TEMPERATURE AND DOPING.

THE DIRECTIONAL ASPECTS OF THE PIEZORESISTIVE PHENOMENON MAY BE STUDIED BY CONSIDERING THE RESPONSE OF A DIFFUSED RESISTOR TO LONGITUDINAL AND TRANSVERSE TENSILE STRESSES AS IT IS IMAGINED TO ROTATE IN A GIVEN CRYSTAL PLANE. REF. 14 HAS SOME NICE POLAR PLOTS...

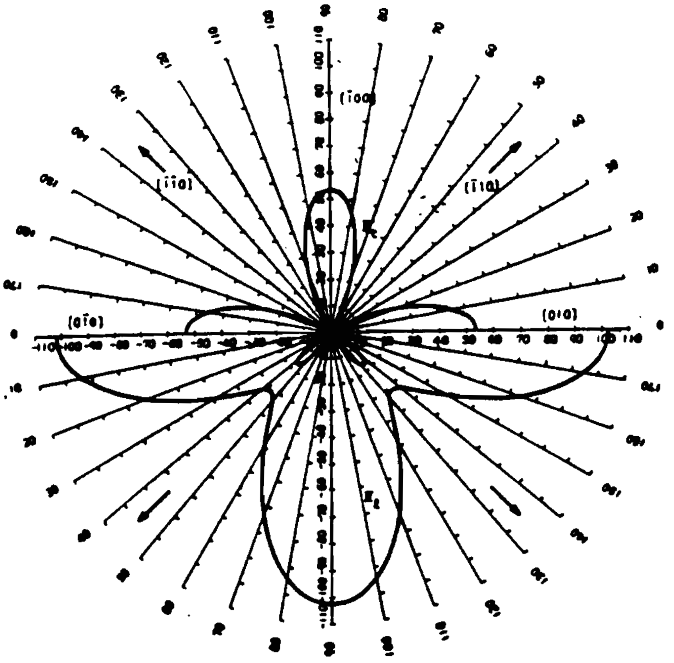


Fig. 2. Room temperature piezoresistance coefficients in the (001) plane of n-Si (10^{-12} cm^2/dyne).

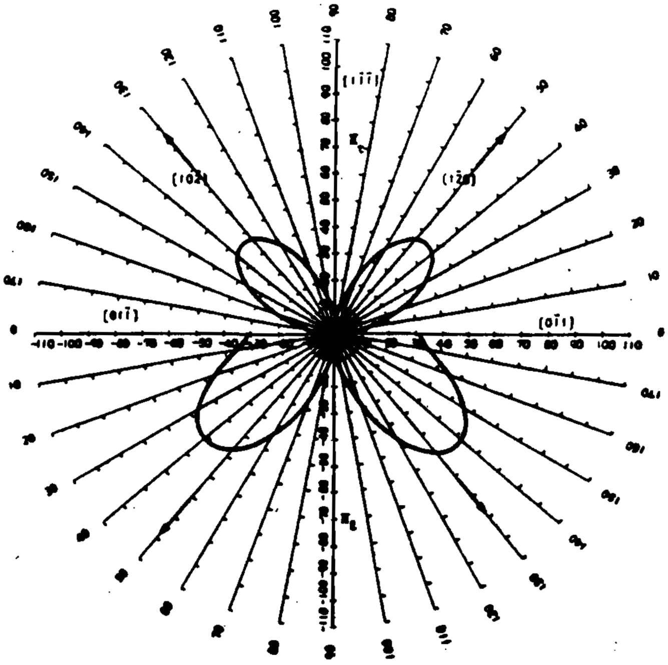


Fig. 4. Room temperature piezoresistance coefficients in the (211) plane of n-Si (10^{-12} cm^2/dyne).

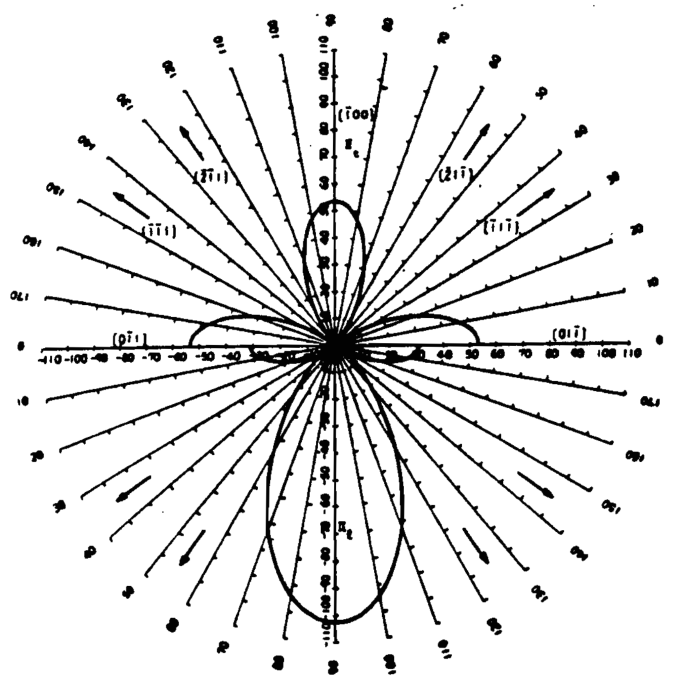


Fig. 3. Room temperature piezoresistance coefficients in the (011) plane of n-Si (10^{-12} cm^2/dyne).

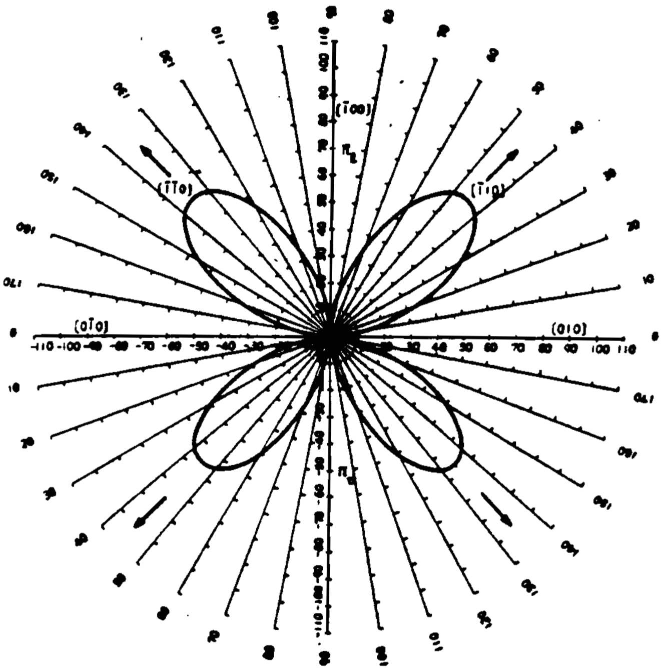


Fig. 5. Room temperature piezoresistance coefficients in the (001) plane of p-Si (10^{-12} cm^2/dyne).

STRAIN GAUGE DESIGN (CONTINUED)

APPLICATION:

TYPICALLY, ONE USES THREE OR FOUR RESISTORS ALIGNED ALONG MAJOR CRYSTALLOGRAPHIC DIRECTIONS. GENERALLY IT CAN BE ASSUMED THAT ONLY STRESSES IN THE PLANE OF THE DIE ARE SIGNIFICANT, SO ONLY σ_1 , σ_2 AND τ_{12} ARE NON-ZERO. A TYPICAL STRAIN GAUGE BUILT INTO THE (001) SURFACE OF A CHIP WOULD APPEAR AS FOLLOWS.

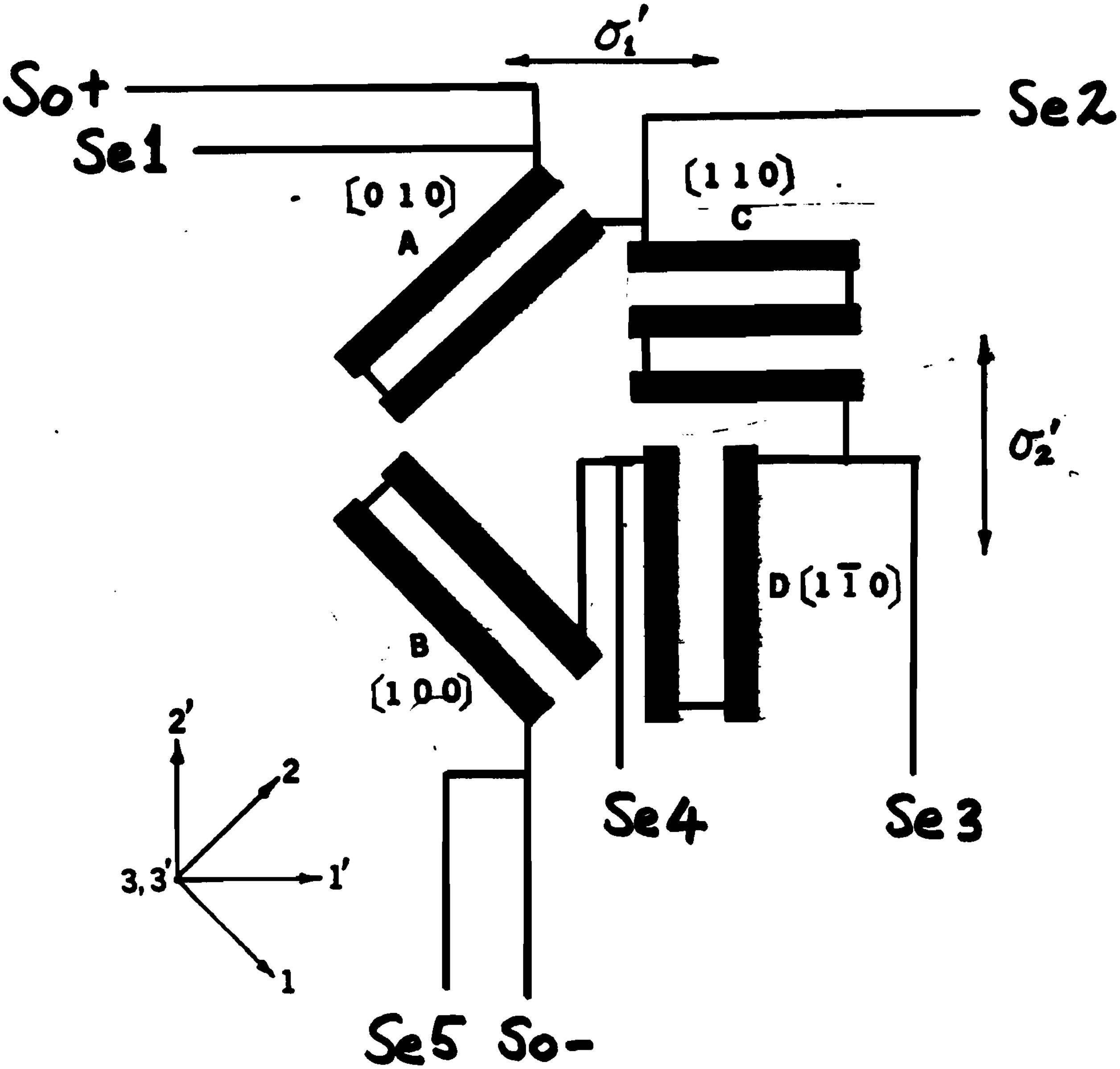

σ1'
So+
Se1
Se2
(1 1 0)
C
[0 1 0)
A
σ2'
D (1 1̄ 0)
B
(1 0 0)
2'
2
3,3'
1'
1
Se4
Se3
Se5
So-

Figure 1. Crystallographic orientations of the resistor rosette and the two coordinate systems.

STRAIN GAUGE DESIGN (CONTINUED)

IT CAN BE SHOWN FROM (1) THAT

$$\Delta R_A/R_A = \frac{1}{2}(\pi_{11}+\pi_{12})(\sigma_1'+\sigma_2') + (\pi_{11}-\pi_{12})\tau_{12}' \quad \text{(3A)}$$

$$\Delta R_B/R_B = \frac{1}{2}(\pi_{11}+\pi_{12})(\sigma_1'+\sigma_2') - (\pi_{11}-\pi_{12})\tau_{12}' \quad \text{(3B)}$$

$$\Delta R_C/R_C = \frac{1}{2}(\pi_{11}+\pi_{12}+\pi_{44})\sigma_1' + \frac{1}{2}(\pi_{11}+\pi_{12}-\pi_{44})\sigma_2' \quad \text{(3C)}$$

$$\Delta R_D/R_D = \frac{1}{2}(\pi_{11}+\pi_{12}-\pi_{44})\sigma_1' + \frac{1}{2}(\pi_{11}+\pi_{12}+\pi_{44})\sigma_1' \quad \text{(3D)}$$

THE STRESSES (PRIMED) ARE REFERRED TO X- AND Y- AXES OF THE CHIP, WHICH LIE ALONG 110 DIRECTIONS, WHEREAS THE PIEZORESISTANCE COEFFICIENTS ARE REFERRED TO THE CUBIC AXES OF THE CRYSTAL, WHICH LIE ALONG 100 DIRECTIONS.

SO MEASUREMENT OF THE FOUR FRACTIONAL RESISTANCE CHANGES OVERDETERMINES THE STRESSES. SO A CONSISTENCY CHECK IS AVAILABLE IN CASE RESISTANCE CHANGES ARE DUE TO EFFECTS OTHER THAN STRESS.

VALUES OF PIEZORESISTANCE COEFFICIENTS HAVE BEEN MEASURED BY MANY WORKERS (REFS. 15-20).

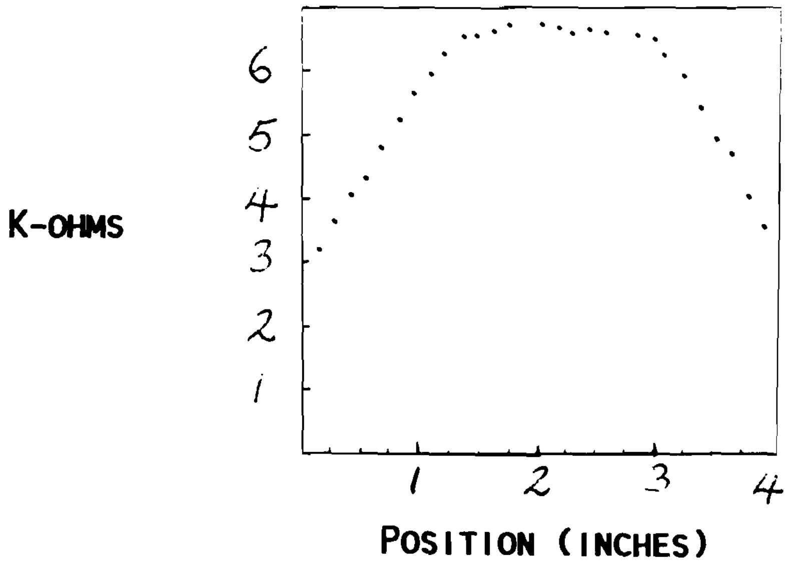
STRAIN GAUGE DESIGN (CONTINUED)

MEASUREMENT ISSUES:

- O TYPICAL RESISTANCE CHANGES DUE TO DIE ATTACH ARE FRACTIONS OF A PERCENT, UP TO ABOUT 2 PERCENT.

- O TEMPERATURE OF BEFORE AND AFTER MEASUREMENTS MUST NOT DIFFER BY MORE THAN A DEGREE OR SO. RESISTANCE CHANGES DUE TO TEMPERATURE ARE TYPICALLY 0.2% PER DEGREE C.

- O IDENTITY MUST BE TRACKED BECAUSE THE WAFER-TO-WAFER AND ACROSS-WAFER VARIATION OF RESISTANCE CAN BE AS MUCH AS 100%.



- O A HIGH-RESOLUTION (5 1/2 DIGIT) DVM SHOULD BE USED, AND THE MEASUREMENTS SHOULD BE 4-POINT.

- O BEWARE OF RESISTANCE CHANGES DUE TO EFFECTS OTHER THAN STRESS. ESPECIALLY IF DICE SEE TEMPERATURES GREATER THAN ABOUT 440 DEG C.

STRAIN GAUGE DESIGN (CONTINUED)

PROBLEMS:

DERIVE EQUATIONS (3) FROM EQUATION (1).

DERIVE A SIMPLE CONDITION ON $\Delta R_A/R_A$ ETC. WHICH CHECKS THE CONSISTENCY OF EQUATIONS (3).

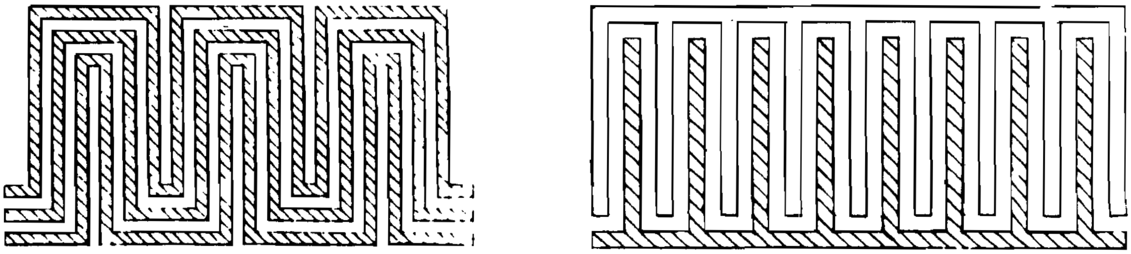
WHAT ARE THE PROBLEMS IN DETERMINING THE TRANSIENT STRESSES DUE TO THERMAL SHOCK USING A PIEZORESISTIVE STRAIN GAUGE?

HOW MANY SQUARES SHOULD A STRESS-SENSITIVE RESISTOR BE?

MOISTURE SENSING ELEMENT DESIGN

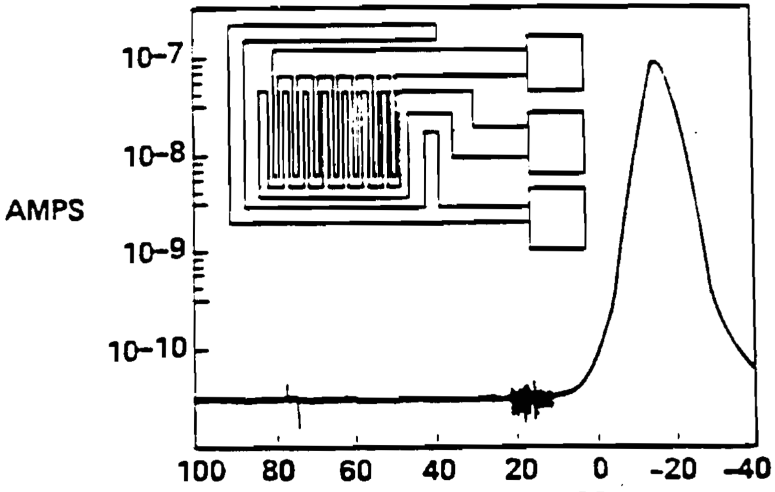
SCOPE:

- o TO DETECT THE EFFECT OF MOISTURE AND IONIC CONTAMINANTS.
- o MEASUREMENTS CAN BE DC OR AC.
- o USE A TRIPLE TRACK FOR DC.
- o USE INTERLEAVED STRUCTURE FOR AC.



- o THE ELEMENTS CAN BE PASSIVATED OR UNPASSIVATED. WE WILL FOCUS ON PASSIVATED ELEMENTS.
- o GOOD REVIEWS OF SURFACE CONDUCTION DUE TO MOISTURE CAN BE FOUND IN REFS. 6, 7, AND 22. THIS MUST BE CONSIDERED IN DESIGN OF SENSORS.
- o SOMETIMES ADJACENT METAL TRACKS ARE USED MERELY TO DETECT CONDENSATION. THIS IS A MUCH LESS DEMANDING MEASUREMENT PROBLEM. REF. 8 IS A GOOD EXAMPLE.

SURFACE CONDUCTIVITY SENSOR



MOISTURE SENSING ELEMENT DESIGN (CONTINUED)

DC MEASUREMENTS USING TRIPLE TRACKS:

- SUSTAIN 100 V BETWEEN CENTER AND OUTER CONDUCTOR.
- USE MINIMUM SPACING TO MAXIMIZE ELECTRIC FIELD (TYPICALLY CAN GET 1XE5 V/CM).
- DESIGN SUCH THAT CURRENTS WILL BE GREATER THAN 1 PA.
- SURFACE (OR INTERFACE) CURRENTS USUALLY DOMINATE. THAT IS,

RHO(BULK) [OHM-CM] > RHO(SURFACE) [OHM/SQUARE] X T [CM]

TYPICAL RHO(BULK) AT 23 DEG C AND E ABOUT 1XE6 V/CM (REF. 9):

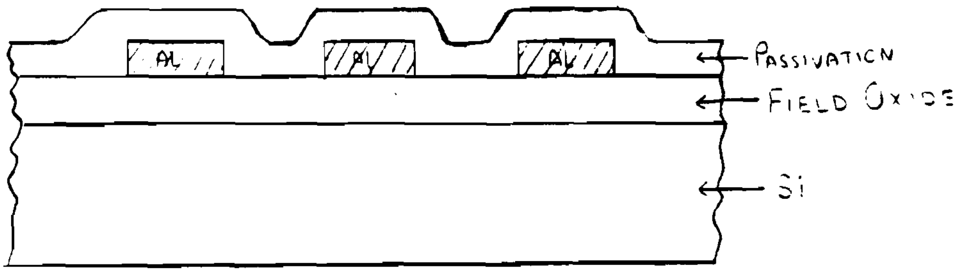
MATERIAL	DEPOSITION PROCESS	RHO(BULK) [OHM-CM]
SI3N4	PLASMA SIH4 + NH3 SUBST 300 DEG C	1.0XE15
SIO2	CVD, SIH4 + O2 AT 450 DEG C	3.3XE15
PSG	CVD, SIH4 + O2 + PH3 AT 450 DEG C	6.6XE16

TYPICAL RHO(SURFACE) AT 23 DEG C AND ABOUT 1XE5 V/CM (REF. 10):

MATERIAL	RELATIVE HUMIDITY (%)	RHO(SURF) [OHMS/SQ]
CVD SIO2	30	8.9XE16
CVD SIO2	50	1.4XE15
CVD SIO2	70	3.5XE13
CVD SIO2	90	2.8XE12

TENDS TO BE INDEPENDENT OF MATERIAL AND DEPOSITION CONDITIONS (SEE ALSO REFS 6 AND 7).

SO FOR TYPICAL PASSIVATION THICKNESSES (T = 1XE-4 CM) THE ABOVE INEQUALITY IS USUALLY EASILY SATISFIED.



MOISTURE SENSING ELEMENT DESIGN (CONTINUED)

EXAMPLE:

WHAT LENGTH OF 10 MICRON SPACING TRIPLE-TRACK WOULD BE NEEDED TO HAVE A SIGNAL CURRENT OF 1 PA AT 30 % R.H. FOR A 1 MICRON THICK PSG FILM?

SHEET RESISTIVITY DUE TO SURFACE IS 9xE16 (OHM/SQ). THE PARALLEL SHEET RESISTIVITY DUE TO THE BULK IS 7xE20 (OHM/SQ). ASSUME 100 VOLTS, SO E=1xE5 V/CM. SO CURRENT PER UNIT LENGTH LEAVING CENTER CONDUCTOR IS

J = 2 X E/RHO (SHEET) = 2 X E5 / 9xE16 = 2.2 X E-12 A/CM

(FACTOR OF TWO ACCOUNTS FOR TWO CURRENT PATHS). SO REQUIRED LENGTH IS

L = 1 X E-12/2.2 X E-12 = .45 CM

MOISTURE SENSING ELEMENT DESIGN (CONTINUED)

AC MEASUREMENTS USING INTERLEAVED STRUCTURES:

O THE BEST PRACTICAL APPROACH IS DUE TO MERRETT, SIM AND BRYANT (REF. 11).

O THEY ALSO ASSUME THAT BULK CONDUCTION IS NEGLIGIBLE.

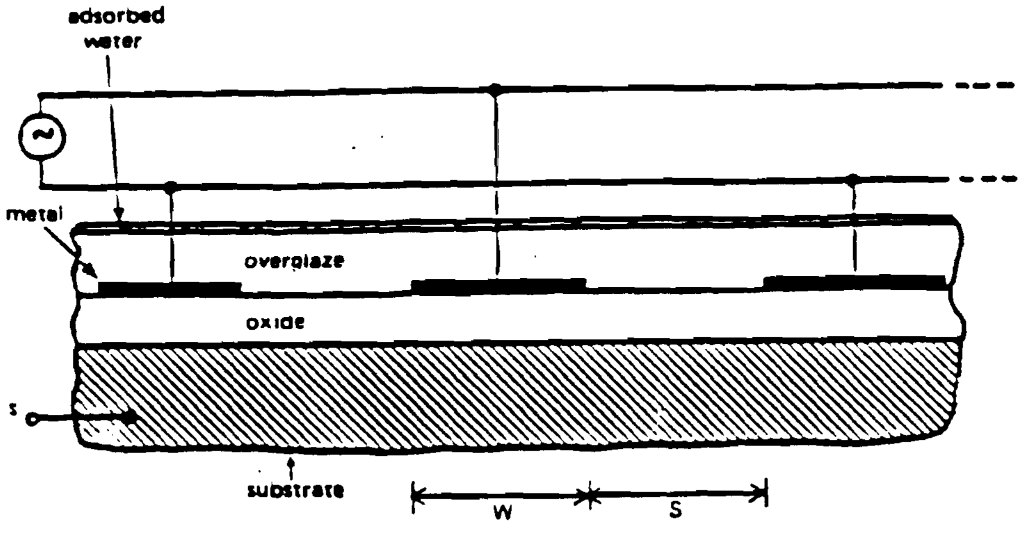
O THEY ASSUME THAT THE ELEMENTS ARE PASSIVATED.

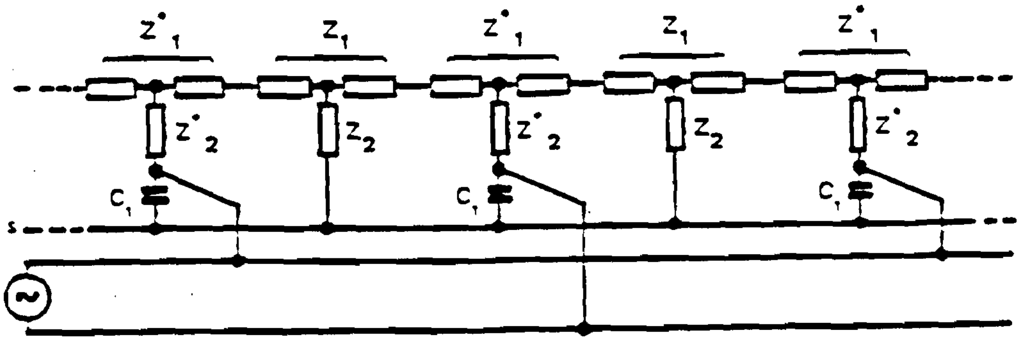
O THERE IS NO NEED TO USE HIGH VOLTAGE.

O THE TECHNIQUE WORKS ON REAL DEVICES, AS WELL AS ON TEST CHIPS.

O THEY MEASURE THE CAPACITANCE, CM, BETWEEN THE TWO SETS OF TRACKS. CM IS THE SUM OF CI, THE (CONSTANT) INHERENT CAPACITANCE, AND CW, THE CAPACITANCE DUE TO WATER.

O THE INTERLEAVED STRUCTURE CAN BE MODELED AS AN AC NETWORK AS FOLLOWS:


adsorbed water
metal
overglaze
oxide
s
substrate
W
S


Z^*_1
Z_1
Z^*_1
Z_1
Z^*_1
Z^*_2
Z_2
Z^*_2
Z_2
Z^*_2
C_1
C_1
C_1
s

MOISTURE SENSING ELEMENT DESIGN (CONTINUED)

O AC NETWORK ANALYSIS SHOWS THAT C_W IS GIVEN VIA THE CAPACITANCE RATIO

$$\frac{C_w}{C_i} = \left\{ \frac{1}{C_t W} \sqrt{\frac{2 \sigma C_o}{\omega}} \right\} (1+Y)^{1/2} \qquad (1)$$

WHICH HOLDS WHEN THE CONDITION

$$S \sqrt{\frac{\omega C_o}{2 \sigma}} \geq 4 \qquad (2)$$

IS SATISFIED. IN EQUATIONS (1) AND (2),

C_O IS THE CAPACITANCE PER UNIT AREA BETWEEN THE CONDUCTING FILM AND THE SUBSTRATE,

C_T IS THE CAPACITANCE PER UNIT AREA BETWEEN THE TRACKS AND THE SUBSTRATE,

Y IS THE THICKNESS OF THE PASSIVATION DIVIDED BY THE TOTAL THICKNESS OF THE PASSIVATION AND THE OXIDE UNDER THE TRACKS,

σ IS THE SHEET CONDUCTIVITY OF THE WATER FILM,

S AND W ARE, RESPECTIVELY, THE SPACING AND WIDTH OF THE INTERLEAVED ALUMINUM LINES.

O NOTE THE FOLLOWING FEATURES

- THE SURFACE CONDUCTIVITY IS THE ONLY SURFACE-SENSITIVE PARAMETER.
- NEITHER THE SPACING, NOR THE LENGTH OF THE LINES ARE INVOLVED, SO THE EQUATION IS VALID FOR ANY METALLIZATION PATTERN.
- MOST STRUCTURES HAVE COMPARABLE VALUES OF C_O, C_T, Y, AND W SO THE VALUE OF THE CAPACITANCE RATIO IS PRIMARILY DEPENDENT ON THE SURFACE CONDUCTIVITY.
- THE CAPACITANCE RATIO VARIES INVERSELY AS THE SQUARE ROOT OF FREQUENCY, SO THE CONTRIBUTION ABSORBED WATER MAKES TO THE MEASURED CAPACITANCE DECREASES AS THE FREQUENCY IS INCREASED.

MOISTURE SENSING ELEMENT DESIGN (CONTINUED)

O MEASUREMENT NOTES:

- A GOOD FREQUENCY TO USE IS A COMPROMISE BETWEEN MAKING (1) LARGE ENOUGH TO MEASURE, AND SATISFYING (2). A GOOD CHOICE IS 100 HZ.

- TO ISOLATE CW, MAKE TWO MEASUREMENTS: ONE AT A FREQUENCY SUFFICIENTLY HIGH TO ELIMINATE THE EFFECT OF CW, AND ONE AT 100HZ. THEN

CW/CI = [C(100HZ) - C(INFINITY)]/C(INFINITY)

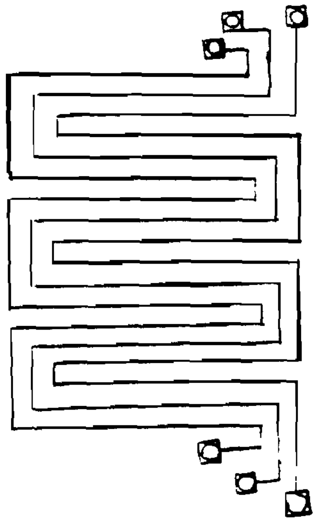
PROBLEMS:

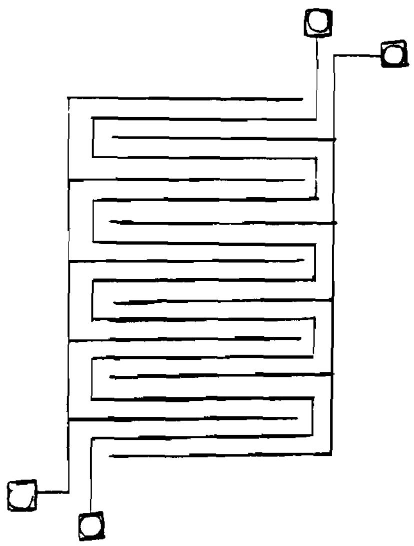
HOW WOULD THE CAPACITANCE RATIO BE EXTRACTED IF THE HIGHEST FREQUENCY AVAILABLE COULD NOT MAKE CW NEGLIGIBLE?

WOULD A CONDUCTANCE MEASUREMENT BE MORE SUITABLE?

IS THERE AN UPPER LIMIT ON THE SPACING OF THE INTERLEAVED STRUCTURE?

WHICH OF THE FOLLOWING STRUCTURES MAKES MORE EFFICIENT USE OF REAL-ESTATE? BY WHAT FACTOR? DOES THE MORE AREA-EFFICIENT ONE HAVE ANY DISADVANTAGES RELATIVE TO THE OTHER?





5. DESIGN GUIDELINES

- REVIEW OF OBJECTIVES
- GUIDELINES

5. DESIGN GUIDELINES

A REMINDER OF OUR OBJECTIVES:

- USE THE TEST CHIPS TO CHARACTERIZE AND QUALIFY NEW WAFER AND ASSEMBLY PROCESSES.
- EXPERIMENTS WILL INVOLVE HUNDREDS OF PIECES TO GIVE A STATISTICAL CHARACTERIZATION OF PROCESSES.
- FACTORY (UNSKILLED) ASSEMBLY SHOULD BE EASY. DESIGN RULES SHOULD BE FOLLOWED.
- USE AN AUTOMATIC PARAMETRIC TESTER WITH SOFTWARE-CONTROLLED SWITCHING MATRIX.
- BUILD A QUALITY AND RELIABILITY DATA BASE BASED ON A FEW WELL-CHARACTERIZED SENSORS.

5. DESIGN GUIDELINES (CONTINUED)

EXPERIENCE HAS GENERATED THE FOLLOWING DESIGN GUIDELINES:

IN ORDER OF PRIORITY...

(A) THE DIE SIZE SHOULD BE ADJUSTABLE. IT MUST BE POSSIBLE TO SIMULATE THE DIE SIZE OF ANY PRODUCT CHIP.

(B) THE TEST CHIP MUST OBEY WAFER FAB AND ASSEMBLY (ESPECIALLY WIRE-RELATED) DESIGN RULES.

(C) THE TEST CHIP MUST BE TESTABLE AT THE WAFER LEVEL.

(D) TEST CHIPS MUST HAVE VERY HIGH WAFER FAB YIELD.

(E) A GIVEN TEST CHIP SHOULD BE MANUFACTURABLE ON ANY WAFER FAB PROCESS.

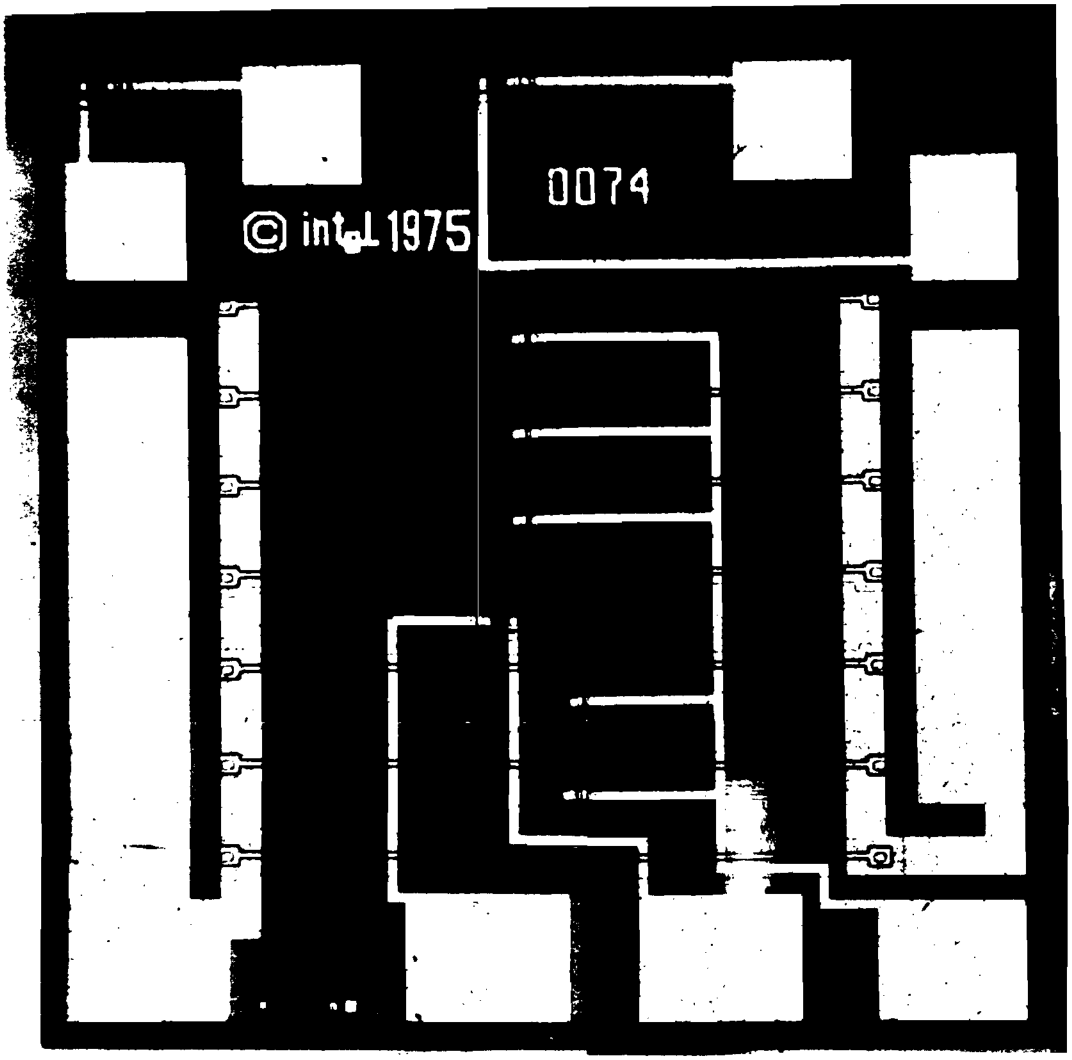
(F) FOR TEST CHIPS THAT USE A PARAMETRIC SHIFT AS AN INDICATION (EG. STRESS MEASUREMENTS, OR THERMAL DEGRADATION) IT IS DESIRABLE TO MAINTAIN CHIP IDENTITY THROUGH ASSEMBLY WITHOUT SPECIAL ATTENTION.

(G) IT IS DESIRABLE TO BE ABLE TO PRODUCE A MAP OF ENVIRONMENTAL PARAMETERS ACROSS THE CHIP SURFACE.

6. CASE STUDIES

- THERMAL TEST CHIP
- CRACK DETECTION CHIP
- STRESS MEASUREMENT
- MOISTURE SENSING TEST CHIP
- CASE STUDY SUMMARY

THERMAL IMPEDANCE CHIP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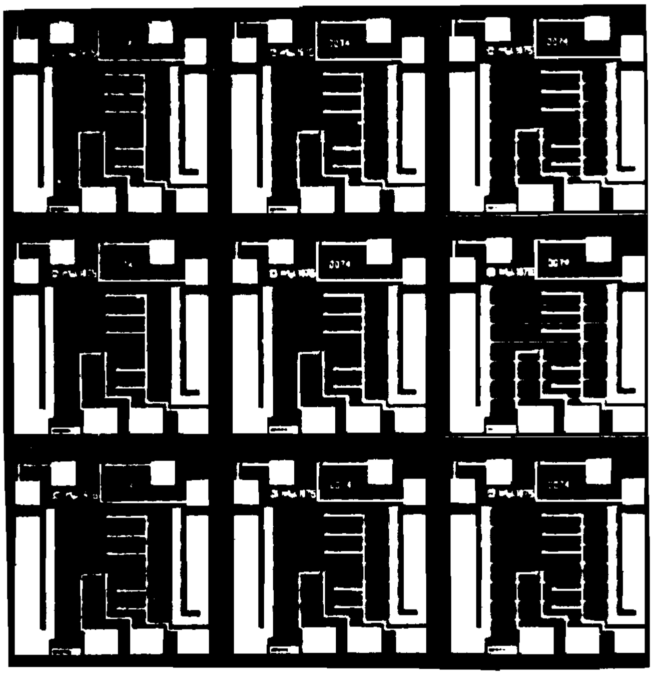


THERMAL TEST CHIP

FEATURES:

- O VARIABLE DIE SIZE.
- O VARIABLE DISSIPATION AND TEMPERATURE SENSE DISTRIBUTION.

BUT

PROBLEMS:

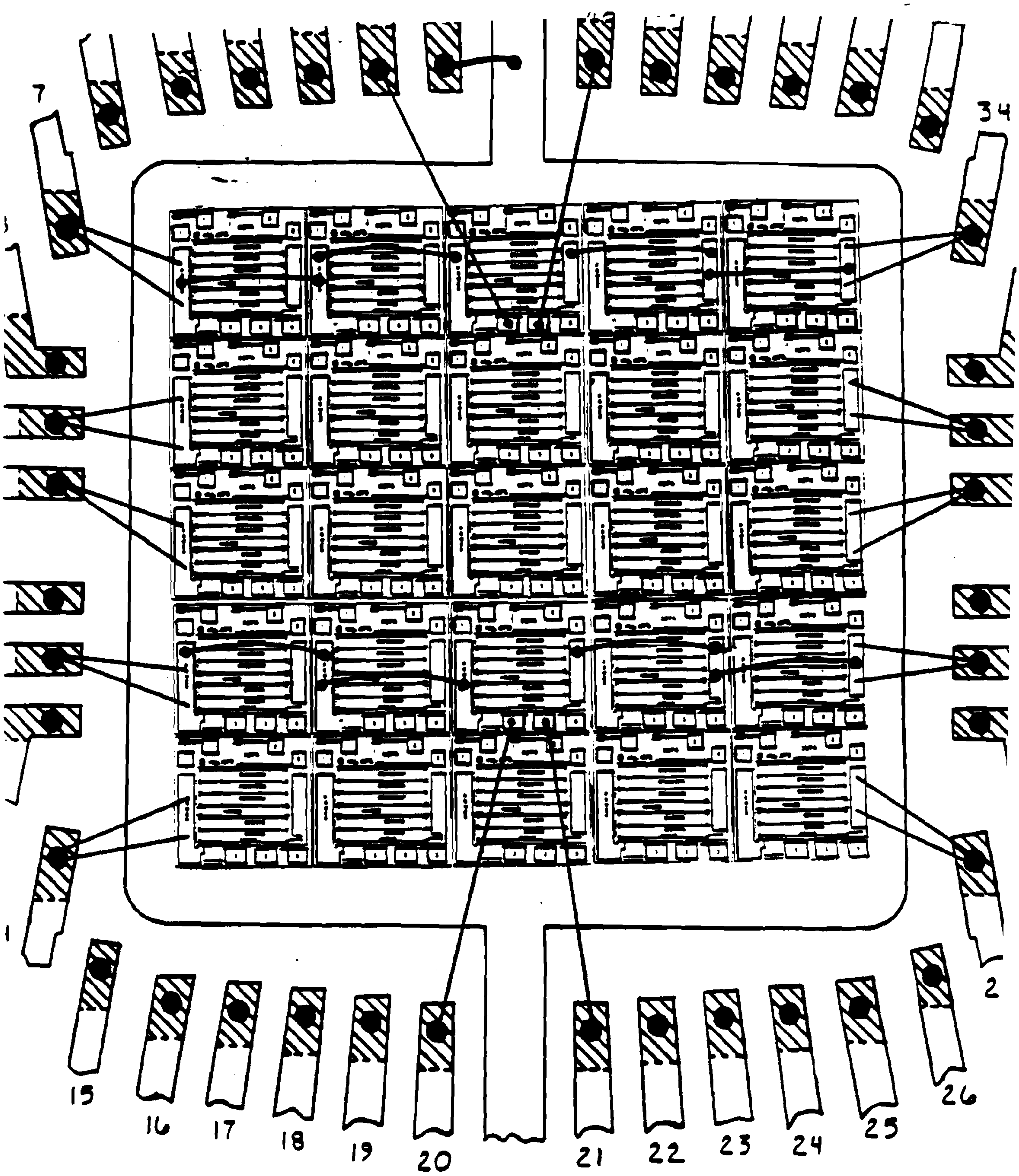
- O VARIABLE DISTRIBUTION IS ACHIEVED THROUGH WIREBOND PLACEMENT, LEADING TO DESIGN RULE VIOLATIONS:
  - - WIRE OVER EDGE
  - - ON-CHIP BONDS

SOLUTIONS:

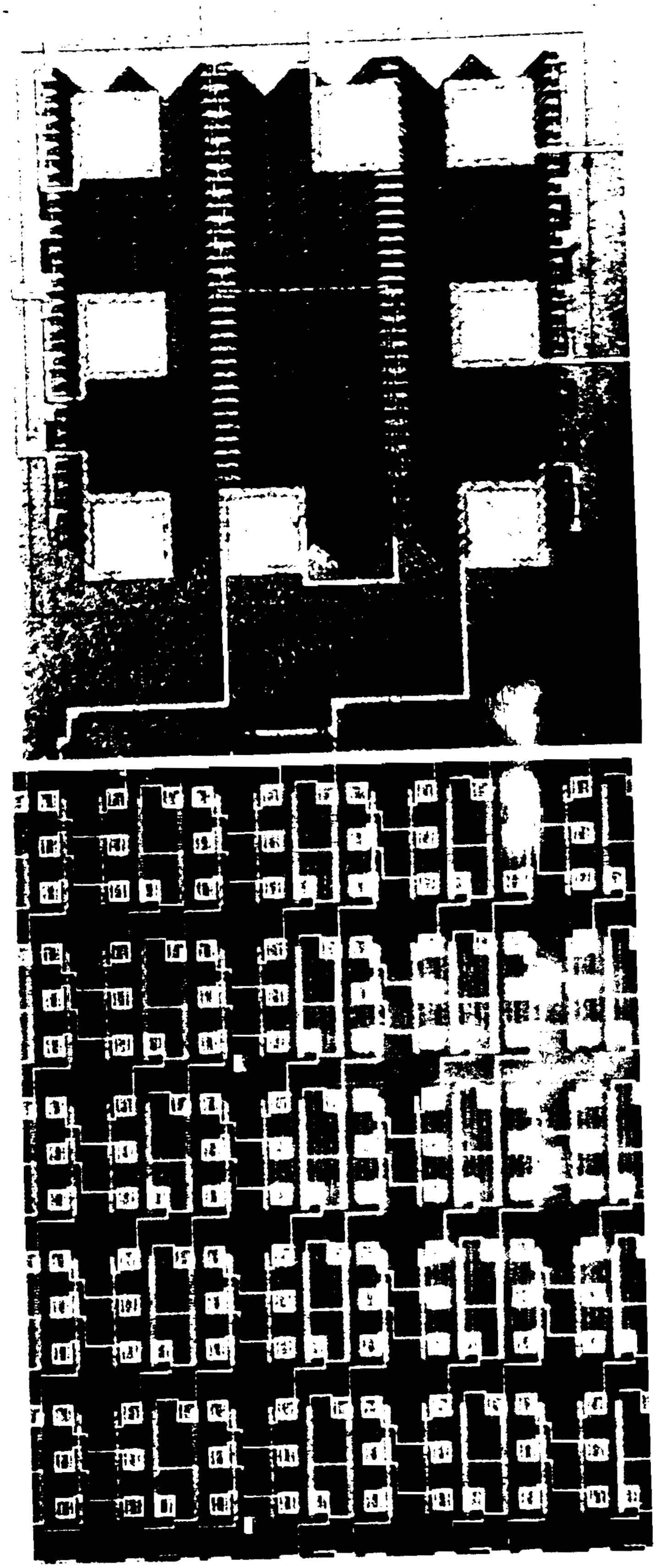
- O LINK POWER RESISTORS ACROSS SCRIBE GRID.
- O LINK SENSE DIODES, OR MULTIPLEX.

DESIGN GUIDELINE EVALUATION:

A. ADJUSTABLE DIE SIZE	YES
C. OBEY DESIGN RULES	ASSEMBLY NO, FAB YES.
C. WAFER TESTABLE	YES
D. HIGH FAB YIELD	YES
E. ANY FAB PROCESS	YES
F. ELECTRICAL ID	NO
G. DIE SURFACE MAPS	CRUDE



CRACK DETECTION CHIP



CRACK DETECTION CHIP

FEATURES:

- o ELECTRICAL MAPPING OF DIE CRACKS DUE TO DIE ATTACH OR WIREBOND.
- o JUNCTIONS SENSITIVE TO THERMAL HISTORY.
- o DIE-OFF DETECTION.

PROBLEMS:

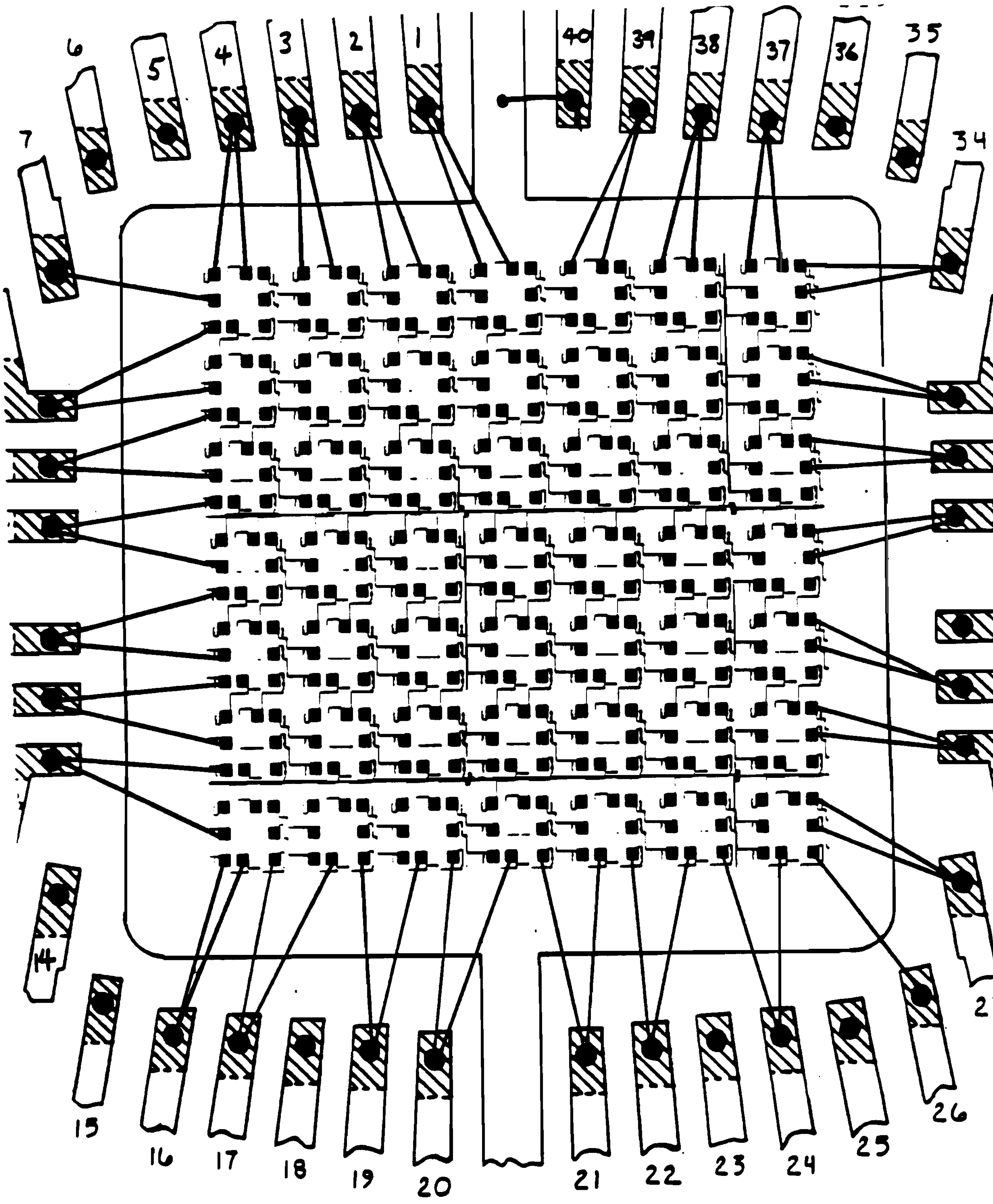
- o HARD TO TEST AT THE WAFER LEVEL.
- o RESISTORS TOO HIGH IN VALUE (ABOUT 4K OHM).
- o BOND PADS VIOLATE DESIGN RULES (ALUMINUM OVER POLYSILICON).

SOLUTIONS:

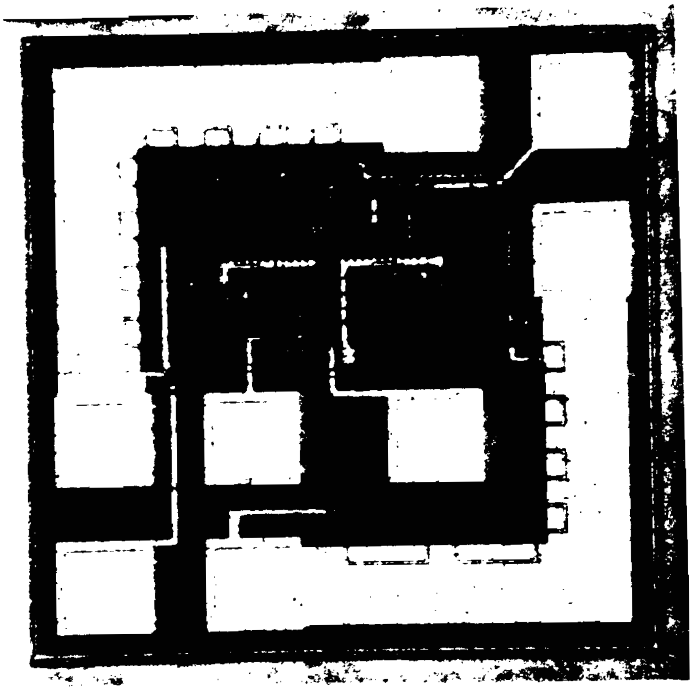
- o PUT FUSES IN SCRIBE LINES.
- o FATTEN UP RESISTORS.
- o USE DIFFERENT SENSORS UNDER BOND PADS TO DETECT FRACTURE DUE TO WIRE BONDING.

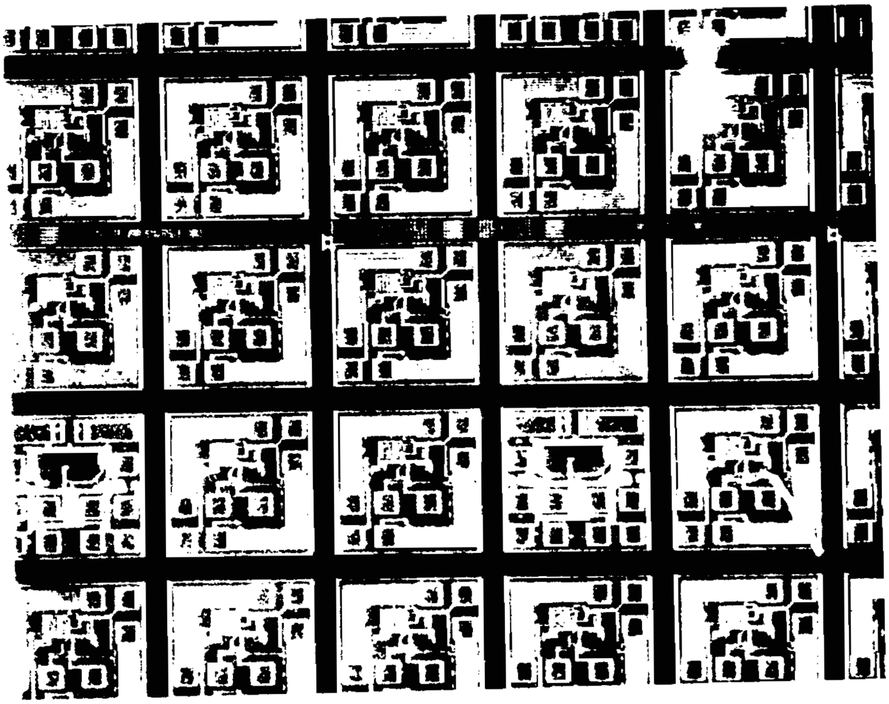
DESIGN GUIDELINE EVALUATION:

A. ADJUSTABLE DIE SIZE?	YES
B. OBEY DESIGN RULES?	ASSEMBLY YES, FAB NO
C. WAFER TESTABLE?	NO
D. HIGH FAB YIELD	YES
E. ANY FAB PROCESS	YES
F. ELECTRICAL ID	NO
G. DIE SURFACE MAPS	YES



STRESS MEASUREMENT CHIP





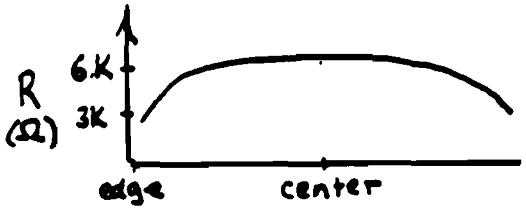
STRESS MEASUREMENT

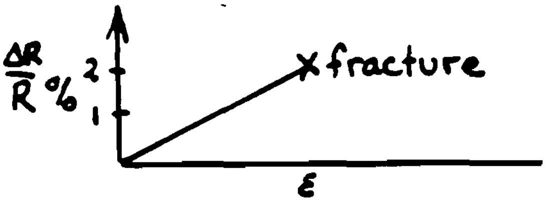
FEATURES:

- FOUR-RESISTOR, FOUR POINT STRAIN ROSETTE.
- FAB DESIGN VARIATION.
- DIODES FOR TEMPERATURE MEASUREMENT.
- PARAMETRIC MEASUREMENTS.

PROBLEMS:

- LARGE NUMBER OF PADS PER SUBDIE. LEADS TO AWKWARD PAD LOCATIONS AND WIRE BOND DESIGN RULE VIOLATIONS.
- PROCESS VARIATIONS ACROSS WAFER OF STRAIN GAUGE RESISTORS ARE GREATER THAN THE PARAMETRIC SHIFTS TO BE DETECTED. HENCE MANUAL IDENTITY TRACKING IS NECESSARY.





- PRODUCING ONE VARIANT IS DIFFICULT - EITHER WASTE SILICON, DO VISUAL SORTING, OR DO COMPLICATED MULTI-PASS SAWING.
- MANY SENSORS CANNOT BE REACHED BY WIRES. MAPPING PARAMETERS ACROSS THE DIE IS PRACTICALLY IMPOSSIBLE.

SOLUTIONS:

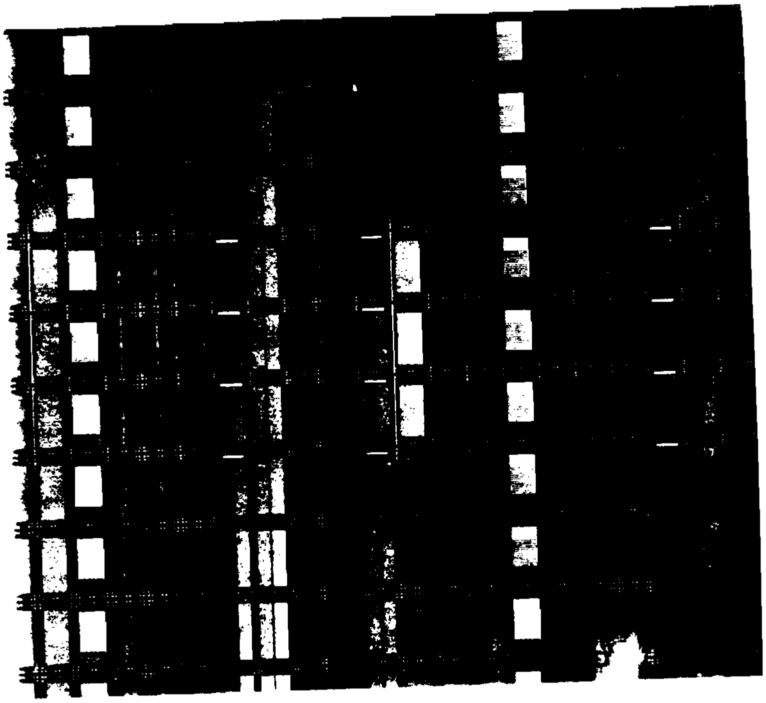
- MAKE SUBDIE LARGER AND PUT PADS ONLY ON ITS PERIPHERY.
- MAKE PROVISION FOR ELECTRICAL DIE IDENTITY.
- MAKE EACH SUBDIE IDENTICAL. ALL FUNCTIONS ON EACH DIE.
- LOCAL AMPLIFICATION OF SIGNALS, MULTIPLEX TO PERIPHERY VIA CONNECTIONS ACROSS SCRIBE LINES.

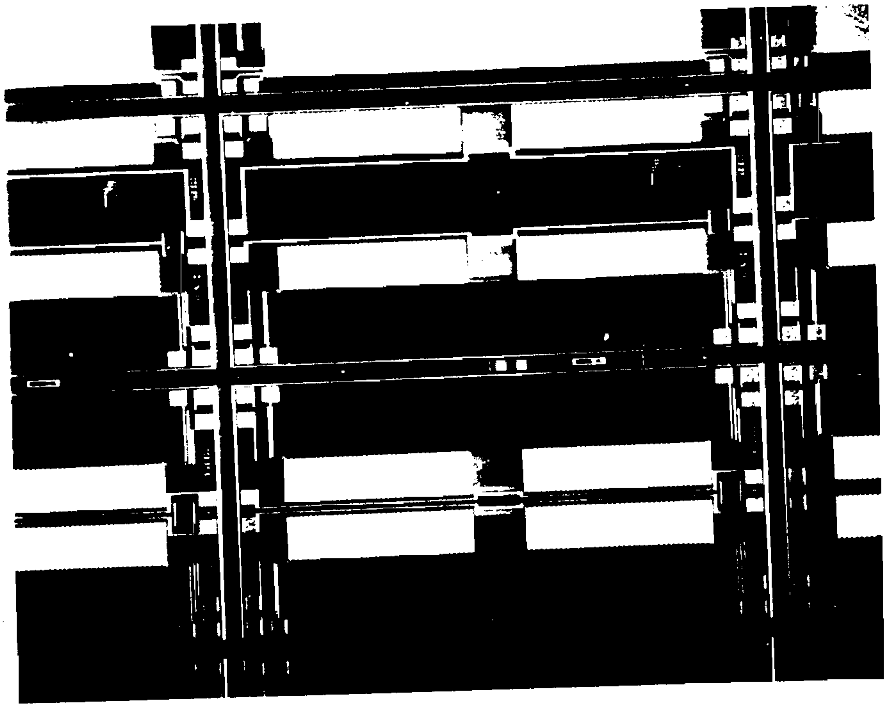
STRESS MEASUREMENT (CONTINUED)

DESIGN GUIDELINE EVALUATION:

A. ADJUSTABLE DIE SIZE?	YES(?)
B. OBEY DESIGN RULES?	ASSEMBLY NO, FAB YES
C. WAFER TESTABLE?	YES
D. HIGH FAB YIELD	YES
E. ANY FAB PROCESS	YES
F. ELECTRICAL ID	VARIANT ONLY
G. DIE SURFACE MAPS	NO

MOISTURE/CORROSION SENSING CHIP





MOISTURE SENSING TEST CHIP

FEATURES:

- o SIMULATES A SPECIFIC CHIP (16K DRAM).
- o HAS 12 VARIANTS WITH VARIOUS MOISTURE-SENSITIVE STRUCTURES.
- o PROVISION FOR ELECTRICAL IDENTIFICATION OF VARIANT.
- o SENSORS USED ARE TRIPLE TRACKS AND MOS CAPACITORS.

PROBLEMS:

- o SPECIFIC TO ONE TYPE OF CHIP.
- o DIE SIZE TOO LARGE (180 X 90 MILS) TO USE AS MODULE IN "ADJUSTABLE" CHIP.
- o TOO MANY VARIANTS ON ONE WAFER.

SOLUTION:

- o A COMPLETELY DIFFERENT DESIGN IS NEEDED TO IMPLEMENT THE SENSORS IN OUR METHODOLOGY.

DESIGN GUIDELINE EVALUATION:

A. ADJUSTABLE DIE SIZE?	NO
B. OBEY DESIGN RULES?	ASSEMBLY YES, FAB YES
C. WAFER TESTABLE?	YES
D. HIGH FAB YIELD	YES
E. ANY FAB PROCESS	YES
F. ELECTRICAL ID	NO
G. DIE SURFACE MAPS	YES

CASE STUDY SUMMARY

GUIDELINE	THERMAL	CRACK	STRESS	MOISTURE
A. ADJUSTABLE DIE SIZE	YES	YES	YES(?)	NO
B. OBEYS DESIGN RULES				
- ASSEMBLY	NO	YES	NO	YES
- FAB	YES	NO	YES	YES
C. WAFER TESTABLE	YES	NO	YES	YES
D. HIGH FAB YIELD	YES	YES	YES	YES
E. ANY FAB PROCESS	YES	YES	YES	YES
F. ELECTRICAL ID	NO	NO	VARIANT	VARIANT
G. DIE SURFACE MAPS	CRUDE	YES	NO	YES

THE PRIMARY CHALLENGE IS TO PUT YES IN ALL OF THE FIRST THREE GUIDELINES

7. DESIGN SOLUTIONS

- o WE NEED TO SATISFY THE FOLLOWING SIMULTANEOUSLY:

  A. ADJUSTABLE DIE SIZE

  B. OBEY DESIGN RULES.

  C. CHIPS TESTABLE AT THE WAFER LEVEL

  HOW DO WE DO IT?

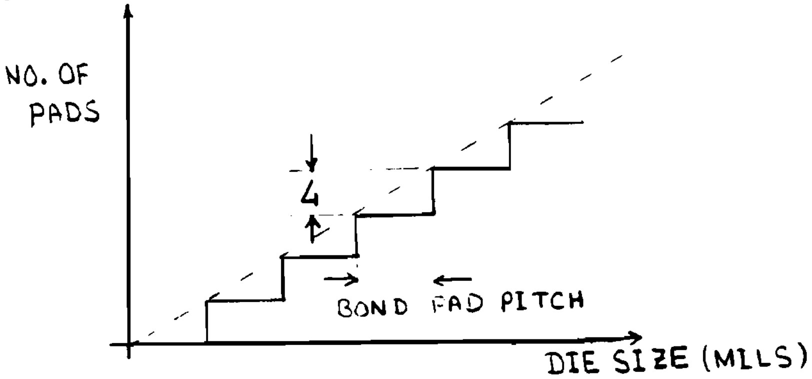
- o BONDING PAD PLACEMENT.

- o PROBLEM

7. DESIGN SOLUTIONS (CONTINUED)

A. DIE SIZE SHOULD BE ADJUSTABLE

- o KEY QUESTION: HOW LARGE SHOULD THE MODULES BE?

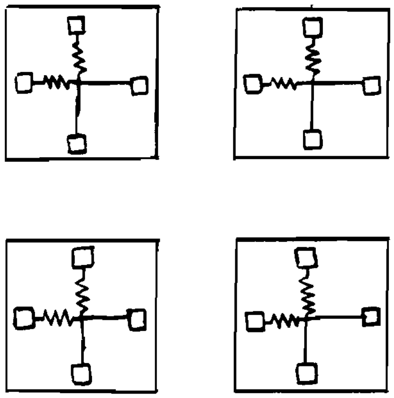


- o SMALL MODULES ALLOW GOOD SIZE FLEXIBILITY BUT LIMIT THE NUMBER OF BOND PADS, AND REAL-ESTATE FOR SENSORS, PER MODULE.

- o LARGE MODULES LIMIT SIZE FLEXIBILITY.

- o MODULAR CHIPS TEND TO LEAD TO WIRE-RELATED DESIGN RULE PROBLEMS.

- o EXAMPLE:



- o PROBLEM:

IS THERE ANY ADVANTAGE TO MAKING THE MODULES RECTANGULAR?

7. DESIGN SOLUTIONS (CONTINUED)

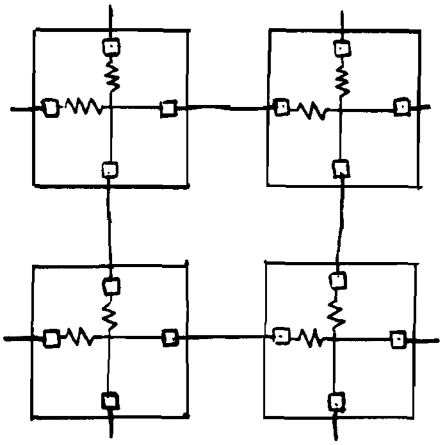
B. WAFER FAB AND ASSEMBLY DESIGN RULES MUST BE OBEYED

o THE CHIPS MUST "LOOK" LIKE PRODUCT CHIPS IN FAB AND IN ASSEMBLY.

o FOR MODULAR CHIPS, THE MOST DIFFICULT DESIGN RULES TO OBEY ARE WIRE-RELATED DESIGN RULES.

o THE SOLUTION IS TO INTERCONNECT MODULES ACROSS SCRIBE LINES.

o INTERCONNECTION ACROSS SCRIBE LINES LEADS TO TESTABILITY PROBLEMS AT THE WAFER LEVEL.



7. DESIGN SOLUTIONS (CONTINUED)

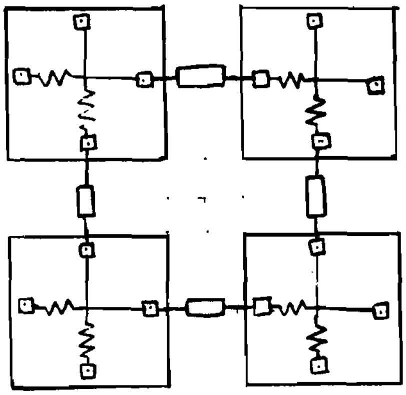
C. CHIPS MUST BE TESTABLE AT THE WAFER LEVEL

o TESTABILITY AT THE WAFER LEVEL IS CRITICAL TO CHARACTERIZATIONS WHICH SEEK INFORMATION ABOUT THE EFFECT OF ASSEMBLY ON CHIPS. NOT SO IMPORTANT FOR STUDIES OF THE EFFECT OF ENVIRONMENT ON PACKAGED CHIPS.

o TEST CHIPS COMPRISING SEVERAL MODULES MUST BE ELECTRICALLY ISOLATED FROM EACH OTHER BEFORE TESTING.

o USE FUSES IN SCRIBE LINES AND DO A DOUBLE PROBE PASS. THE FIRST PASS WILL BLOW FUSES IN THE APPROPRIATE SCRIBE LINES, AND THE SECOND PASS WILL ELECTRICALLY TEST (AND INK) THE ELECTRICALLY ISOLATED TEST CHIPS.

o FOR SOME APPLICATIONS POLYSILICON FUSES HAVE UNACCEPTABLY HIGH RESISTANCE.

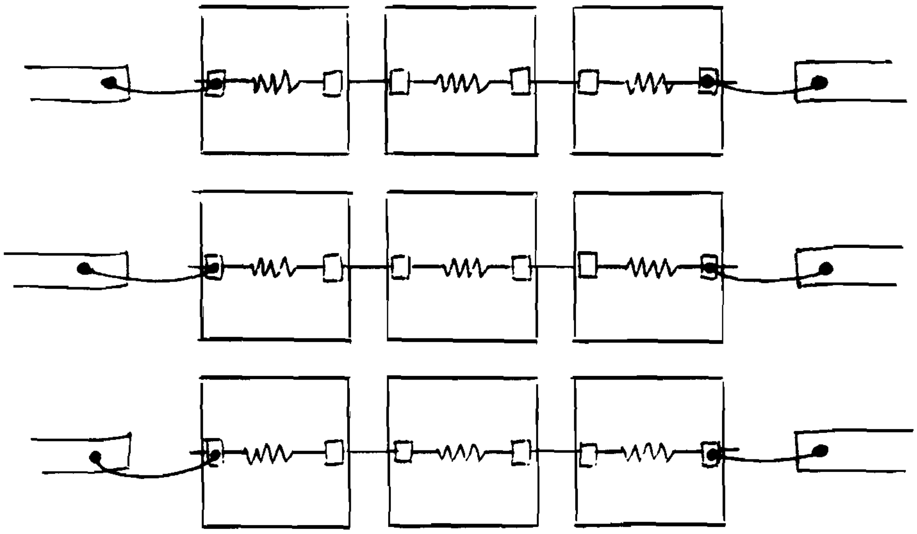


7. DESIGN SOLUTIONS (CONTINUED)

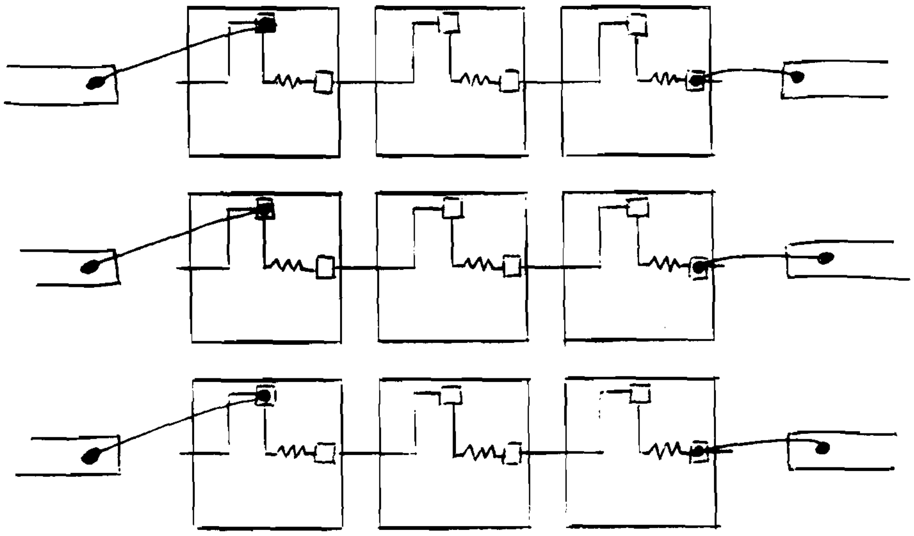
BONDING PAD PLACEMENT

- DISTRIBUTED SENSORS (INTERCONNECTED BETWEEN MODULES): PADS MUST BE ON OPPOSITE EDGES OF THE MODULE. FOR EXAMPLE:

THIS



NOT THIS



7. DESIGN SOLUTIONS (CONTINUED)

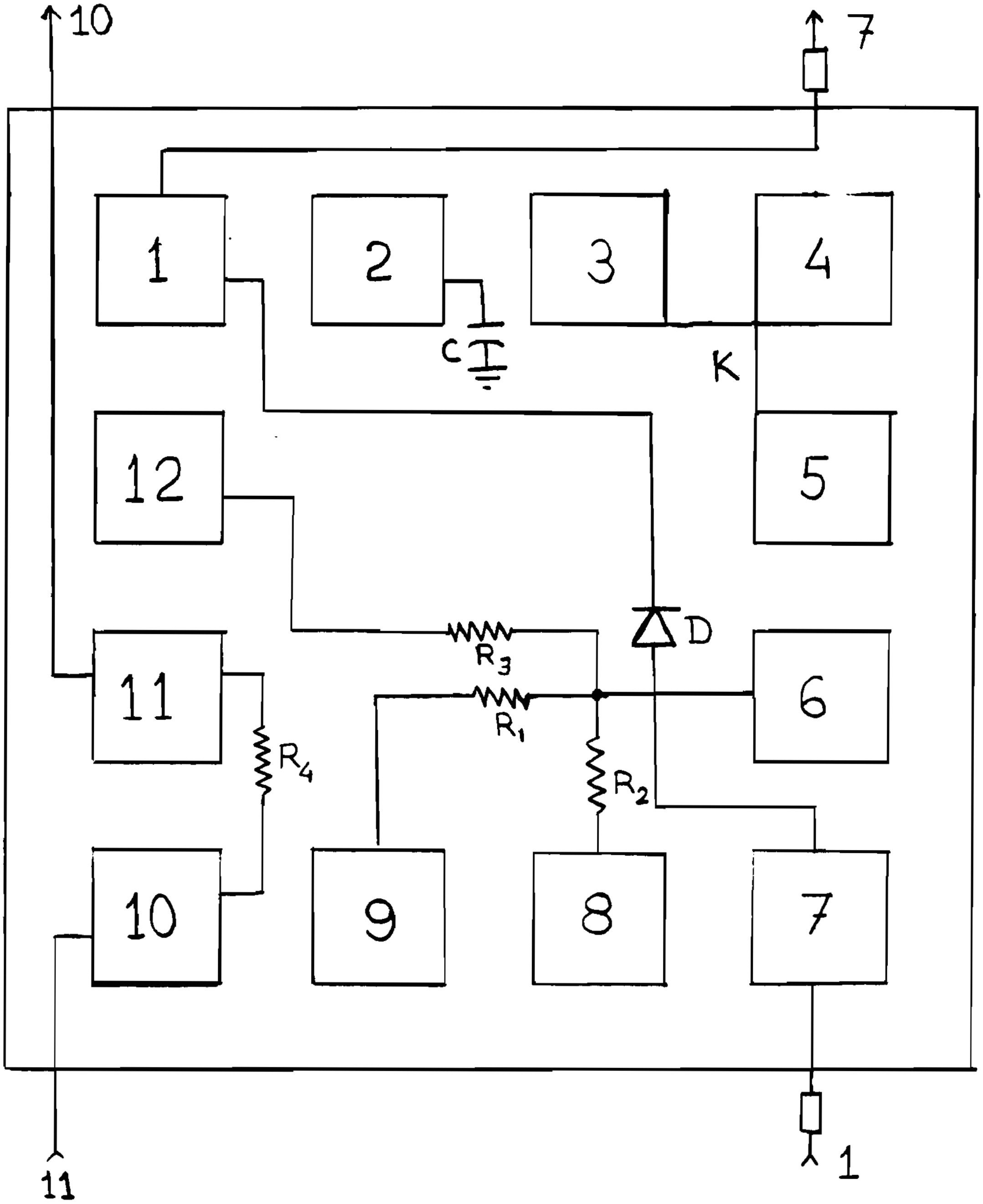
o LOCAL SENSORS (NOT INTERCONNECTED BETWEEN MODULES, ACCESSIBLE ONLY IN MODULES ON THE CHIP PERIPHERY): ACCESSIBILITY RULES ARE...

NO. PADS PER SENSOR	PAD LOCATION ON MODULE	WIRE ACCESS TO CHIP
1	CORNER	2 EDGES
2	BOTH SAME SIDE	1 EDGE
2	ADJACENT SIDES	1 CORNER
2	OPPOSITE SIDES	NOT ACCESSIBLE

o A PROBLEM IS THE BEST WAY TO ILLUSTRATE THESE RULES...

PROBLEM

YOU ARE AN ASSEMBLY ENGINEER WITH THE JOB OF DESIGNING A MODULAR TEST CHIP. YOUR BOSS INSISTS THAT YOU SEEK THE ADVICE OF THE EXPERTS - THE LOCAL VLSI DESIGNERS. YOU'VE NEVER YET SEEN A DESIGN PRODUCED BY THOSE GUYS WHICH TOOK ACCOUNT OF ASSEMBLY DESIGN RULES. SO YOU'RE NOT TOO OPTIMISTIC. STILL, TO DEMONSTRATE THE GOOD ATTITUDE YOU DON'T REALLY HAVE, YOU GO ALONG WITH YOUR BOSS. WEEKS LATER THE VLSI DESIGNERS PRODUCE A DESIGN WITH THE FOLLOWING SCHEMATIC. YOUR MOUTH WATERS. HERE'S YOUR CHANCE TO SHOW THOSE HOT-SHOTS (AND YOUR BOSS) A THING OR TWO. POINT OUT THE ERRORS IN THE SCHEMATIC, AND PRODUCE A CORRECTED VERSION.



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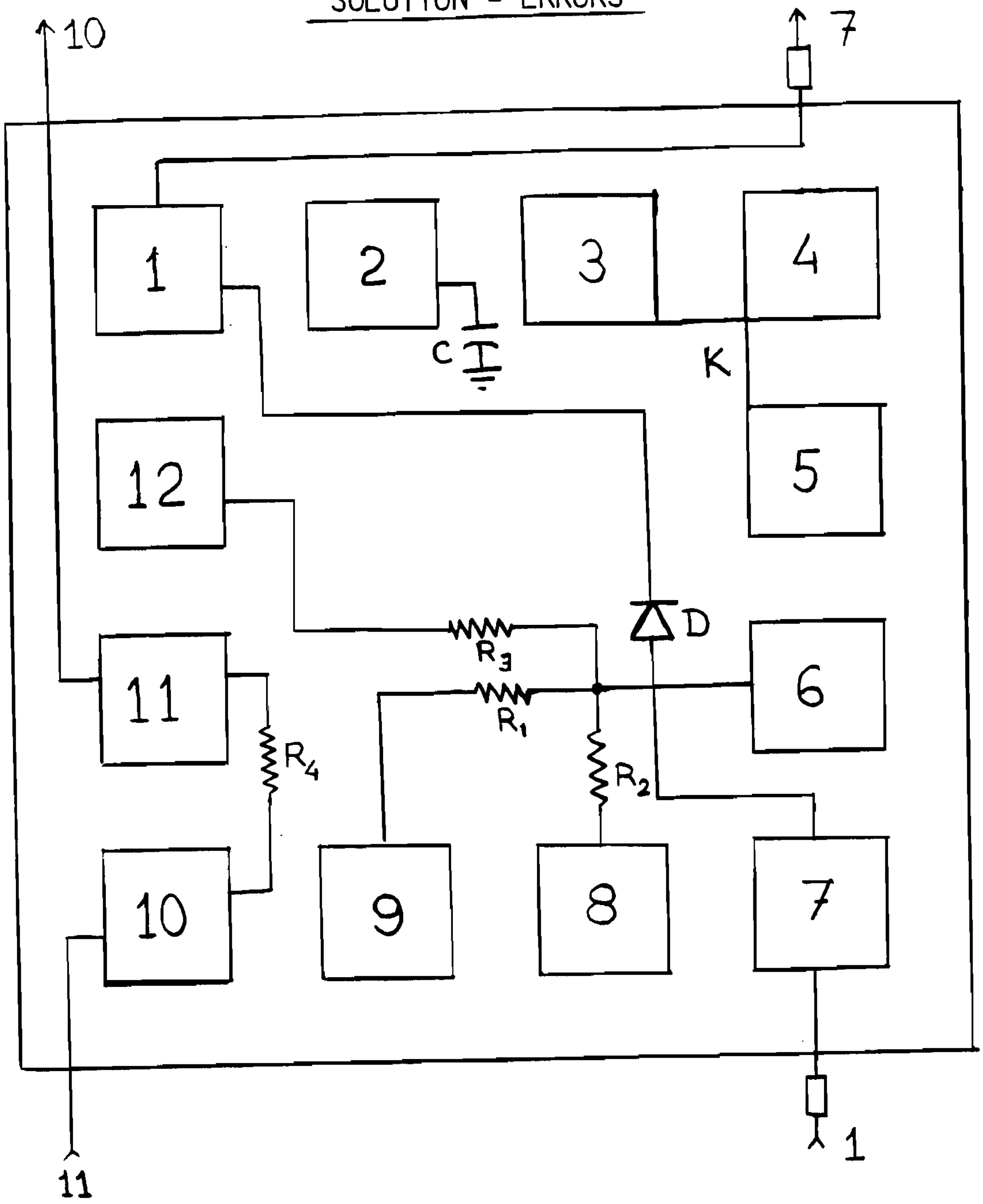
SOLUTION - ERRORS


10
7
1
2
3
4
C
K
12
5
D
R3
11
6
R1
R4
R2
10
9
8
7
1
11

K: ACCESS AT CORNERS ONLY. USES THREE PAD PER DIE.

R3: NOT ACCESSIBLE.

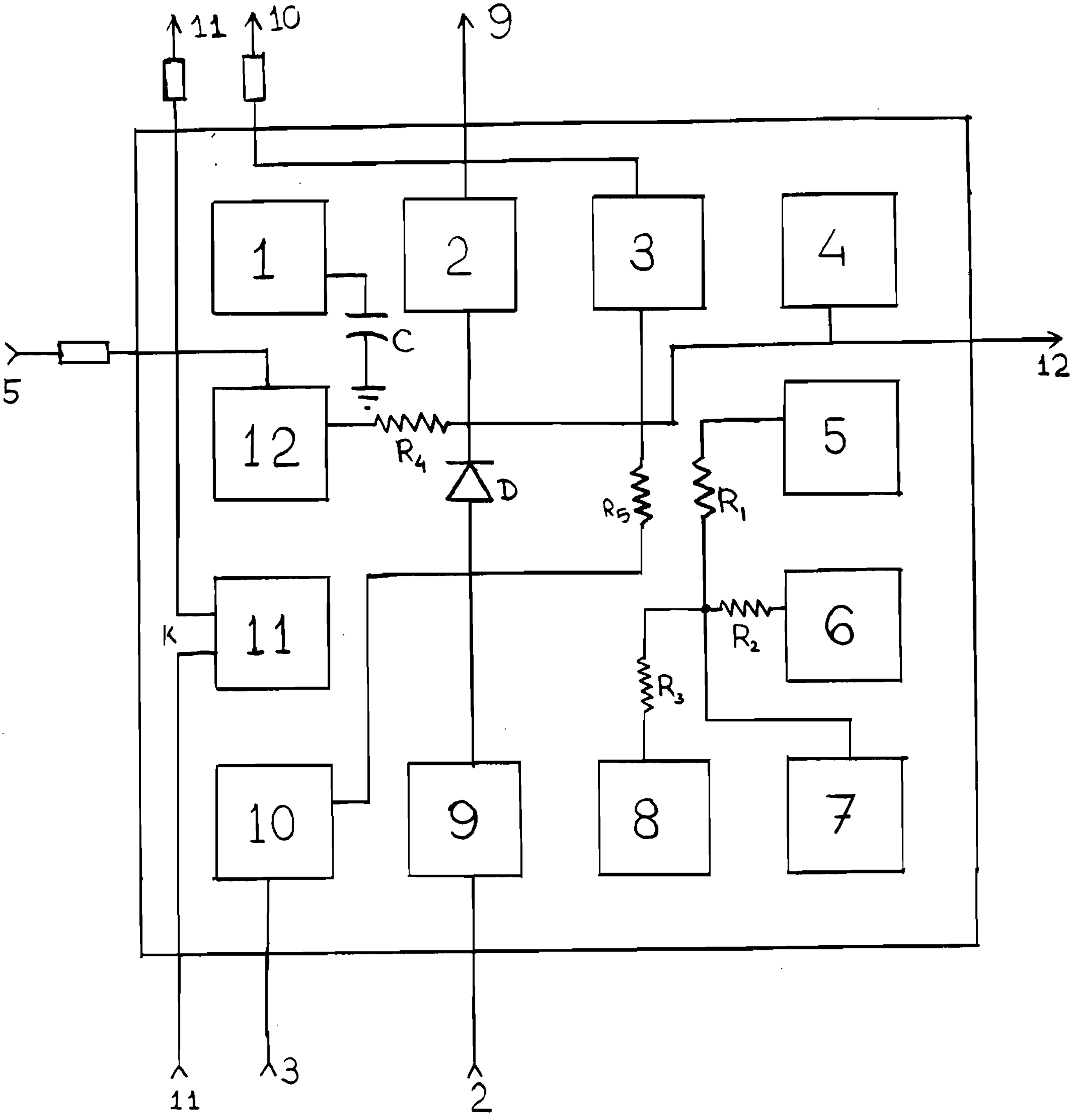
R1, R2: ACCESSIBLE AT ONE CORNER ONLY.

R4 : DOES NOT USE OPPOSITE EDGES. NOT TESTABLE ON WAFER (NO FUSES). WASTES A CORNER PAD.

D: USES CORNER PADS. SHOULD NOT USE FUSES.

C: SHOULD BE ON A CORNER TO ALLOW ACCESS FROM TWO EDGES.

SOLUTION - IMPROVED LAYOUT


11
10
9
1
2
3
4
C
5
12
12
R4
D
R5
R1
5
11
K
R2
6
R3
10
9
8
7
11
3
2

DISTRIBUTING K FROM MODULE TO MODULE FREES UP TWO PADS. IT ALSO MAKES IT UNNECESSARY TO USE THREE PADS ON THE SAME EDGE (A VERY RESTRICTING REQUIREMENT). TWO EXTRA PADS ALLOWS THE ADDITION OF ANOTHER CRACK-DETECTION RESISTOR.