BUILDING IN RELIABILITY FOR PACKAGING AND ASSEMBLY

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ABSTRACT

Rapidly evolving package technology, especially plastic package technology, combined with shortening silicon process and product development cycles, demands increasingly rapid integration of package technology with silicon technology. On the other hand, package reliability evaluation still requires repeated cycles of fabrication, environmental test, and analysis. This forces parallel, modular, highly accelerated evaluation of the major reliability interactions between silicon and package. We survey the major technology trends, and how these affect silicon/package interactions inportant to reliability. Development cycle time may be reduced by replacing 85/85 with HAST and by using assembly-oriented test chips. A key area for future development is the development of models for the prediction of reliability, which will reduce the testing required.

INTRODUCTION

Slide 1. In this talk we cover three main areas. The first is technology trends insofar as they affect package reliability, then a brief overview of package-related failure mechanisms and models, and then we discuss the development strategy used today for building-in reliability for packaging and assembly. As I discuss the strategy we use today I will point out areas of weakness; areas in which we need new knowledge. I'll wrap up the paper by discussing directions for further improving our methods for building reliability into plastic packages.

TECHNOLOGY TRENDS

Slide 2. High-performance VLSI is moving to price-sensitive everyday products so that economics is pushing VLSI into plastic packages. Today, package reliability issues are primarily *plastic* package reliability issues. First, I'll say a few words about package outline and lead frame trends. Die sizes are getting larger, lead counts are increasing, lead pitches are becoming finer, and packages are becoming thinner and wider. Also, copper lead frames are increasingly used to improve electrical and thermal performance, and multiple planes of copper are sometimes employed to even further improve thermal and electrical performance.

Slide 3. Here you see an example of a modern multi-plane plastic package. It's a 100-lead PQFP package; Intel's 80386SX goes into this package. It has a 25 mil lead pitch. Notice the multiple planes of metal insulated from each other by specially formulated tape. This is the last plastic package generation to use gold wire bond. Subsequent generations will use TAB which is capable of bonding to even finer pad pitches than the 150 micron pad pitch for this generation. The multiple planes in this package introduces a completely new combination of materials, which has the potential to strongly affect reliability in new ways.

Slide 4. In this slide, I've summarized parameters such as the maximum number of leads, lead pitch, number of planes and package thicknesses for representative families of plastic packages. Generally the package technology is more advanced as one goes from top to bottom in this table. And each of these technology indicators advances, we get closer to some reliability "cliff". For example, plane-to-plane leakage becomes a possibility with multiple planes, thinner packages are less mechanically stable, finer pitch leads are more likely to short, and more leads gives higher statistical vulnerability to defects.

Slide 5. Interconnect technologies are also changing in the direction of finer pitches. Gold wire bonding is limited to about 150 micron pitch. For finer pitches than 150 microns, TAB is the bonding technology of choice in plastic. TAB has some potential reliability advantages since the leads are more robust than gold wires, and as we'll see below, have some advantage in sealing the edge of openings in passivation at bond pads. On the other hand, bonding forces are higher, so that mis-adjustment can cause new kinds of substrate damage that is not easily detected in production, and only shows up later.

Question: What is TAB? TAB stands for Tape-Automated-Bonding. Its a replacement for wire bonding which uses a prefabricated tape with multiple leads already formed. The leads are then bonded all at once or in groups. The bond pads on the wafer have to be pre-bumped with gold bumps. It is capable of bonding to pitches down to 100 microns.

For ceramic packages, aluminum wire bond can probably reach 125 micron pitches, but for finer pitches than this, C4 (controlled-collapse-chip-connect) is needed.

Next, I'd like to discuss passivations. There are two main requirements for a passivation: (1) The passivation should be hermetic, that is, be a moisture barrier (remember that plastic molding compound is not a barrier to moisture; moisture goes right through it), and (2), the passivation should provide mechanical protection to the die not only from the stresses on the die due to the plastic package (remember that the molding compound is in intimate contact with the die), but also mechanical protection is needed to protect the die during handling throughout the assembly process. There are at least two current approaches to producing passivations which satisfy both mechanical and hermeticity requirements. The first approach involves depositing a layer of thin PECVD nitride over the metallization as a barrier to moisture. This layer cannot be thicker than about half the metal spacing or else voids and other severe grown-in defects occur.

Question. Inaudible. The limit on conformal film thickness occurs because during deposition the film grows from all surfaces equally including the vertical side walls of the metal lines that the passivation is covering. When the nominal film thickness reaches about half the space between metal lines, the film "grows into

itself" leaving trapped voids and other growth defects which provide a moisture path to the circuitry on the die.

On the other hand, the film's effectiveness as a moisture barrier fails at thicknesses much below 0.5 microns, since the film begins to "break up". As spaces between metal lines go below about 1 micron, you can see that the film thickness window available becomes quite narrow. Let's skip over Slide 6 and look at Slide 7 for a moment.

Slide 7. This shows the percentage fallout of SRAMs in temperature cycling (condition C) after 1000 cycles as a function of total passivation thickness due to a mechanism which involved passivation fracture. The devices had only a PECVD oxynitride/ nitride film with no polyimide overcoat. You can see that as passivation thicknesses go below about a micron, they become increasingly fragile. This is the reason for using a compliant coating, such as polyimide, for mechanical protection of inorganic passivation films thinner than about 1 micron. In fact, going back to Slide 5...

Slide 5. You can see that we use a 4 micron thick passivation film for mechanical protection. Although polyimide greatly reduces one potential reliability jeopardy, it introduces another related to bonding, which I will discuss a little later in this talk.

Slide 6. Another approach to passivations for VLSI technologies is to use a reflow glass over the metal, to eliminate the restriction on nitride thickness, since it will not have to fill narrow spaces between metal lines. This too has an influence on the potential jeopardies related to bonding, which I'll describe in a moment. The table in this slide shows a variety of passivation systems compatible with increasingly dense technologies. The first three (1.5 microns down to 0.8 microns) follow the first approach we described, (inorganic film directly over metal plus polyimide for mechanical protection if the inorganic film is thinner than a micron). The last one (not actually in production at Intel) uses the planarizing approach. Let's go to slide 9...

Slide 9. Passivations have to be etched to clear bond pads, so that in developing a reliable passivation, one cannot ignore any bonding-related potential reliability jeopardies. At the top of this slide I have illustrated the case of a wire bond overlapping passivation. We have discovered that moisture (accelerated by HAST stress) in combination with polyimide and off-center bonds leads to bond weakening. (**Slide 8**) We have studied the acceleration factor (to be described in the 1993 IRPS) and find no problem at normal use conditions. At the bottom of the slide we see that a planarized glass/nitride passivation will have exposed reflow glass at the bond edge. The low temperature reflow glasses necessary for planarized passivations are susceptible to moisture, so the pads present a potential reliability jeopardy. This problem could be avoided by an extra masking step, but this kind of solution is anathema to factory productivity.

Slide 10. If we look at slide 10, we see that if TAB bumps are used instead of wire bonds then the lateral moisture ingression issue can potentially be eliminated. As I indicated before, the trend is to replace wire bonding with TAB as pad pitches go below 150 microns.

Slide 11. I have described the technology trends at the component manufacturer, but we cannot forget, of course, the technology trends that are occurring at the customers of the component manufacturer. Today, surface mount has become the mainline board mount process. This process involves a severe thermal shock to 215_C during board surface mount. This causes a rapid expansion of any water vapor absorbed by the package which can fracture the package and cause other internal damage (to, for example, wire bonds). Kris Mohan will be discussing this mechanism in some detail in his following talk. The number of times components can be baked to dry them out is limited by lead finish degradation, so this leads to complex logistics which customers of component manufacturers hate. There are fixes in the works such as less hygroscopic molding compounds and packages with better adhesion between internal surfaces, etc.

PACKAGE FAILURE MECHANISMS AND MODELS

Slide 12. Next I'd like to give a broad overview of package failure mechanisms and models. My purpose is just to give a broad classification of mechanisms, and emphasize just how poorly understood, in quantitative terms, these mechanisms are. As we shall see later, this lack of quantitative understanding forces an expensive, time consuming, fabricate-stress-test development strategy. In general, even intrinsic plastic package failure mechanisms are not well understood. This is in contrast to the silicon world where intrinsic mechanisms are well understood, so that the focus is on understanding and eliminating defect mechanisms.

There are three broad classes of failure mechanisms: Thermomechanical, Thermal, and Moisture-Related.

Thermomechanical Mechanisms.

Thermomechanical mechanisms are those caused by temperature or power cycling, or by "popcorn" cracking. The failure mechanisms are package cracking and delamination at internal interfaces, wire damage, and damage to passivations. There is little consensus on even the form of the acceleration models for these mechanisms: Some say the temperature amplitude should be T_{max}-T_{min}, some say (I think it is more likely, but it's just my *opinion*) it should be the greatest deviation from the temperature at which stresses are neutral. Large ranges for Coffin-Manson exponents, M, appear in the literature. Parametric dependence on dimensions (package thickness, die area, buss widths, passivation thicknesses, etc.) are crude.

I include in the thermomechanical classification the "popcorn fracturing" seen in surface mount technology. Kris Mohan will be describing this in some detail in the talk following mine.

Thermal Mechanisms

These are the best understood of the package mechanisms since the acceleration models have simple Arrhenius forms, and there is no dependence on package dimensions etc. Because of this, these rarely crop up as reliability issues. They can be controlled by ensuring that the thermal history of the process does not lead to significant degradation. A couple of examples are the classical "purple plague" of wire bond degradation described by Elliot Philofsky years ago, and the lead finish degradation I have already mentioned.

Moisture Mechanisms

Slide 13. These are chemical mechanisms accelerated by temperature, humidity, and bias. The classical mechanism most people are familiar with is corrosion of aluminum metallization. Actually, improvements in molding compounds (mostly elimination of hydrolyzable chlorine) have eliminated metal corrosion as an issue in modern processes. However, there are plenty of new

moisture-related mechanisms to contend with. Most of the new ones have to do with the internals of the package or with moisture penetration of the die. Multi-planar plastic packages (which I described earlier) are particularly vulnerable to moisture-related interplanar leakage. Also, more fragile moisture barriers in passivations and lateral diffusion from the die edge create potential new moisture failure mechanisms. Charles Hong has a talk at this conference in which he describes a new failure mechanism which involves *lateral* moisture diffusion from the edge of the die where film edges are exposed by the saw cut.

One final point I'd like to make moving on to the next topic is that package mechanisms and models are MUCH less well understood than wafer-level models such as oxide reliability, electromigration, etc.

DEVELOPMENT STRATEGY

Slide 14. Now that you have an idea of the current state of package technology and of the parts of silicon technology which interact with the package technology, and of the current state of knowledge about failure mechanisms and models, I'd like to show how we currently build package reliability into components.

Reliability must be built into packages in an environment described in this slide. First, we have only 2-3 years to develop each new package technology, typically in parallel with development of a new generation of silicon technologies, and driven by product introduction strategies. Let's jump forward and look at Slide 17.

Slide 17. This slide shows how plastic package and silicon technologies are evolving in parallel. Thus, plastic package technologies are not developed for a single static silicon technology, but is evolving in parallel. Thus there must be a significant amount of synergy between silicon and plastic package development activities, and I will show you how we accomplish this. Let's go back to **Slide 14**...

Slide 14. Another fact of life, which I've already shown you, is that reliability models are inadequate for extrapolation of package and package-die interactions to different dimensions, and to environmental conditions other than the accelerated test conditions (including to use conditions). Thus, we're forced into a fabricate-stress-test cycle for the most demanding package and die size available.

Also, because of inadequate models, we're forced to employ arbitrary standards to gauge satisfactory performance because we have no idea how the "old war-horse" industry standards relate to use conditions.

Slide 15. In this development environment, we have arrived at an approach which is quite effective in building-in package reliability in a timely fashion. The approach is essentially a process of minimizing risks in each part of the technology even before the entire technology can be exercised. That way, when all the pieces are finally put together in a flagship product, any remnant "interactions" will be minor and easily dealt with.

Specifically the approach is to shorten and parallelize the development cycle by modularization, by short loop processing, and by use of test vehicles designed for electrical testability. The time-to-information can be reduced greatly by using highly accelerated stresses, as long as very careful correlation to lower stresses is done to ensure that spurious mechanisms are not introduced. There is also a continuing effort to minimize the number of cases which need to be tested, this requires an improved understanding of what defines the "outer edges" of the technology window. The simplest example is, if the largest die possible in a package satisfies reliability standards, then smaller dice in the same package may be assumed to satisfy the standards also.

One absolutely key concept is that to build in reliability, it must be developed-in when the technology is being defined. Then reliability will automatically be built into the high volume production process when it is transferred out of development. In my opinion, the concept of building in reliability in a high volume production factory, as something distinct from normal process control, is wrong and dangerous. Reliability engineers should only be employed in developing technologies and, to a lesser extent, in developing products, they have no place in a well-run manufacturing environment. At least, that is the ideal we should be aiming for. (If design tools were perfect, they wouldn't be needed in product development either.)

Slide 16. I'd like to explain in more detail what I mean by modularization and short-loop processing. To characterize the reliability of a package/assembly technology we use three methods. Wireless packages very quickly provide information about the package-only mechanisms (such as the plane-plane leakage mechanisms I described earlier). This does not test everything of course, but it has the virtue of being *fast* because you don't need to be involved with the Fab's production schedule. Next, special test chips can be used to understand intrinsic die-package interactions. These are good for converting gross (intrinsic) failure mechanisms into easily-interpreted electrical signals. This can be pretty fast too, since testing and interpretation (including failure analysis), can be simple. Finally, we need to use the SRAM to understand defect modes. Another way to look at this is shown in Slide 18...

Slide 18. This shows the parallel development of the assembly process on the left and the silicon process on the right, culminating in the fabrication of a flagship product in the new package and silicon technology. The dashed lines are information feedback loops. I have just explained two of the loops shown at the upper left of this slide (wireless package/test chips, and SRAM for defects). A similar activity occurs in development of silicon technology without strong involvement with assembly. This is shown in the upper right-hand corner of this slide. Since many at this conference are familiar with wafer-level reliability, I'd like to point out the analogous role of special test chips and wireless packages in developing-in package reliability to the role of wafer-level reliability in developing-in reliability in the silicon technology. A lot of activity is embodied in the dashed-line feedback loops in this diagram. One activity is fabrication of silicon test vehicles. This can be shortened by using partially processed silicon to explore specific aspects of the package-die interaction. For example, wire bonding evaluations need a complete thin film metal/dielectric stack under the bond pads, but they do not need gate oxides, diffusions, etc.

Slide 19. Time taken to perform environmental stress is also a major contributor to the time-to-information in those dashed feedback lines. This slide is a typical environmental flow which produces reliability information. The most time consuming stress in this flow is the 1000 hour 85/85 standard THB test and the moisture saturation time in preconditioning. HAST can reduce both of these times by 5X or better. Temperature cycling also takes a long time, and there is scope for shortening the time by increasing the cycling frequency (NOT by increasing the amplitude or by using liquid-liquid shock!). Failure analysis is also time consuming and can be shortened by using more intelligent test vehicles which provide more informative electrical signatures of failure. Jim

Sweet's talk today will cover more detail about test chips that could be used as part of this strategy. There is a lot of scope for improved optimization and efficiency in the information feedback loop.

FUTURE

Slide 20. Let me wrap up this talk by saying that the quickening pace of technology has forced us to come up with ways to build reliability into package/assembly technologies, particularly plastic technologies, which are in synch with the pace of process development in silicon, and with the pace of introduction of new VLSI-enabled low-cost products such as PCs printers, etc. We are now keenly aware that reliability must be developed-in so the main focus of my talk has been the development cycle.

In the course of the talk I have mentioned several areas in which improvements and further efficiencies are possible. In closing, I'd like to collect them. First, a better understanding of thermomechanical and moisture mechanisms and models would allow extrapolation and simulation of reliability, and reduce the need for fabricate-stress-test activity. Second, better models would allow us to use sensible environmental standards rather than the arbitrary ones used today. (We may well be over-stressing in some cases.) Improved accelerated test methods can shorten the information feedback cycle. For example, we use HAST to accelerate the information feedback cycle. We can't we also speed up temperature cycling by increasing it's frequency. The mil spec is very slow, and there is scope for increasing the frequency. Finally, test chips could be used which provide easier-to-interpret electrical signals. Today, we use open/short test chips because they are easy to interpret and to fabricate. More sophistication is feasible, but formal standards and test methods are needed so that people who are not test chip "experts" can use them. Jim Sweet will be discussing package test chips in some detail in his talk later.

Question: What HAST conditions would you use instead of 85/85? The highest JEDEC standard condition is 140/85, but the highest condition about which there is no controversy is 130/85, so I think that 100 or 200 hours of 130/85 has the potential to be a standard that will replace 85/85. We have good experience with higher conditions, so I think we'd like to aim for a 140/85 standard. In fact, in development we use the highest condition which our chamber allows, which is 156/85 to get information as fast as possible. We do correlations to verify that the mechanisms observed at 156/85 are the same as at 85/85. We find that about 40 hours at 156/85 is predictive of failure rates at 1000 hours of 85/85.

Question. How should we go about modeling and simulation of package reliability? A semi-empirical approach is needed. Someone cannot just sit at the screen of a workstation and "simulate". One of the key properties required in simulation of package mechanics are interfacial adhesion parameters. These are very process-dependent, depending on the exact silicon process, the specific passivation used, the molding compound used, etc. So you need to have the tools and methodologies (Instron machines, etc.) right in your own lab to get the critical parameters for your own process. So the first step in doing modeling is to get that kind of data, using specially fabricated test structures, not packages - they're too complicated and hard to interpret.

BUILDING IN RELIABILITY FOR PACKAGING AND ASSEMBLY

C. Glenn Shirley, Intel

Technology Trends

Package-Related Failure Mechanisms and Models

Development Strategy

Future

SLIDE 1

TECHNOLOGY TRENDS

High-performance VLSI is moving to price-sensitive everyday products.

Economics is pushing VLSI into plastic packages.

Package reliability issues are mainly *plastic* package reliability issues.

Package Outline Trends

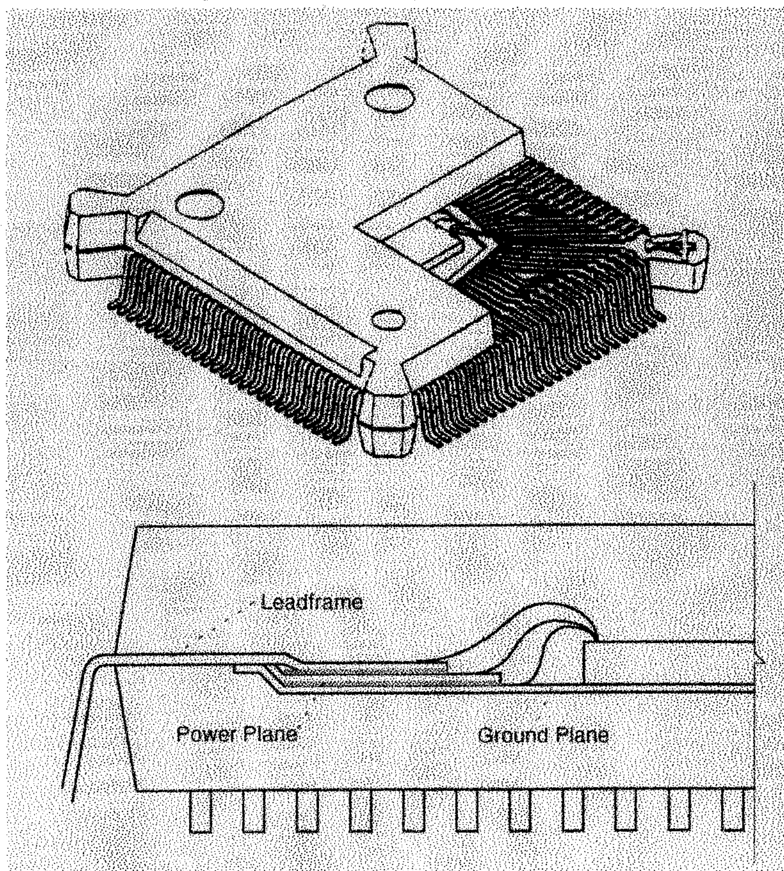
- Die sizes are larger (apprx 500 mils and up)
- Higher lead count. (Reliability statistics).
- Finer pitch leads. (Pin-pin leakage/shorts.)
- Thinner, wider packages. (Less thermomechanical stability.)

Lead frame Trends

- Copper lead frames for improved thermal performance. (Si/Cu TCE mismatch.)
- Multiple planes of metal separated by insulating tape for thermal & electrical performance. (Tape/Cu chemical reactions in moisture and bias.)

SLIDE 2

TECHNOLOGY TRENDS



SLIDE 3

TECHNOLOGY TRENDS

	Max No. of Leads	Lead pitch (mils)	No. of planes	Pkg. thickness (mils)
DIP	48	100	1	185
PLCC	84	50	1	160
TSOP&	32	20*	1	40
PQFP	196	25	1	120
PQFP/DPH	196	25	2	120
PQFP/MM	196	25	3	120
HDPQFP	>296	16#	2	95

DIP = plastic dual in-line. PLCC = plastic leaded chip carrier. TSOP = thin small-outline plastic package. PQFP = plastic quad flat pack. DPH = integral (second plane of metal) die-pad heat-spreader. MM = multi-layer metal quad flat pack. HDPQFP = high density plastic quad flat pack.

Notes: * = 0.5 mm exactly, # = 0.4 mm exactly, & = alloy 42 lead frame (all others in table are copper).

SLIDE 4

TECHNOLOGY TRENDS

Interconnection Technology Trends:

- Increasing lead count is demanding finer pitch bond pads.
- Plastic: Gold wire bonding pitch > 150 μ.
- Plastic: TAB bond pitch > 125 μ or 100 μ. (Bump-passivation overlap = new failure mechanisms.)
- Ceramic: Al only, 125 μ pitch, then 100 μ pitch, then C4 75 μ pitch.

Passivation Trends:

- *Hermetic*, and *mechanically robust* passivations needed for plastic.
- Approach 1. Nitride/polyimide.

Nitride is moisture barrier. Process window: 0.5 μ < thickness < metal space. (Nitride can affect metal voiding.)

Polyimide is mechanical protection. 4 μ thick (Polyimide can affect bond strength.)

SLIDE 5

TECHNOLOGY TRENDS

- Approach 2. Reflowable glass/nitride

Planarize metal topography before nitride deposition

Nitride thickness is not limited by the top metal spacing.

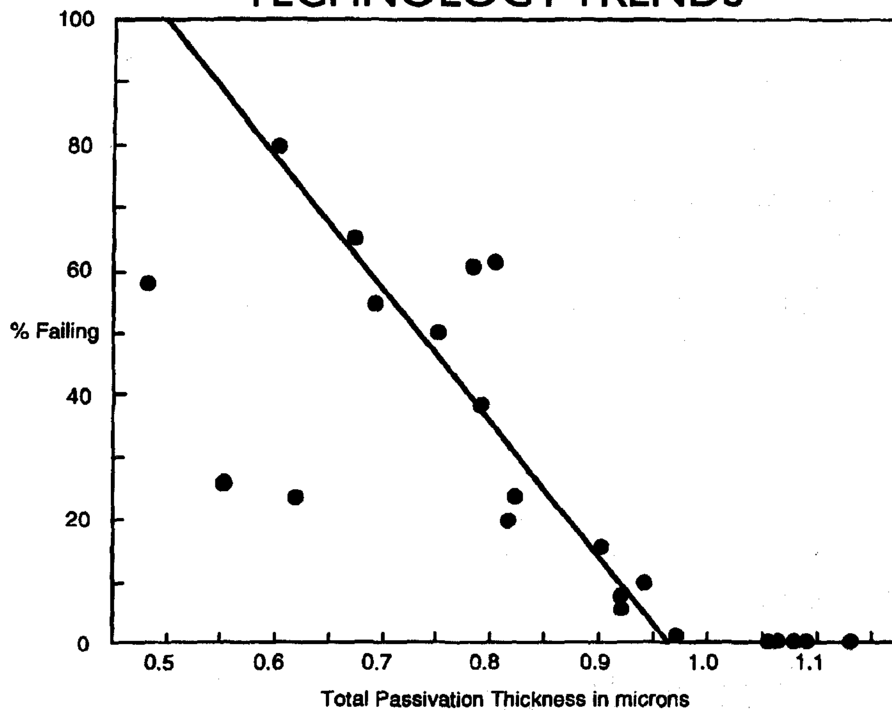
For single mask, exposed glass thin films at bond pad openings admit moisture for wire bond, but not TAB.

EXAMPLES OF PASSIVATION SYSTEMS

Technology	Top Metal Pitch/Space(μ)	Passivation (Bottom/Top)
1.5 μ	6/2	1 μ plasma oxide/1 μ oxynitride
1.0 μ	3.1/1.6	0.6 μ oxynitride/0.3 μ nitride/4 μ polyimide
0.8 μ	2.4/1.2	0.6 μ oxynitride/4 μ polyimide
0.6 μ	1.8/0.9	1.7 μ PTEOS/0.6 μ nitride

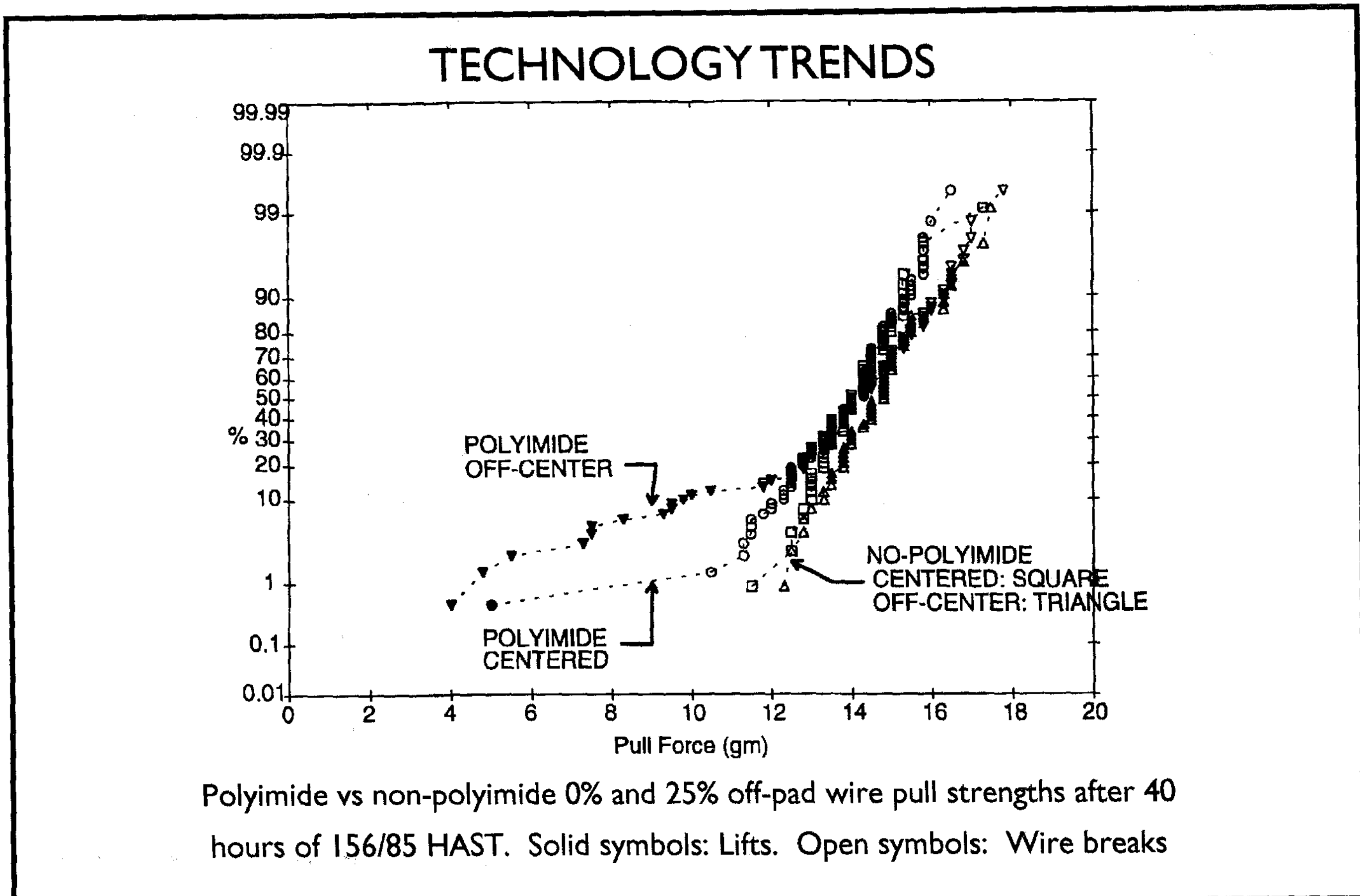
SLIDE 6

TECHNOLOGY TRENDS



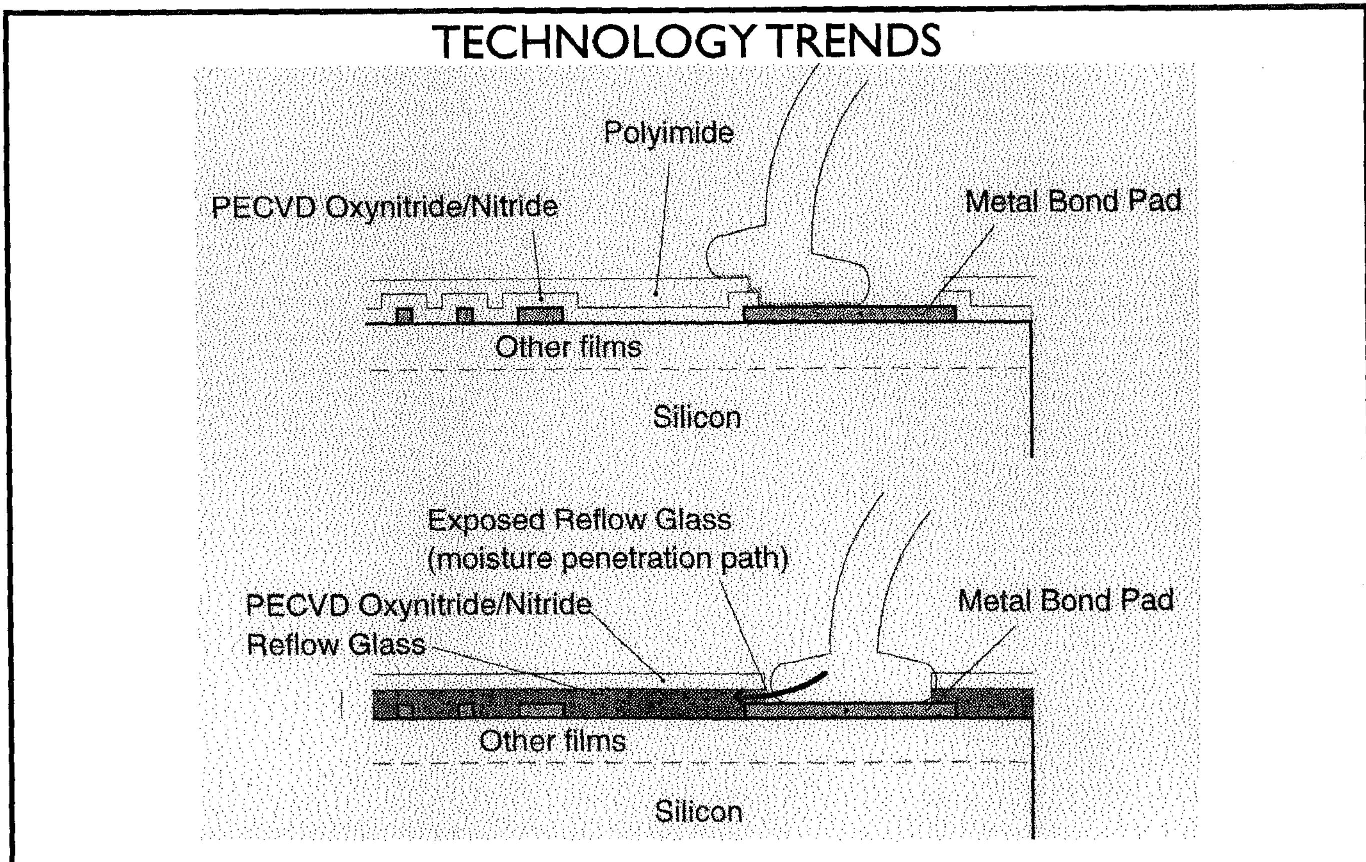
Cumulative SRAM failures after 1k cycles of T/C C versus oxynitride/nitride passivation thickness. Packaged in PDIP, no polyimide die coat.

SLIDE 7



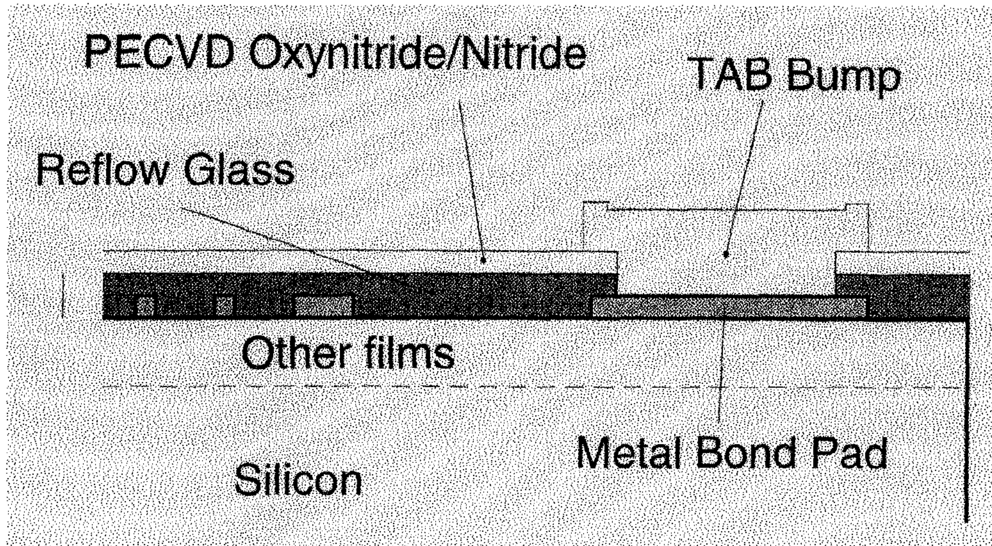
Polyimide vs non-polyimide 0% and 25% off-pad wire pull strengths after 40 hours of 156/85 HAST. Solid symbols: Lifts. Open symbols: Wire breaks

SLIDE 8



SLIDE 9

TECHNOLOGY TRENDS



SLIDE 10

TECHNOLOGY TRENDS

Customer Board Mount Process Trends.

- Surface mount plastic is the mainline board mount process.
- Severe thermal shock to 215 _ C (solder reflow temperature) during board surface mount.
- The big issue is "popcorn" fracture (and other damage) during surface mount due to absorbed moisture.
- Re-bake options are limited by solder wettability degradation. Solder wettability affects *board-level* yield and reliability.
- Customers hate the complex bagging, shipping, shelf-life guidelines required to keep parts dry.
- Fixes: Less hygroscopic mold compounds, better internal adhesion & package integrity.

SLIDE 11

PACKAGE FAILURE MECHANISMS AND MODELS

Thermomechanical (Accelerated by T/C)

- $AF = Const. \times (T_{max} - T_{neutral})^M$, $M = 2 - 20$
- Package cracking (larger die, thinner packages). $M = 20$.
- Plastic delamination (larger die, thinner packages) $M = ?$
- Wire damage (more wires) . $M = ?$
- Thin film cracking. $Const = Const' \times (\text{bus width/pass. thickness})^2$

Thermal (Accelerated by bake)

- $AF = Const. \times exp(-Q/kT)$
- Wire bond degradation (particularly Au) $Q = 1.2$ eV
- Lead finish degradation. $Q = 0.74$ eV

SLIDE 12

PACKAGE FAILURE MECHANISMS AND MODELS

Moisture (Accelerated by THB, and steam)

- $AF = Const. \times F(V) \times H^M exp(-Q/kT)$ ("Peckian")
- External package. $M = ?, Q = ?$
- Internal Package (New interplanar insulating tape). $F(V) = V$, $M = 5\text{-}12$, $Q = 0.75$eV.
- Internal Die
  - passivation (thinner moisture barriers) $F(V) = 1 \cdot 0.6V$, $M = 4.6$, $Q = 0.8$eV *(single bit failures)*,
  - corrosion $F(V) = V(?)$, $M = 2.7$, $Q = 0.8$ eV *(Peck)*
  - thin film delimitation (large die) $Q = ?$.

Package mechanisms and models are MUCH less well understood than wafer-level models such as oxide reliability, electromigration

SLIDE 13

DEVELOPMENT STRATEGY

Today's problems:

- *Timing*. Have 2-3 years to develop a new package technology in *parallel* with silicon technology.
- *Models are inadequate* for extrapolation or simulation of package and package-die interaction reliability, so
- Package reliability requires fabricate-stress-test for many cases.
- *Arbitrary standards* unrelated to use conditions. Eg.
  < 0.5% failure at 1000 hours of 85/85.
  < 1% failure after 1000 cycles of T/C C.
  < 1% failure after 168 hours of 121/100 (steam).

SLIDE 14

DEVELOPMENT STRATEGY

Solutions are:

- Shorten and parallelize the cycle by
  modularization
  short-loop processing
  maximize use of test vehicles designed for electrical testability
- Further accelerate stresses.
- Improve models to extend technology window without actual test of every case.

Develop-in reliability, don't retrofit in high volume production.

SLIDE 15

DEVELOPMENT STRATEGY

Modularization:

- Use *wireless package* to understand intrinsic package-only mechanisms.
- Use *test chips* to understand intrinsic package-die interaction (die attach, wire/TAB bond, passivation).
- Use *SRAM* to understand major defect failure modes, develop (defect) yield- reliability models and production defect monitoring tools.

Short-loop processing:

- Use back-end short loops (metal/passivation) to screen passivation, metal, bond pad stack options.
- Shortest loop of all: *Empty package!*

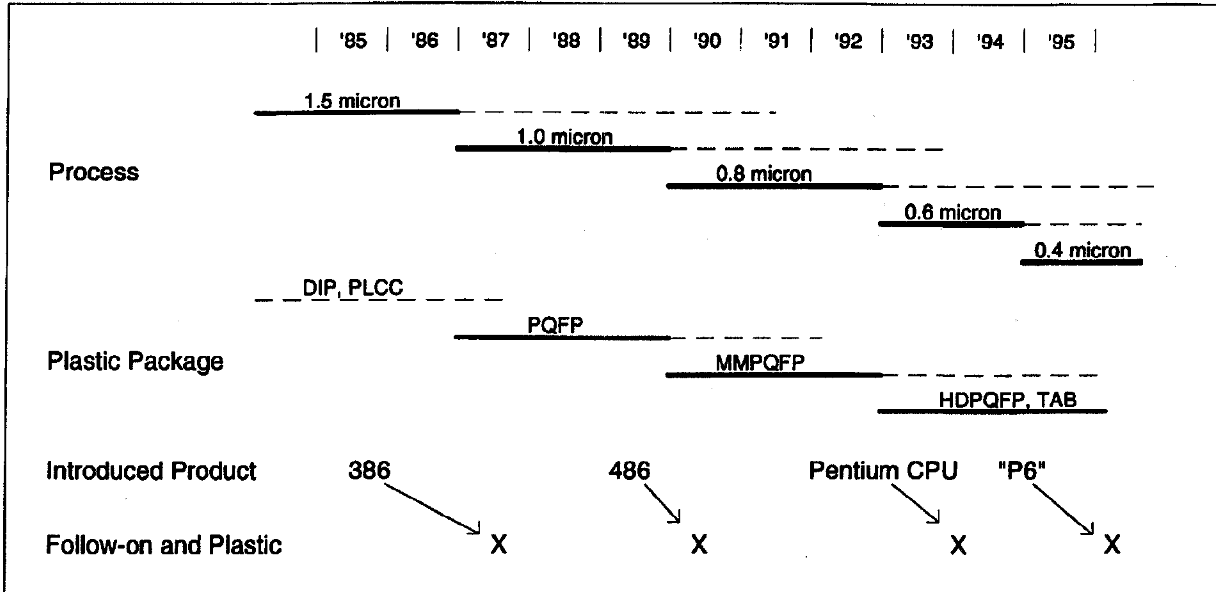
Modularization and short loop processing can only demonstrate that a process/package is inadequate, it cannot prove that it is adequate.

The purpose is to *minimize risk* before the flagship product is produced.

SLIDE 16

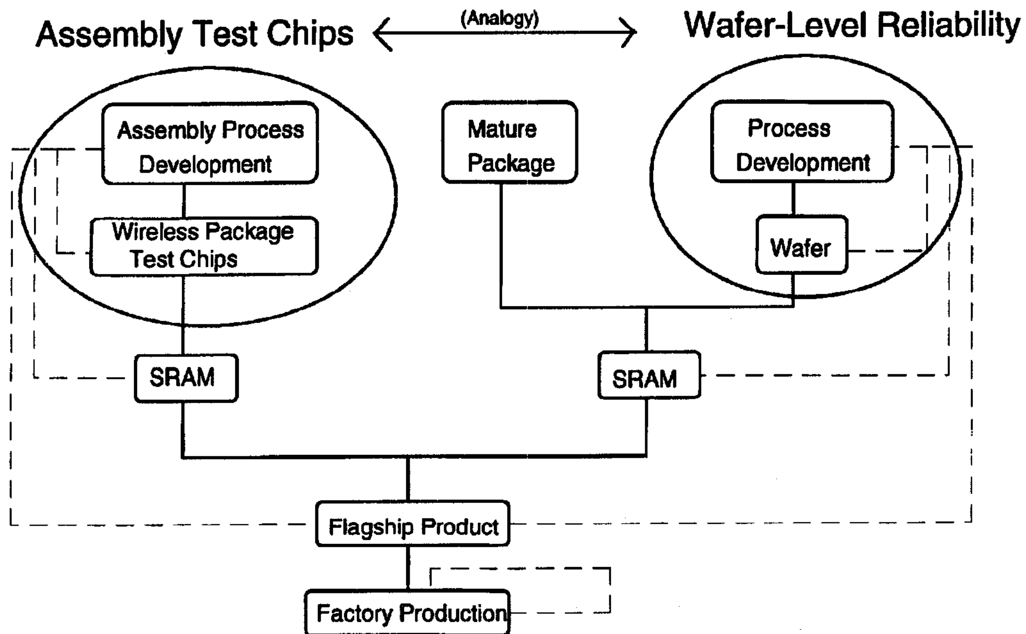
DEVELOPMENT STRATEGY

Timing and parallel development of package, silicon technologies, and product design...



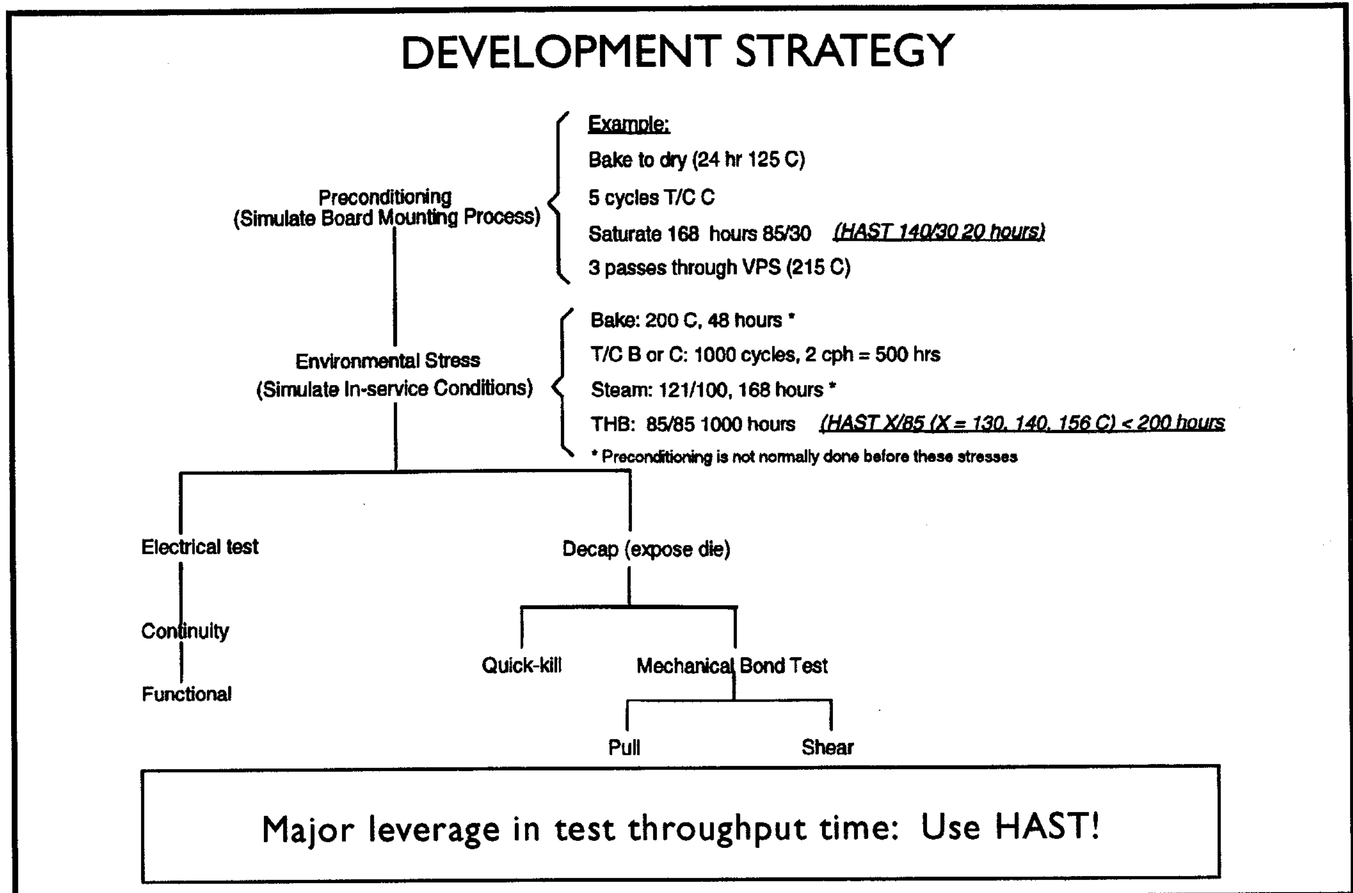
SLIDE 17

DEVELOPMENT STRATEGY



Need for parallel development drives a modular approach. Wafer-level reliability techniques modularizes silicon aspects, empty package and test chip techniques modularize assembly aspects.

SLIDE 18



SLIDE 19

FUTURE

To better build-in reliability for packaging and assembly we need:

- Better models for extrapolation and simulation of reliability.
  - Thermomechanical models of package mechanics incorporating realistic crack propagation and adhesion properties.
  - Moisture acceleration models.
- Sensible environmental standards.
- Improved accelerated test methods
  - Particularly HAST.
  - Higher frequency temperature cycle?
- Better test chips
  - Beyond open-short.
  - Test chip standards and test methods.

SLIDE 20